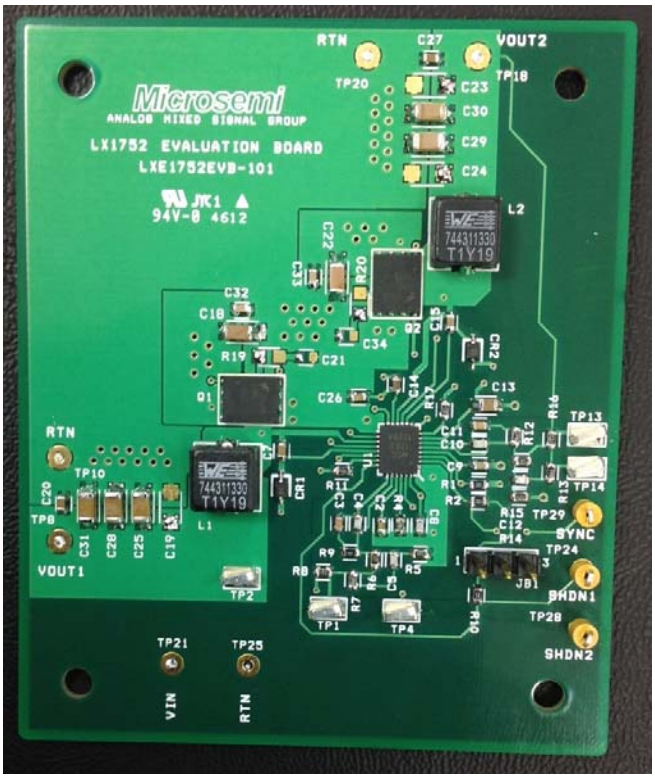
LX1752EVB - 101

Dual Interleaving PWM Controller

Evaluation Board



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Rev. 1.0, 2012-12-05

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

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Introduction to Product

LX1752 is a dual output, PWM controller. It is designed to generate two independent output voltages. Multiple LX1752 ICs can be synchronized to an external clock, or slaved to a single LX1752 IC operating as a master. The LX1752EVB - 101 Evaluation board is configured for 5V and 3.3V outputs, however these voltages can easily be changed by a single resistor value change (1 per output). The evaluation board is capable of continuous output currents up to 5 Amps with the components installed.

Features:

Dual Output with individual input voltages for each output.
Jumper selectable phase positioning for interleaving of 2 LX1752 ICs in synchronized operation.
Can be synchronized with external clock signal.

Operation

The LX1752EVB - 101 Evaluation Board has a single input for power, and two outputs for powering external loads. A power supply capable of 9V to 15V at a minimum current of 5 Amps is required for full output load operation. The LX1752EVB - 101 Evaluation Board is optimized for 12V +/- 10% power supply input. Multiple LX1752s may be synchronized together by connecting together their respective sync signals (available at TP29 on the evaluation board). Synchronizing to an external clock is possible by connecting TP29 through an open drain switch to ground and driving the switch with a 100ns pulse at a frequency 5% higher than the set PWM frequency. Two synchronized LX1752s can be interleaved in a three output, 120°degree phase, or a four output, 90° phase configuration by changing the state of the PSET input. PSET input is determined by the jumper position on JB1 and is shown in Table 1:

Table1

LX1752 Phase Position			
JB1 Jumper Position	PSET Input	VOUT 1 Phase Position	VOUT 2 Phase Position
2 - 3	Ground	0°	180°
Open	Open	90°	270°
1 – 2	High	120°	240°

The LX1752 Evaluation board is configured to operate at 800kHz switching frequency, with outputs set at 5.0V and 3.3V. The Output Voltage can be changed by changing the value of R5 (VOUT1), and R14 (VOUT2). The value of these resistors can be determined as follows:

$$R = \frac{14.7 \times 10^3}{V_{OUT} - 0.7}$$

Note: the above equation is based on the default compensation component values.

The switching frequency can be changed by changing the value of R4. R4 is found by:

$$R_{FREQ}(K\Omega) = \frac{1}{27.56E^{-9} \times F_{OSC}} - 5.156$$

Note: Changes in PWM frequency (without changing the inductor) will change inductor ripple current (ripple will increase significantly at lower frequencies), and subsequent output ripple voltage. Depending on load current, the maximum saturation current rating of the inductors could easily be exceeded at lower switching frequencies. The inductors installed in the LX1752 Evaluation board have a saturation current rating of 9 Amps for both VOUT1, and

VOUT2. The closed-loop bandwidth of the LX1752 Evaluation Board is set at 80kHz with a 12 Volt input; lower switching frequencies will require changing the compensation components. See the applications information section in the LX1752 Datasheet for details.

The following tables describe the test point signals available on the LX1752EVB - 101 Evaluation Board.

Test points

Test Point	Description
TP1 & TP2	Measurement points for a Network Analyzer, such as AP Industries model 200. Used to generate Bode Plot for closed-loop analysis of compensation components. TP1 and TP2 are connected to each side, respectively, of a 20Ω resistor, in line with the feedback signal from VOUT1.
TP4	Buffered VREF output. Provides a source for 0.8V reference.
TP13 & TP14	Measurement points for a Network Analyzer, such as AP Industries model 200. Used to generate Bode Plot for closed-loop analysis of compensation components. TP13 and TP14 are connected to each side, respectively, of a 20Ω resistor, in line with the feedback signal from VOUT2.

Input and Output Connection Points

Test Point	Description
TP21 & TP25	Power and Ground connection for LX1752s VIN pin. TP21 is supply positive; TP25 is supply return. TP21 is jumpered to V1 (TP22) and V2 (TP23) on the LX1752 Evaluation Board, but may be disconnected from V1 and V2 and ran separately. Supply voltage on TP21 is limited to 22V.
TP8 & TP10	Output load connection for VOUT1. TP8 is output positive; TP10 is return. Capable of 5 Amps max. output current at 3.3V.
TP18 & TP20	Output load connection for VOUT2. TP18 is output positive; TP20 is return. Capable of 5 Amps max. output current at 1.2V.
TP24	Test Point connection for SHDN1 pin. May be used to monitor the discharge portion of hiccup mode during a fault condition. This signal switches low during the discharge portion of hiccup, and switches high during the recovery (soft start) portion of hiccup. Primarily used for test, but can be used as a fault monitor at the system level.
TP28	Test Point connection for SHDN2 pin. May be used to monitor the discharge portion of hiccup mode during a fault condition. This signal switches low during the discharge portion of hiccup, and switches high during the recovery (soft start) portion of hiccup. Primarily used for test, but can be used as a fault monitor at the system level.
TP29	Sync Signal. Can be connected to another LX1752 sync pin for synchronous operation. May also be connected to an external sync clock by connecting TP29 to an open drain switch to ground and driving the switch with a 100ns pulse at a frequency 10% higher than the PWM frequency set by R4. The LX1752 syncs on the falling edge of Sync signal.

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LX1752EVB-101 Evaluation Board BOM

Item Number	Quantity	Part Reference	Description	Manufacturer	Manufacturer Part Number
1	REF		Schematic, LX1752 Evaluation Board	Microsemi	24720 X1
2	1	PCB	Printed Circuit Board, LX1752EVB-101 Evaluation Board	Microsemi	SGE3270 X1
3	2	CR1,CR2	Diode, Schottky, 30V 100MA SOD323	Central Semi	CMDSH-3
4	2	C2,C9	Capacitor, Ceramic, 0.22uF, 10V, 10%, X5R, 0603 Case	Panasonic	ECJ-1VB1A224K
5	2	C3,C11	Capacitor, Ceramic, 3.3nF, 50V, X7R, 0603 Case	Panasonic	ECJ-1VB1H332K
6	2	C4,C10	Capacitor, Ceramic, 22pF, 50V, NPO, 0603 Case	Panasonic	ECJ-1VC1H220J
7	1	C5	Capacitor, Ceramic, 330pF, 50V, NPO, 0603 Case	Panasonic	ECJ-1VC1H331J
8	5	C7,C15,C20, C26,C27	Capacitor, Ceramic, 0.1uF, 16V, 10%, X7R, 0603 Case	Panasonic	ECJ-1VB1C104K
9	1	C8	Capacitor, Ceramic, 470pF, 50V, NPO, 0603 Case	Panasonic	ECJ-1VC1H471J
10	1	C12	Capacitor, Ceramic, 220pF, 50V, NPO, 0603 Case	Panasonic	ECJ-1VC1H221J
11	1	C13	Capacitor, Ceramic, 1UF 16V 10% X7R 0805	TDK	C2012X7R1C105K
12	1	C14	Capacitor, Ceramic, 1UF 6.3V 10% X7R 0603	TDK	CGJ3E2X7R0J105K
13	2	C18,C22	Capacitor, Ceramic, 10UF 16V 20% X7R 1206	TDK	C3216X7R1C106M
14	3	C19,C23,C24	Not Used		
15	4	R19,R20,C21, C34	Not Used		
16	5	C25,C28,C29, C30,C31	Capacitor, Ceramic, 22UF 10V 20% X7R 1206	Taiyo Yuden	LMK316AB7226ML-TR
17	2	C32,C33	Capacitor, Ceramic, 0.1UF 16V 10% X7R 0603	TDK	C1608X7R1C104K
18	1	JB1	Header, 3 Position, Vertical Mount, 0.100 Center	3M	929647-02-36-1
19	2	L1,L2	INDUCTOR POWER 2.2UH 9A SMD	Wurth	744311220
20	2	Q1,Q2	MOSFET N-CH 30V DUAL POWER56	Fairchild	FDMS7602S
21	3	R1,R2,R10	Resistor, 1.0K, 5%, 1/10W, 0603 Case	Panasonic	ERJ-3EGYJ102V

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Item Number	Quantity	Part Reference	Description	Manufacturer	Manufacturer Part Number
22	1	R4	Resistor, 40.2K, 1%, 1/16W, 0603 Case	Panasonic	ERJ-3EKF4022V
23	1	R5	Resistor, 5.62K, 1%, 1/16W, 0603 Case	Panasonic	ERJ-3EKF5621V
24	2	R6,R15	Resistor, 21.0K, 1%, 1/16W, 0603 Case	Panasonic	ERJ-3EKF2102V
25	1	R7	Resistor, 1.2K, 5%, 1/10W, 0603 Case	Panasonic	ERJ-3EGYJ122V
26	2	R8,R16	Resistor, 20, 5%, 1/10W, 0603 Case	Panasonic	ERJ-3EGYJ200V
27	1	R9	Resistor, 10K, 5%, 1/10W, 0603 Case	Panasonic	ERJ-3EGYJ103V
28	2	R11,R17	Resistor, 2.74K, 1%, 1/16W, 0603 Case	Panasonic	ERJ-3EKF2741V
29	1	R12	Resistor, 8.2K, 5%, 1/10W, 0603 Case	Panasonic	ERJ-3EGYJ822V
30	1	R13	Resistor, 1.5K, 5%, 1/10W, 0603 Case	Panasonic	ERJ-3EGYJ152V
31	1	R14	Resistor, 3.40K, 1%, 1/16W, 0603 Case	Panasonic	ERJ-3EKF3401V
32	5	R18,R21,R22, R23,R24	Resistor, 0 Ohm, 0603 Case	Panasonic	ERJ-3EGY0R00V
33	5	TP1,TP2,TP4, TP13,TP14	Test Point, Miniature Surface Mount	Keystone	5015
34	1	U1	IC, Dual Interleaving PWM Controller	Microsemi	LX1752CLQ

Silkscreen and Test Setup

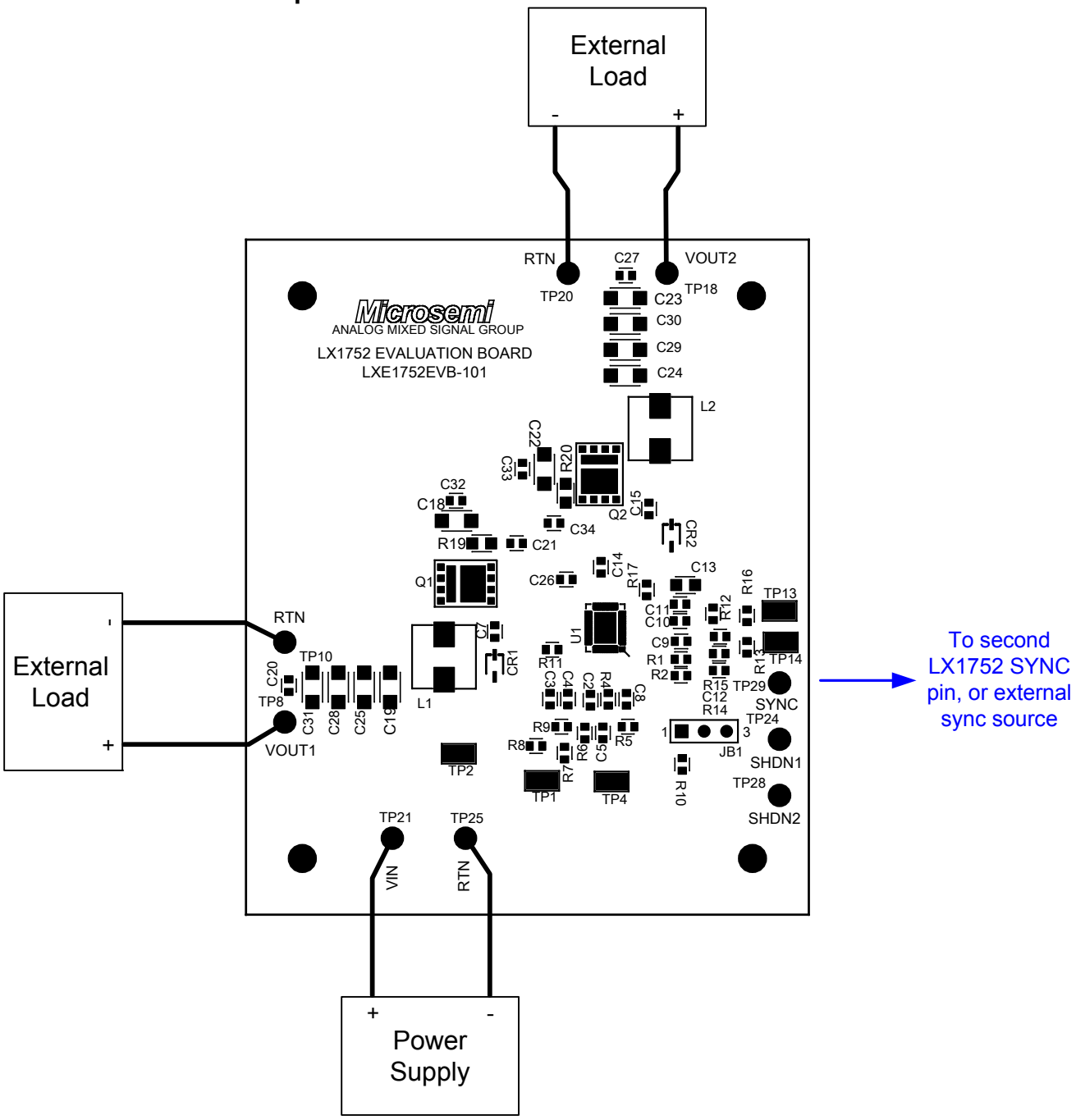

Figure 1. LX1752 Evaluation Board Test Setup

Schematic

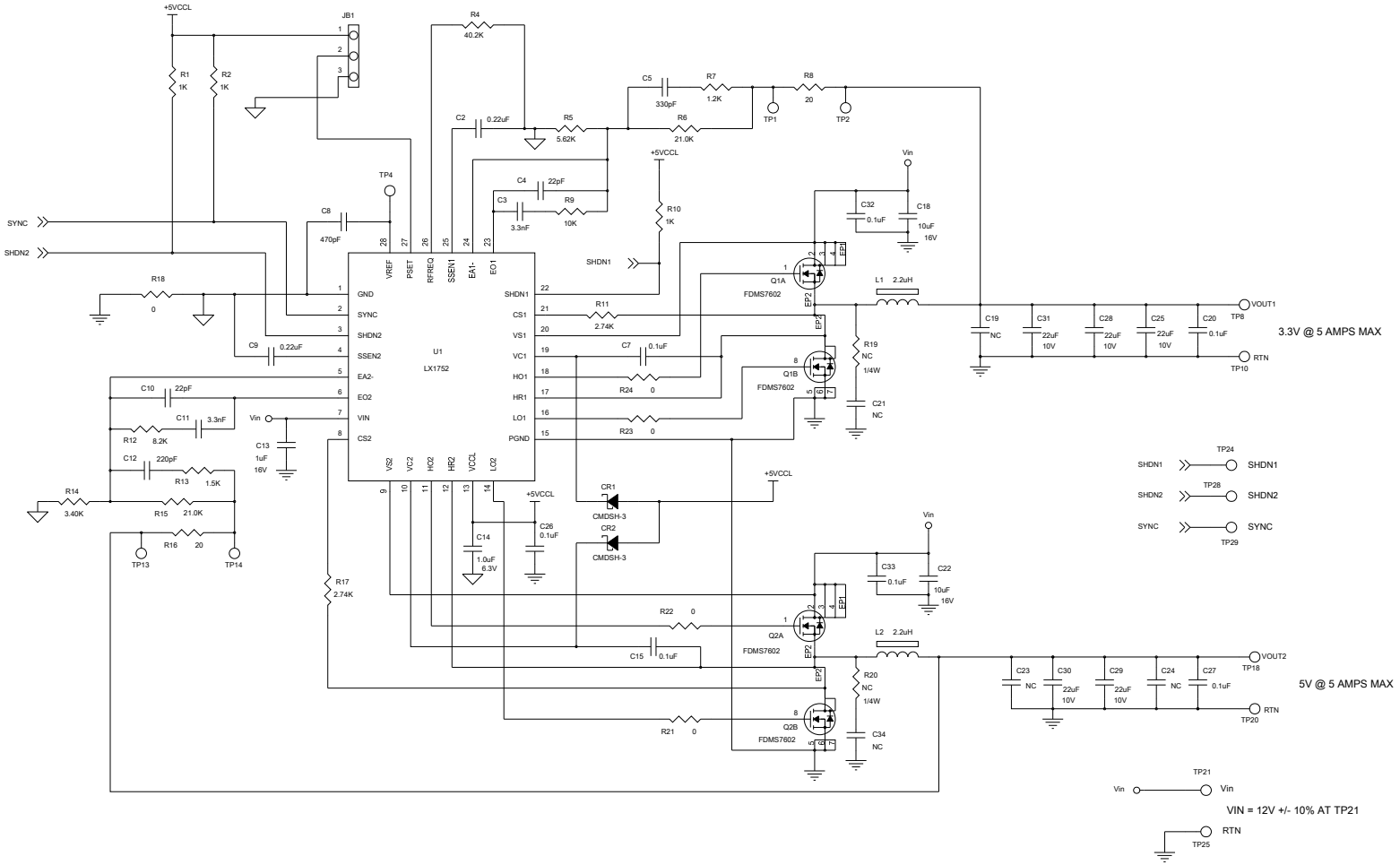

Figure 2. LX1752EVB-101 Evaluation Board Schematic

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Printed Circuit Board Layout Recommendations

Careful attention to PCB layout is necessary to insure proper operation with minimal noise generation. When laying out the PCB, these guidelines should be followed:

1) Keep the input capacitor, output capacitor, output inductor and output MOSFETs (upper and lower), close together, and tie all high current output returns directly to a suitable power ground plane.
2) Keep the high current ground return paths separate from the signal return paths. It is recommended that a separate signal ground plane be used, with a common tie point between the power ground plane and the signal ground plane established at the IC signal ground pin.
3) Place the VIN input decoupling capacitors as close to the upper and lower MOSFETs as practical. Connections between these capacitors and the Upper and Lower MOSFETs Drain and Source connections, respectively, should be as short as practical. The LX1752 internal LDO filter capacitor should be placed as close to the VCCL pin as practical.
4) PGND connection to the Source pin of the Lower MOSFET should be as short as practical, and should be established with a direct connection (using no vias) if possible.
5) VS_X Pin connections should be Kelvin connected directly at the Upper MOSFET's drain pin(s).
6) HR_X connection to the Upper MOSFET's Source pin should be as short as practical.
7) LOX and HOX should be connected to their respective MOSFET gate pins with as short a trace as practical.
8) The current sense (CS_X) resistor connection to the junction of the Upper MOSFET's Source, and the Lower MOSFET's drain should be as short as possible.
9) Place the CS_X resistor as close to the CS_X pin as possible. CSx pin is sensitive to capacitance to ground. If possible, minimize this capacitance by removing any ground plane area directly below the CSx pin pad and trace connection to the CSx resistor.
10) Place all compensation and feedback components as close to their respective error amplifier pins as practical. Keep the error amplifier input connections (EA_X-) as short as possible.
11) Place the frequency programming resistor, R_{FREQ} as close to the RFREQ and GND pins as practical.
12) For best thermal performance, the LX1752 thermal pad should be tied to signal ground, using 12 mil diameter (drill size) vias. Vias should be spaced 47mils apart in a grid array. See Figure 3 for details. Thermal vias are optional; the LX1752 will operate with reduced thermal performance without them.

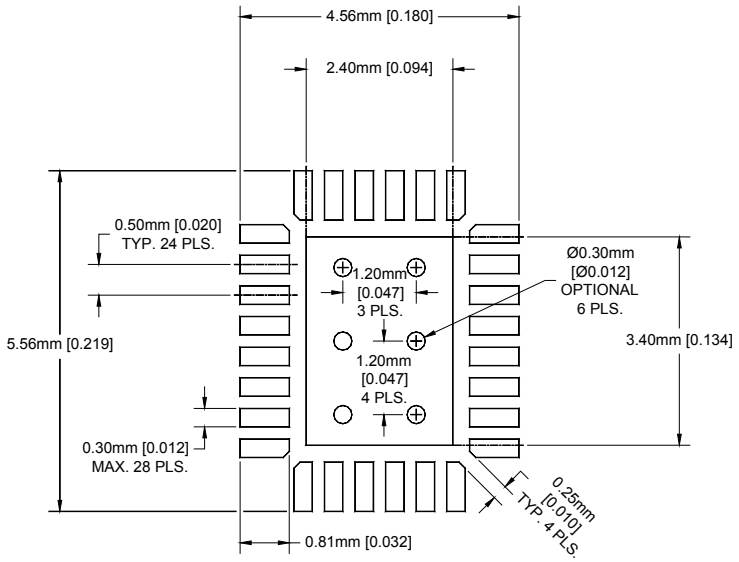
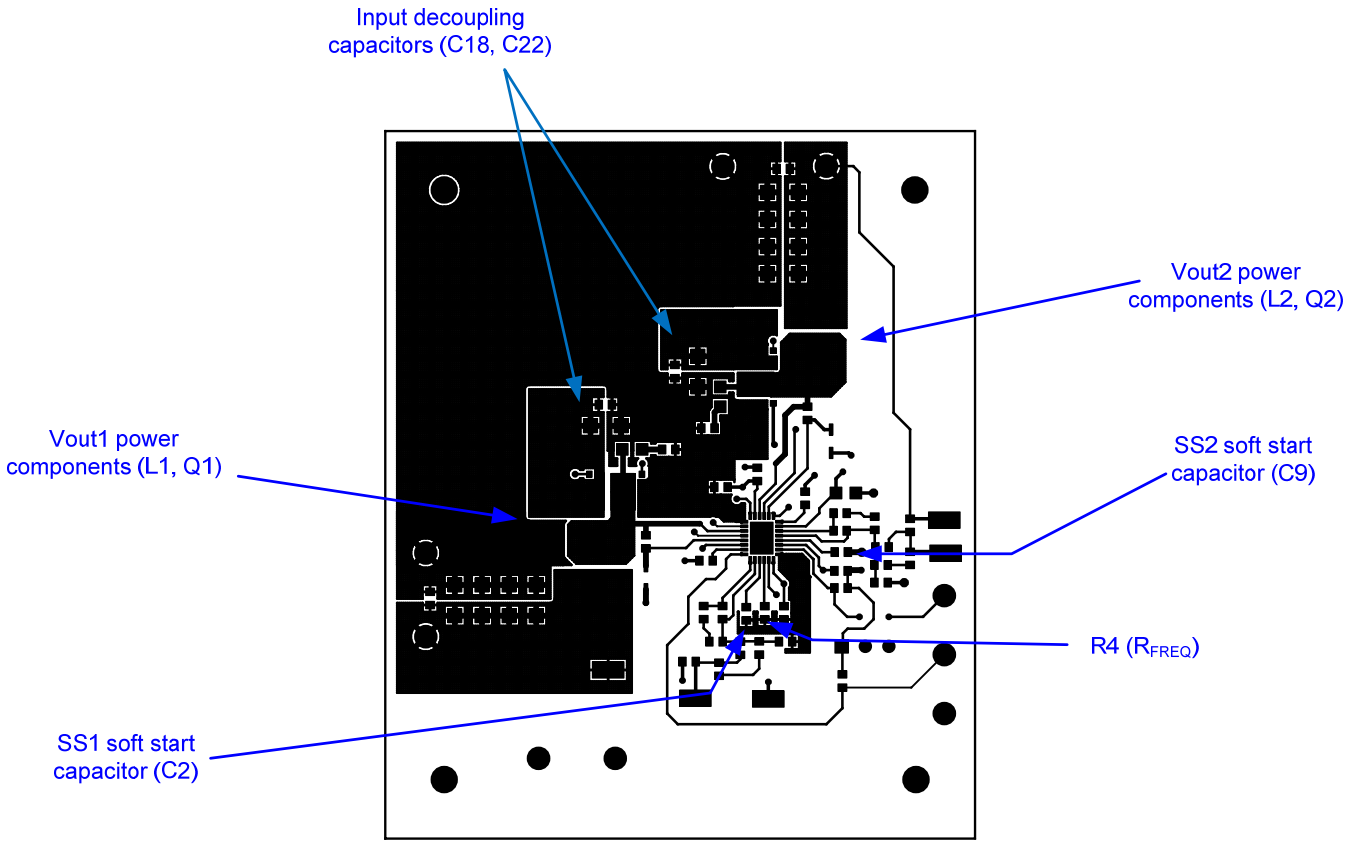


Figure 3. 4x5mm LQ package suggested PCB pad layout.

LX1752EVB-101 Evaluation Board Printed Circuit Layout

PCB LAYOUT GUIDE – TOP LAYER



External PCB dimensions (W x H): 2.5 in. X 3.0 in. (63.5mm x 76.2mm)

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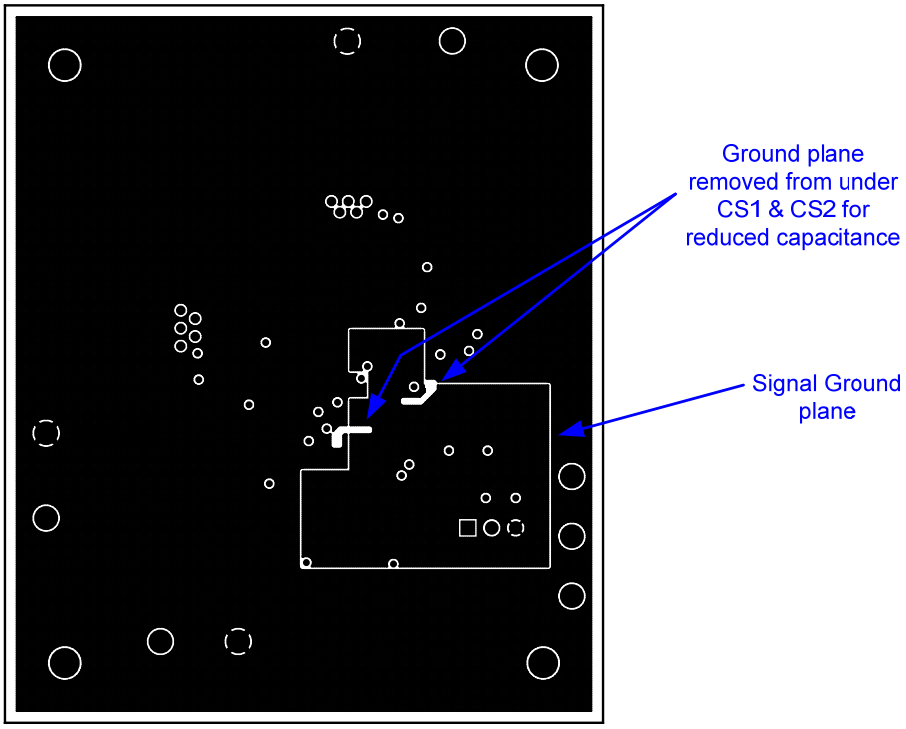
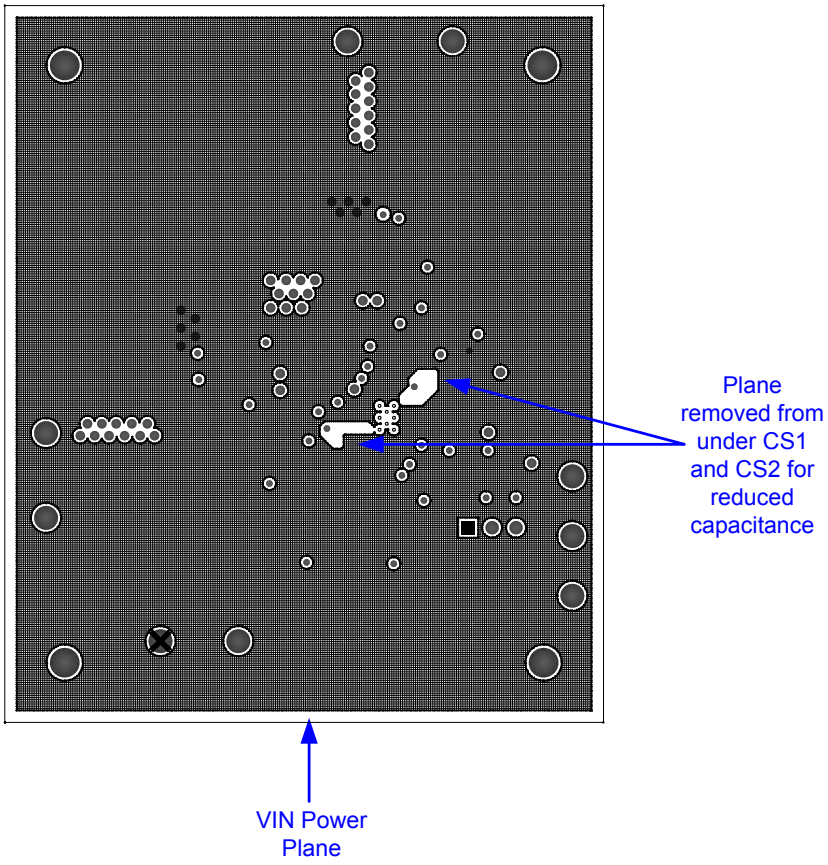
PCB LAYOUT GUIDE – INNER LAYER 1 – POWER & SIGNAL GROUND PLANE



PCB LAYOUT GUIDE – INNER LAYER 2 –V1 & V2 POWER



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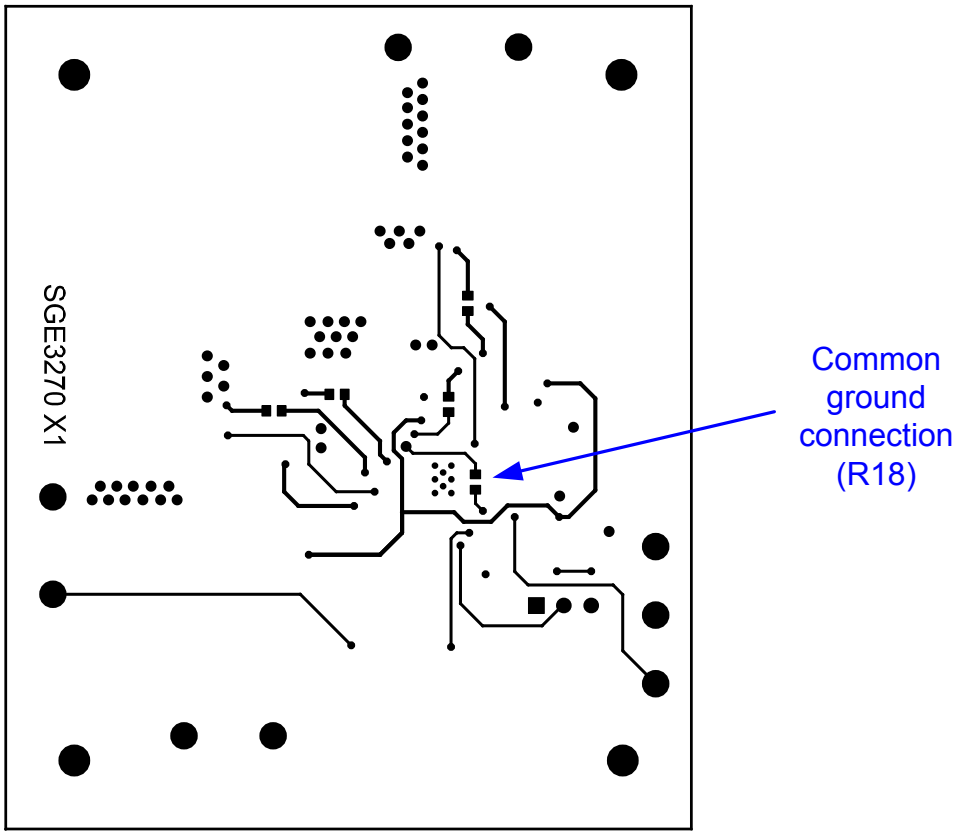
PCB LAYOUT GUIDE – BOTTOM LAYER (TOP SIDE VIEW – MIRROR IMAGE FROM BOTTOM SIDE)



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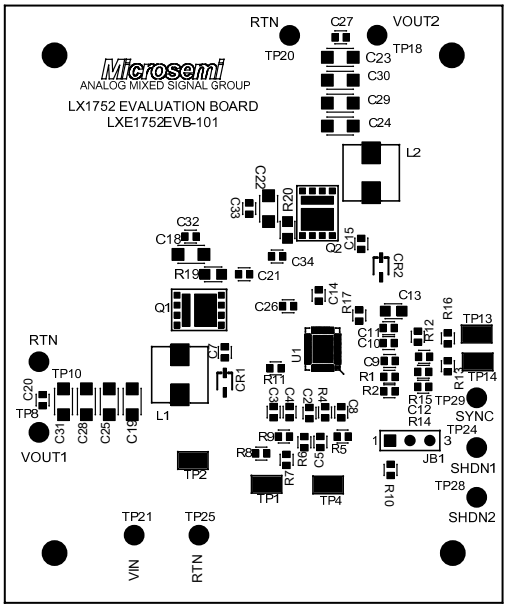
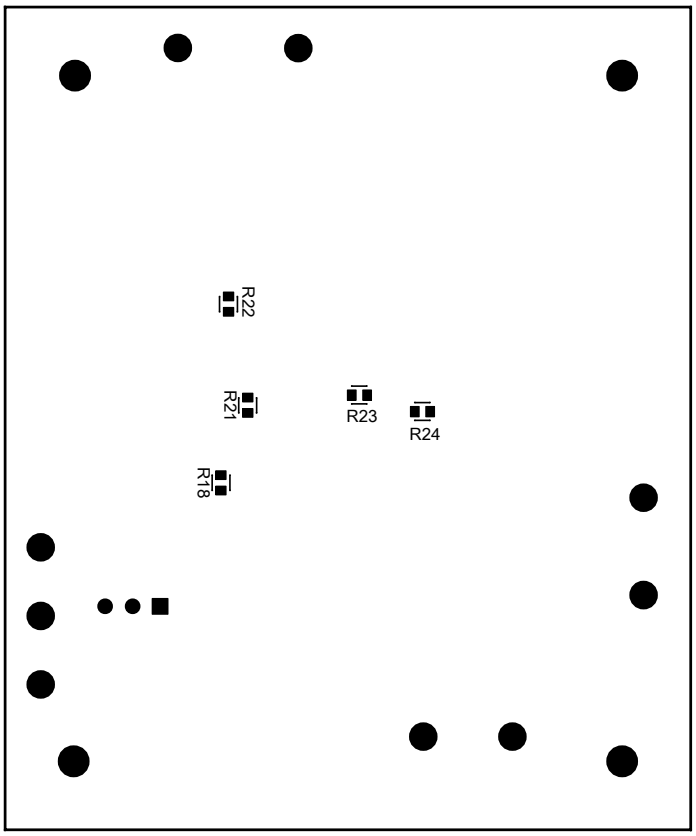
PCB LAYOUT GUIDE – TOP SILKSCREEN & SOLDER MASK



PCB LAYOUT GUIDE – BOTTOM SILKSCREEN & SOLDER MASK



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Test Hookup and Operation

The following is a demonstration scenario that can be used to evaluate the LX1752:

1) Connect a Power supply capable of 12V +/- 10%, 5 Amps output, to VIN and RTN (TP21 (+) and TP25 (-), respectively). Insure the supply is shut off before connecting.
2) Using an Oscilloscope, monitor R19, R20, and TP29. R19 and R20 are monitored at their respective connections to Q1 and Q2; these are VOUT1 and VOUT2 switch nodes, respectively; TP3 is the LX1752's sync signal. Trigger on the falling edge of the signal on TP3. Probe grounds should be through short leads to the ground side of C18 or C22.
3) Monitor VOUT1 (TP8 (+), and TP10 (-)), and VOUT2 (TP18 (+) and TP20 (-)) with a DMM.
4) Insure the position of the jumper JB1 is as follows:
    a. JB1 = jumper in position 2-3.
5) Power on the supply, and insure current is less than 100mA. Switch node waveforms on R19 and R20 should be continuous pulse waveforms with peak voltage levels approximately equal to the supply voltage.
6) SYNC signal present on TP29 should be a narrow, negative-going spike, approximately 5 Volts in amplitude. Frequency will be 800kHz +/- 5%
7) VOUT1 should measure 3.3 Volts, +/- 3%; VOUT2 should measure 5.0 Volts, +/- 3%.
8) Connect suitable loads to VOUT1 and VOUT2: TP8 (+) and TP10 (-) for VOUT1; TP18 (+) and TP20 (-) for VOUT2. Loads may be resistive or electronic loads. Loads should be able to handle at least 15 Watts (VOUT1), and 25 Watts (VOUT2). If using a resistive load, 0.66 Ohms 15 Watts (or higher) on VOUT1, and 1 Ohm 25 Watts (or higher) on VOUT 2 will load the outputs to their full rated capacity (assumes standard configuration with 3.3V and 5.0V output on VOUT1 and VOUT2, respectively).
9) Check short circuit limit: momentarily short VOUT1 with a small, heavy gauge wire. Average input power supply current will reduce significantly, and will cycle up/down in magnitude. Verify VOUT1 switch node signal at TP7 changes from a continuous pulse stream to a pulse stream that cycles on/off, with the on period approximately 4% of the overall on/off cycle. The on time for VOUT1 will be approximately 9.5 ms with the installed 0.22uF capacitor (C2). Verify that VOUT2 is unaffected and is still regulating. Remove the short across VOUT1
10) Momentarily short VOUT2 with a small, heavy gauge wire. Average input power supply current will reduce significantly, and will cycle up/down in magnitude. Verify VOUT2 switch node signal at TP17 changes from a continuous pulse stream to a pulse stream that cycles on/off, with the on period approximately 4% of the overall on/off cycle. The on time for VOUT2 will be approximately 9.5ms with the installed 0.22uF capacitor (C9). Verify that VOUT1 is unaffected and is still regulating. Remove the short across VOUT2
11) For 4 output interleaving, synchronize two LX1752 Evaluation Boards by connecting a wire between both evaluation board's SYNC signal test points (TP29). Place jumper JB1 on one of the evaluation boards in position 2-3, and leave jumper JB1 on the other board open. Monitoring R19 and R20 on both boards, verify that the switch node outputs are interleaved at approximate 90° intervals.