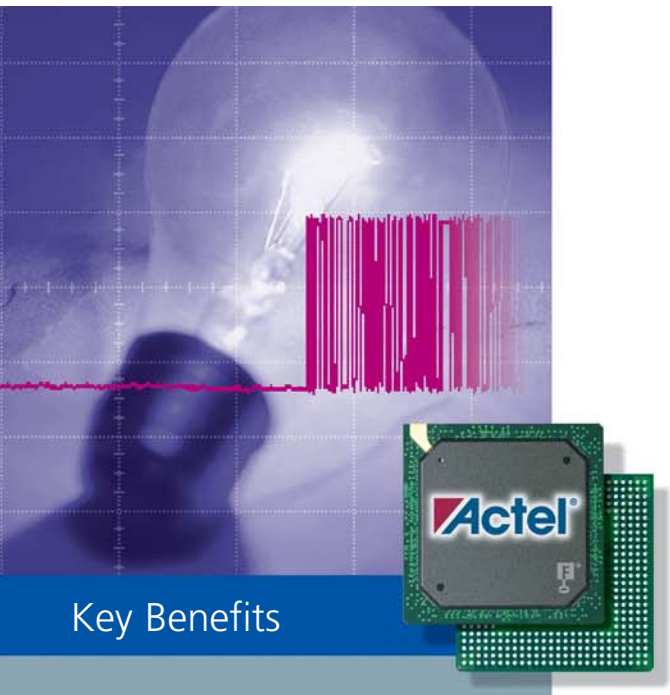
Actel
POWER MATTERS

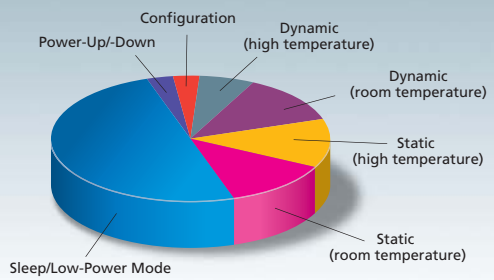


Total System Power

EVALUATING THE POWER PROFILE OF FPGAs

Key Benefits

- Lowest Power In-System Programmable FPGAs Starting at $0.49
- Flash*Freeze Technology Enables Ultra-Low Power Consumption (from 2 µW) while Maintaining FPGA Content
- 16X Better Power per I/O Ratio with IGLOO® PLUS FPGAs
- ARM®-Enabled and Fusion Devices Allow System Power Management by Controlling and Monitoring Supplies
- Low Core and I/O Voltage (1.2 V) Minimizes Static and Dynamic Power Consumption
- Small-Footprint (as small as 3x3 mm) and Low-Profile Packages for Portable Applications
- No Inrush Current Spikes at Power-Up or Configuration
- Power Optimization Tools Can Help Achieve Up to 30 Percent Power Savings



Example of System Power (over time)

Although often promoted as ASIC alternatives, not all FPGA technologies provide the complete feature set offered by an ASIC. Only nonvolatile flash and antifuse FPGAs have power characteristics similar to those of an ASIC. When selecting FPGAs, design engineers neglect to take the entire power profile of the programmable logic solution into account. The various FPGA core technologies have significantly different power profiles, and these differences can have a profound impact on the overall system design and power budget.

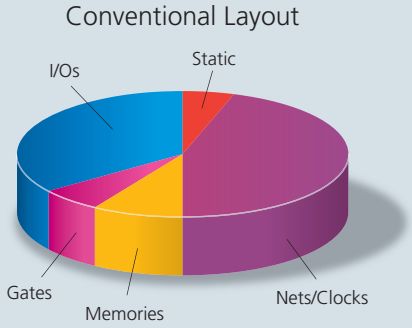
The Power Profile

The power profile of an FPGA is determined by the base technology of the interconnect element used. Nonvolatile, reprogrammable flash FPGAs use a single flash cell to form their efficient interconnect. SRAM FPGAs utilize a six-transistor SRAM cell to perform the interconnection between routing lines and logic cells, resulting in higher static and dynamic power.

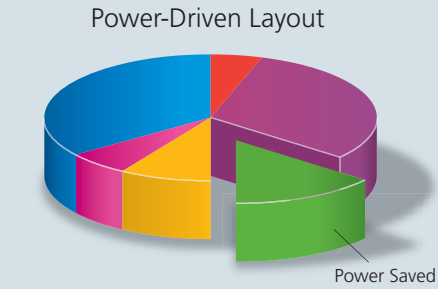
When evaluating the respective programmable technologies, there are five components to the FPGA power profile that must be considered: inrush current, configuration current, static power, dynamic power, and power during sleep/low-power mode. Unlike SRAM FPGAs, flash and antifuse FPGAs have no power-up or configuration power components. They offer lower static and dynamic power consumption over a large temperature range and support low-power modes that allow further minimization of power consumption when the system is idle.

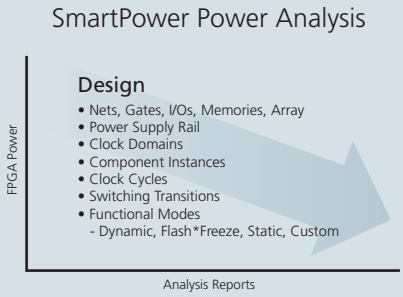
To analyze total system power consumption, designers should calculate the percentage of time the system spends in power-up or -down, static or dynamic mode, and sleep/low-power mode. Designers must also consider temperature variation, as power consumption rises significantly when temperature increases. Additionally, Actel Fusion® and ARM-enabled Fusion devices allow for complex system power management through controlling and monitoring power supplies.

Typical IGLOO Power Distribution



Addressing Power Consumption





Design Software

Libero® Integrated Design Environment (IDE) is Actel's comprehensive software toolset for designing with all Actel FPGAs. Libero IDE performs design entry, synthesis, and simulation through floorplanning, place-and-route, timing constraints and analysis, power analysis, and program file generation. Libero IDE easily manages the entire design flow and ensures maximum device performance and resource utilization.

Power Optimization with Libero IDE

While Actel FPGAs inherently use less power than competing SRAM-based technologies, the power consumption of your Actel flash design can be reduced significantly by using the wide array of features in the Libero IDE tool suite.

Power-Driven Layout

Libero IDE offers a power-sensitive layout process that automatically reduces the power consumption of a design as part of the place-and-route process. By using a simulation Value Change Dump (VCD) file or initialization from SmartPower, the dynamic power of Fusion, IGLOO (IGLOO, IGLOO PLUS, IGLOOe), and ProASIC®3 (ProASIC3, ProASIC3L, ProASIC3E) designs can be reduced up to 30 percent with little to no impact on timing performance.

SmartPower Analysis

Today's portable electronics typically do not spend 100 percent of their "on" time in a fully powered-up mode. "On" time is a combination of active and semi-active modes, such as static, sleep, power-up, power-down, and Flash*Freeze for ProASIC3L and IGLOO designs. In addition to SmartPower's traditional analysis of nets, gates, I/Os, clock domains, memories, supply rail, component instances, and modes, SmartPower analyzes the power based on the total power consumption of the design measured over time. SmartPower allows you to create a power profile for a design. The profile can be a combination of dynamic, static, Flash*Freeze, and custom modes. The total power is reported based on the weighted average of the power consumption of all modes. Consequently, a more realistic report of power is provided.

Battery Life

The mode and profile analysis feature is taken to the next level with the addition of a battery life estimator. Simply enter the proposed battery capacity and SmartPower reports the estimated battery life based on the mode or combination of modes in the power profile. Battery choices and power profiles can be created to test different configurations in order to create an optimal design.

Libero Options

Libero IDE is available for Microsoft® Windows® and RedHat® Linux operating systems, and has a number of license options including free licenses.

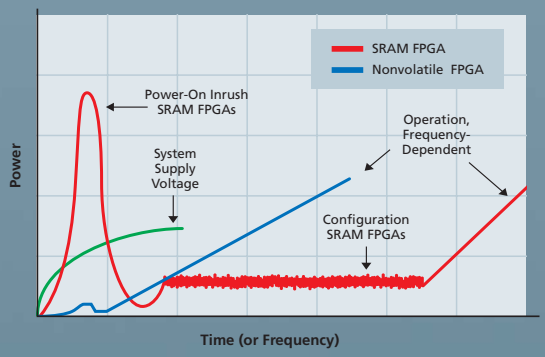
Actel FPGA Power Profiles

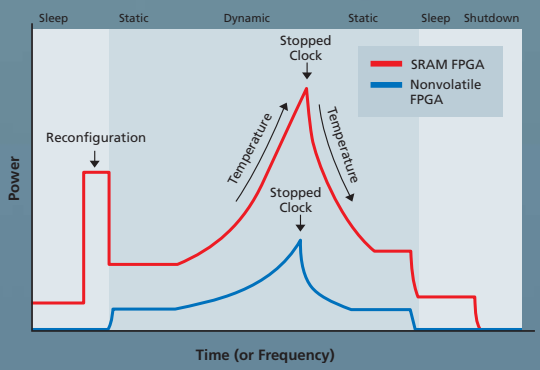
The power profiles of both Actel's nonvolatile (flash and antifuse) FPGAs more closely resemble those of ASICs and ASSPs than SRAM FPGAs. The power profile for these device types is composed of only three significant components: static, dynamic, and sleep/low-power mode power.

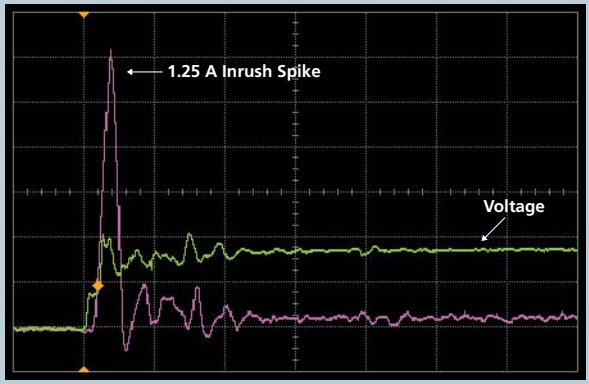
Flash and antifuse FPGAs are live at power-up. They retain their programming information once they have been configured, even after power-down. As a result, there is no configuration cycle during power-up.

True flash FPGAs are the lowest-power full-featured FPGAs on the market, with the lowest static and dynamic power, and no inrush or configuration power.

Single-chip solutions are ideal for portable applications, with the smallest form factor, Level 0 live at power-up, and no power consumed by external devices.





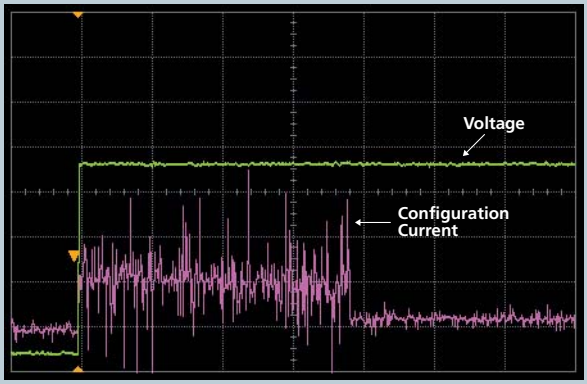


Actual SRAM FPGA Inrush Current

Inrush Current

SRAM or "hybrid" SRAM FPGAs typically power up in an unconfigured state. Until the device completes the initial power-up and reset sequence, the various configuration bits are in unknown states. As these bits are initialized each time power is cycled, a current surge is created that may generate a spike as high as several amperes. This event may also last as long as a few hundred microseconds—all during the time the power supply is ramping up and the rest of the system is attempting to power up.

To mitigate this current spike, many SRAM FPGAs have added complex power sequencing requirements to the system. This results in added design complexity and cost. Actel FPGAs do not exhibit an inrush current spike due to their flash and antifuse technology advantages.



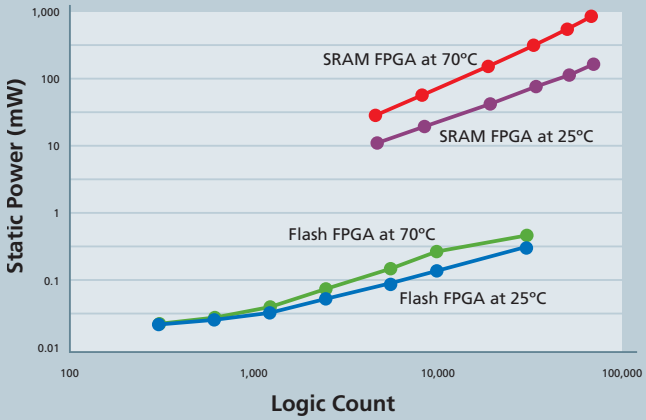
Actual SRAM FPGA Configuration Current

Configuration Current

After an SRAM or "hybrid" SRAM FPGA has completed its initial power-up and reset, it must also be configured. During configuration, a bitstream is downloaded to the device and the various configuration bits are programmed. This configuration programming can often consume hundreds of milliamps and last for hundreds of milliseconds.

The configuration current can prove especially lethal to battery-based supplies, where constant loads are desirable to maximize battery life. This operating characteristic of SRAM FPGAs generally makes them poorly suited for portable applications where battery life is a concern.

Flash and antifuse FPGAs are live at power-up. They retain their programming information once they have been configured, even after power-down. As a result, there is no configuration cycle during power-up.



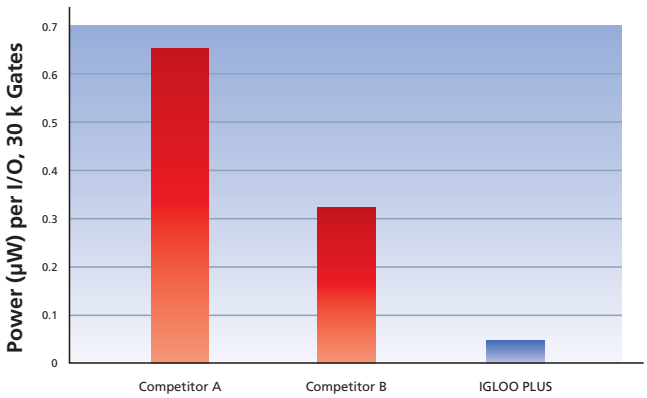
Comparison of Static Current at Room and High Temperature between Flash and SRAM FPGAs

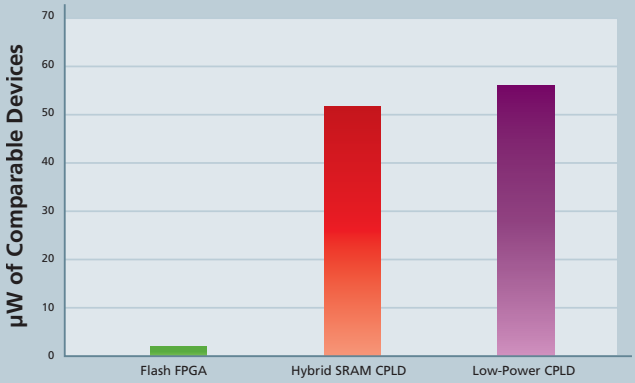
Static Power

Static power is the minimum power required to maintain a device in user mode while the I/Os and logic cells are not switching. SRAM FPGAs consume significantly more static power than do their flash and antifuse counterparts. At room temperature, this difference may be tens of milliamps; at higher operating temperatures, the difference can exceed hundreds of milliamps. This higher current draw drastically impacts the operating life of any battery-supplied system.

The Actel IGLOO device allows for ultra-low power consumption while the IGLOO device is completely functional in the system by maintaining I/Os, SRAM, registers, and logic functions. This enables the IGLOO device to control the system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Actel's IGLOO PLUS I/O–optimized FPGAs offer up to 64 percent more I/Os than IGLOO FPGAs and are best suited for I/O–intensive designs. IGLOO PLUS FPGAs consume 16X less static power per I/O compared to their nearest competitor.





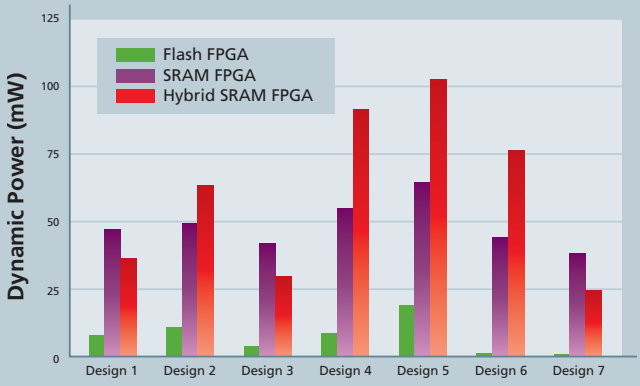
Comparison of Sleep/Low-Power Mode Power between Low-Power FPGAs/PLDs (µW of comparable devices)

Sleep/Low-Power Mode Power

To further reduce power consumption in the system, especially when idle, a few PLD vendors have implemented low-power modes that can lower static power to below 1 mA. SRAM FPGAs lose their configuration and data while in sleep mode and therefore require reconfiguration, which takes hundreds of milliseconds and consumes configuration power. Flash FPGAs offer low-power modes that can be controlled using internal or external signals, and can be put to sleep and woken up after a predefined time.

Fusion and ARM-enabled Fusion devices allow system power management by controlling and monitoring supplies.

Flash*Freeze technology used in Actel IGLOO and ProASIC3L devices enables easy entry to and exit from ultra-low-power mode, which consumes as little as 2 µW while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level.



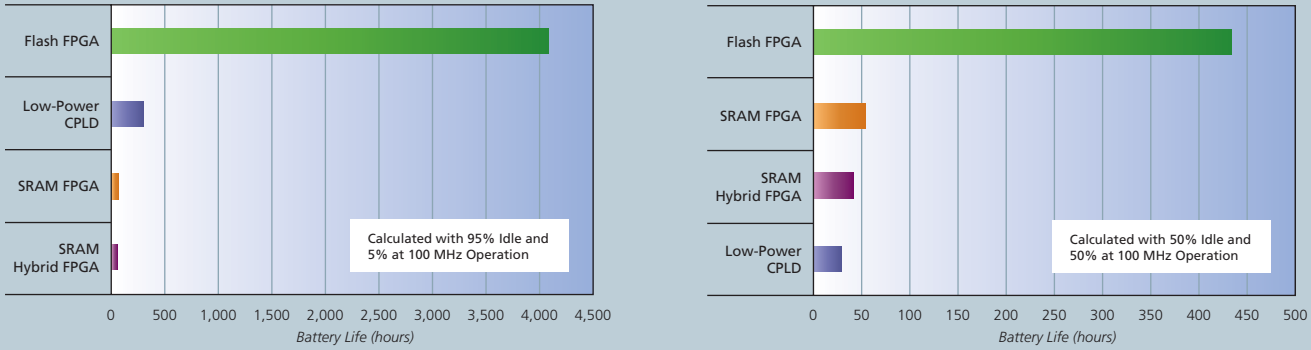
Comparison of Dynamic Power between Flash and Competing SRAM FPGAs

Dynamic Power

Dynamic power is the power consumed when both the I/Os and the logic cells are switching, and is a function of capacitance, operating voltage, and switching frequency. If we look at the dynamic power contribution alone, all advanced FPGA technologies exhibit similar performance; however, the dynamic power also contains the static power consumption component. SRAM FPGAs consume more power under static conditions and at high temperatures than flash and antifuse FPGAs; therefore, the overall dynamic power consumed by SRAM FPGAs is significantly higher.

Actel IGLOO and ProASIC3L low-power FPGAs operate from a 1.2 V core, and consume 30 percent less static power and over 50 percent less dynamic power than 1.8 V “low-power” PLD alternatives.

Dynamic power optimization is possible using a push-button Power-Driven Layout, part of Actel Libero IDE. The ability to place the device in or out of Flash*Freeze mode can reduce dynamic power when the FPGA is not switching, even for a short time.



Battery Life per Device, Based on Vendor Software Power Analysis Tool

Total System Power

Unlike flash and antifuse FPGAs, SRAM FPGAs are not single-chip. They require additional support devices to function properly. In addition to the on-board memory devices needed to store the configuration bitstreams, a CPLD is frequently needed to act as a configuration controller. Additional circuitry is often required to trap brownouts and power glitches to properly reset and reconfigure the FPGA. Aside from the added board space and cost of these components, each adds to the overall power profile of the SRAM FPGA solution and makes system power-up more complex.

Additionally, Fusion devices allow for cost-effective system power management by controlling and monitoring power supplies for total system power considerations at the board level.

All FPGA solutions from Actel are single-chip and do not require any external components to operate. This aspect not only leads to reduced power consumption but also to a smaller overall footprint.

Actel low-power FPGAs lead the industry with lowest static and dynamic power, best power per I/O, selection of power modes, and small-form-factor packages for reduced manufacturing.

Actel IGLOO devices can provide ten times the battery life of their nearest low-power competitor. This is due to the overall power profile and lower power consumption in all five stages of system operation.

Summary

FPGA technologies differ widely in their power consumption characteristics. Both flash and antifuse FPGAs are true live-at-power-up technologies that do not exhibit large inrush current spikes at power-up. Moreover, because Actel FPGA technologies are nonvolatile, they do not suffer from the high configuration current needed during each power cycle.

The nature of the SRAM FPGA power profile can force system designers to unnecessarily oversize system power supplies and complicate the overall design. Actel FPGAs exhibit a power profile similar to that of ASICs and ASSPs, greatly reducing the demand on power supplies and simplifying the designer's task.

Flash technology provides the right mix of features to answer the low-power market need: low power consumption in all modes, availability of ultra-low-power sleep modes and Flash*Freeze technology, reprogrammability to allow easy prototype and field upgrades, a true single-chip solution, high system integration, superior design security protection, small form factor packages, I/O–optimized FPGAs, and the lowest total system cost.

For more information regarding the **Power Profile of Actel FPGAs**, please contact your local **Actel** sales representative.

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