Actel
POWER MATTERS

Power Top Ten

TEN POINTS YOU SHOULD CONSIDER TO MANAGE AND MINIMIZE POWER CONSUMPTION

More and more systems need lower power semiconductors to meet their power requirements. In the last decade, there has been growth in consumer, industrial, medical, and military battery-operated and handheld applications. This growth, when combined with time-to-market pressures and increasing complexity, makes programmable logic a suitable fit if the programmable logic device can meet the power specifications. Additionally, new mixed-signal FPGAs allow for complex system power management by controlling and monitoring supplies.

Low-power programmable logic enables designers to meet the growing power demands. Flash-based, nonvolatile FPGAs provide ideal support for low-power, portable applications. This is demonstrated on several levels by their low-power profile (the lowest available), Flash*Freeze technology, single-chip solution, small-footprint packaging, reprogrammability, the lowest available system cost and their ability to manage and control power supplies across the board.

Low-power flash FPGAs are the preferred choice as ASIC alternatives in battery-operated applications. ASIC technology is increasingly too expensive, too risky, and slows down the development cycle. With ever-changing end-product features, consumer demands, and a competitive landscape, ASIC limitations prohibit their use in many of these applications.

Not all programmable logic is well suited to address the needs of low-power battery-operated or portable applications. The FPGA design world is facing the challenge that 90 nm and 65 nm SRAM technologies are diverging from market power requirements due to ever-increasing static power specifications. Additionally, to control and manage board-level power, high voltage and analog combined with programmable logic in a mixed-signal, programmable system chip is required.

Quick Tips

- **Use Low-Power FPGAs Optimized for Battery-Operated and Portable Electronics**
- **Use Low-Power Mode Technologies that Enable Dramatic Power Reduction While Retaining FPGA Content**
- **Find FPGAs that Consume Low Power in Static and Dynamic Modes**
- **Target Single-Chip Solutions that Eliminate the Need for Additional Components**
- **Choose FPGAs that Manage System Power Efficiently**
- **Optimize Total System Power Using Low-Power, Single-Chip, Small Footprint FPGAs with Portable-Friendly Power Profiles**
- **Create Power Islands and Manage Power Across the Design in Real-Time Using a Mixed-Signal FPGA**

Ten Ways to Lower Your System Power Consumption

1 Select an FPGA with an ASIC-Like Power Profile

No inrush power, no boot-up configuration power, ultra-low static power (especially over extended temperature ranges), and low dynamic power. Low-power and secure in-system programmability allow secure design modifications and field upgrades.

2 Look for Single-Chip, Small Form Factor (Portable-Friendly) FPGAs

ASIC-like form factor—smallest footprint available for an FPGA solution. No configuration PROM, brownout detection, clock management, or supply sequencing chips required, minimizing system power consumption.

3 Look for Low Power Even at Million Gate Densities and at High Temperature

SRAM FPGAs are power-hungry in static and dynamic modes and at high temperature operation. Use flash FPGAs, which offer orders-of-magnitude lower power in static and dynamic modes, across temperatures.

4 Extend Battery Life with Low-Power Modes or Wide Range Support

The availability of low-power modes further reduces total system power when the system is idle. Easy-to-use modes in low-power flash FPGAs can reduce current consumption to as low as 2 µW in Flash*Freeze mode. Wide range (1.2 V to 1.5 V) support on the core voltage helps designers build boards that utilize a battery decay model.

5 Use FPGA Capable of Managing System Power

Low-power, mixed-signal FPGAs and ARM®-enabled flash FPGAs enable system power management and power islands by monitoring and controlling power consumption of the battery and other components in the system to achieve system power efficiency.

6 Optimize for Dynamic Power

Look for vendors that support software tool optimization for low power layout. Use FPGAs that offer reduced core voltage and can instantly be switched in and out of low power modes.

7 Use Flash Memory Save and Restore Capabilities

FPGA on-board user flash memory can enable power-down and power-off modes of operation.

8 Use Level 0 Live-at-Power-Up (LAPU) Nonvolatile FPGAs

Nonvolatile FPGAs simplify low-power system design. Level 0 LAPU FPGAs quickly power up and restore the system state from sleep mode without the need to reload the configuration. Entering and exiting Flash*Freeze mode is done quickly and easily, which helps reduce power consumption and increase usability. Refer to the Actel LAPU Resource Center located at http://www.actel.com/products/solutions/lapu/default.aspx.

9 Reduce Total System Power Using Devices with Higher System Integration

Look for programmable logic that integrates power FET control and supports simplified sleep and static power modes as low as 2 µW. Additional integration of clocking resources, voltage regulator, and analog-to-digital converter removes parts from the board and reduces total current consumption.

10 Utilize Enable Flip-Flops and Regional Clock Resources

Limit dynamic power consumption in the design utilizing FPGA power-friendly architectures that allow the use of segmented clocks and enable flip-flops. Also use low-power, high-performance serial connections such as LVDS with DDR registers to minimize I/O power consumption.

For more information regarding the **Power Consumption of Actel FPGAs**, please contact your local **Actel** sales representative.

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