DC Input Boost Converters with IPS401
(Boost – Tapped Boost – Flyback Topologies for LED Control Solutions)

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July 11, 2007

Introduction

This is a collection of information to assist in understanding the design of LED driver circuits using the IPS401 in a class of variable frequency DC input converters.

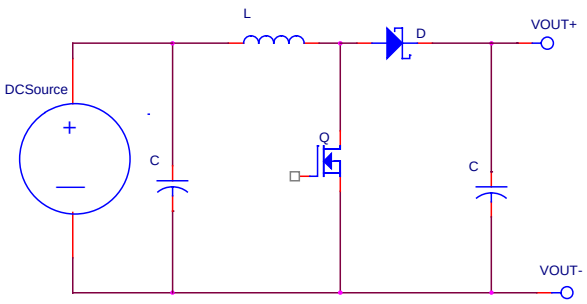
Topology choices

There is a very wide array of power conversion topologies, each with its unique aspects. Most designs use pulse width modulation of the power switch duty cycle to vary the power supply performance to adapt to varying input voltage or output load. The terminology describing these converters subdivides them into discontinuous, critical, and continuous current mode converters. This discussion will be about topologies that use a variable operating frequency, with continuous current conduction provided by the IPS401. The defining aspect of these converters is that the current variation is a fixed amount, specifically, with a two-to-one ratio. The most basic implementation is a non-isolated boost converter.

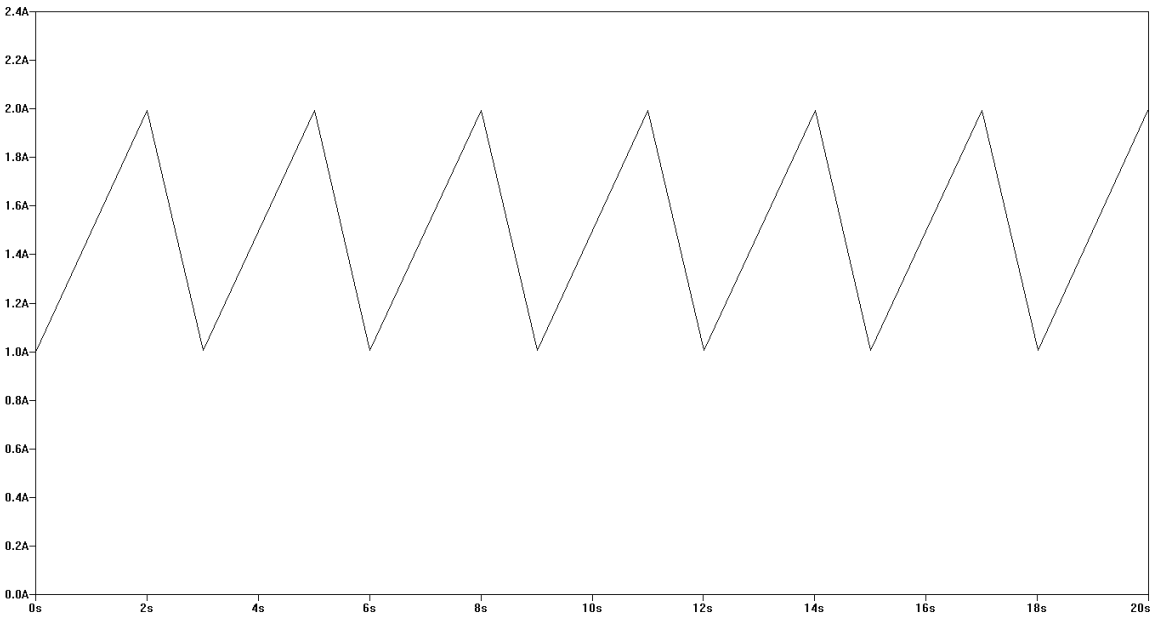
Alternatives to the boost are the tapped-boost and the flyback. Each of these alternatives uses a two winding transformer in place of the boost inductor. The applications targeted are still non-isolated, and the solution still results in varying both the frequency and duty cycle. The turns ratio of the transformer allows for a wider range of output voltages with the duty cycle 'centered' more towards 50%.

Boost Topology

A boost converter (shown below) creates an output voltage greater than the input voltage.
In the proposed scheme, the FET switching is controlled such that the current through the inductor is continuous, and the current at the beginning of the on-state is half the current at the end of the on-state. It can also be described as: the current at the beginning of the off-state is twice the current at the end of the off-state.



A typical plot of the inductor current versus time would look like:



Note that the bottom of the plot is zero amps, with the sawtooth going between one and two amps.

Boost equations

Let I1 be the inductor current at the beginning of the on-time (the valley) and I2 is the current at the end of the on-time (the peak).

From the definition of this control scheme: I2 = 2*I1

The power being converted is the energy-per-cycle times the cycles-per-second. The energy in an inductor is $E = 0.5*L*I^2$. The power is therefore

$P = [0.5*L*I2^2 - 0.5*L*I1^2]*f. = 0.5*L*(I2^2 - I1^2)*f = 0.5*L*([4*I1^2 - I1^2)*f$

$= 1.5*L*I1^2 * f$

The change in current during the on-time is I2-I1 = I1, the voltage across the inductor during the on-time is Vin, so the on-time is Ton = $\frac{L*I1}{Vin}$.

The change in current during the off-time is I1 as well, the voltage across the inductor during the off-time is (Vout – Vin), so the off-time is Toff = $\frac{L*I1}{Vout-Vin}$.

The operating frequency is $f = \frac{1}{T} = \frac{1}{Ton+Toff} = \frac{1}{\frac{L*I1}{Vin}+\frac{L*I1}{Vout-Vin}} =$

$$\frac{Vin*(Vout-Vin)}{L*I1*(Vout-Vin)+L*I1*Vin} = \frac{Vin*(Vout-Vin)}{L*I1*Vout}$$

The duty cycle is D = $\frac{Ton}{T}$ = Ton * f = $\frac{L*I1}{Vin} * \frac{Vin*(Vout-Vin)}{L*I1*Vout} = \frac{Vout-Vin}{Vout}$

The voltage transfer ratio is derived from applying volt-seconds balance to the inductor.

Vin * D = (Vout – Vin)*(1-D) = (1-D)*Vout - Vin + D*Vin
1 = (1-D)*Vout – Vin
Vin = (1-D)*Vout
M = $\frac{Vout}{Vin} = \frac{1}{1-D}$ A plot of this equation is shown below as part of the tapped boost.

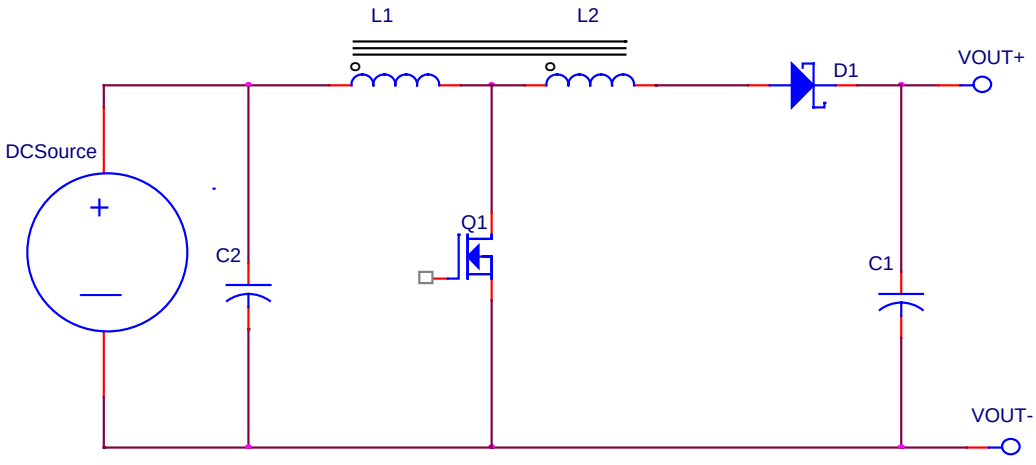
Boost discussion

The boost is the simplest of the topologies discussed here. The input current is continuous (hence the name 'continuous conduction mode"), and the output current is discontinuous. The output voltage has to be equal to or greater than the input voltage. The FET and diode both experience a peak voltage of the output voltage, and both see the same peak current. This can necessitate an expensive FET/diode pair in the cases where there is a high amount of boost. For example: if the application is for 450 volts output and 12 volts input, the average input current (and hence the peak input current) will be large because of the comparatively low input voltage, and both the FET and diode need to be rated for 450 volts, even though the input voltage is only 12 volts. The duty cycle here would be D = (450-12)/450 = 438/450 = 97.3%. Limitations in the speed of the FET drive will limit the maximum frequency because the off-time will be so short.

Tapped Boost Topology

Adding an extra winding to the boost inductor allows the on-time and off-time inductances to be selected independently. This can also be viewed as adding a turns-ratio to the design. It will still act as a boost, and it is still not isolated. During the off-time the input current still flows directly to the output. This last comment is what distinguishes this from a flyback. This means that the 'primary' winding gets better utilization than in a flyback. The component stresses are changed from the simple boost, some to advantage and some not.

Basic topology



The inductance of L2 is typically greater than that of L1, and they are on one magnetic core with the dot polarity as shown. During the switch on-time, energy is stored in inductance L1. There is no current in L2 because the diode is reverse biased (by a voltage greater than the output voltage because the voltage on L2 is equal the voltage on L1 times the turns ratio). During the off-time, when the FET is an open-circuit, the total inductance of L1 and L2 transfers the stored energy to the output.

It is important to remember that inductance is proportional to the square of the number of turns. So, for example, if the turns-ratio is 10 (number of L2 turns is ten times that of L1), the inductance of L2 is 100 times that of L1. And also remember that the total inductance of L1 and L2 during the off-time, as shown, is NOT just L1+L2, because there is coupling between them and the aforementioned square-law relation. So, using this same 10x turns ratio example, the effective total inductance seen during the off-time is 11 x 11 = 121 (one plus the turns ratio squared) times the inductance of L1.

Tapped boost equations

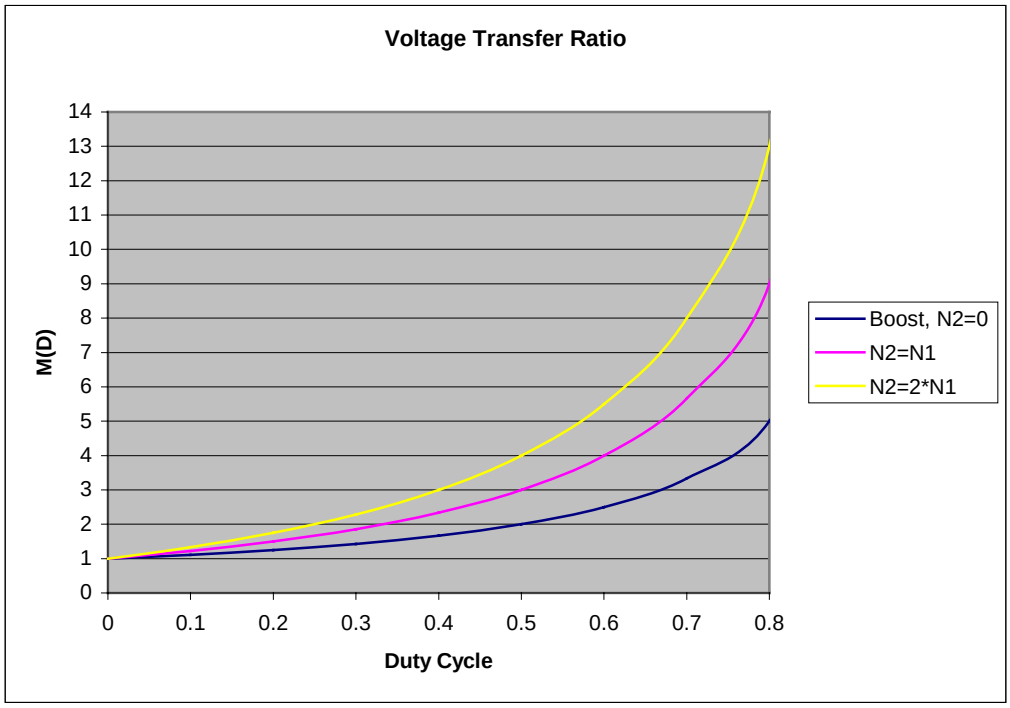
The basic input-output voltage relation is derived from inductor volt-seconds balance, as previously done for the boost. Here, the equation for volt-seconds is balanced across the L1 winding. N1 is the number of L1 turns, and N2 is the number of L2 turns.

Vin * D = (Vout – Vin)*(1-D)* $\frac{N1}{N1+N2}$, solving for Vout, and then for $\frac{Vout}{Vin}$

$$\frac{Vout*(1-D)*N1}{N1+N2} = \text{Vin*D} + \frac{(1-D)*Vin*N1}{N1+N2}$$

$$\text{M} = \frac{Vout}{Vin} = \frac{D+\frac{(1-D)*N1}{N1+N2}}{\frac{(1-D)*N1}{N1+N2}} = \frac{1}{1-D} * \left[\frac{D*(N1+N2)}{N1}+(1-D)\right] = \frac{1+\frac{N2*D}{N1}}{1-D}$$

If N2=0, then you have a conventional boost, and the voltage ratio reverts to that of the boost. So, it can be said that the tapped boost changes the output voltage by a factor of $\left(1+\frac{N2*D}{N1}\right)$. Some examples of this voltage ratio are shown below.



For analyzing the currents, the designer must remember that because the on-time and off-time inductances are different, the input current is continuous, but it changes amplitude abruptly whenever the FET switches. It goes through a jump downwards when the FET turns off, and likewise a jump upwards when the FET turns on. From the definition of this control scheme, the maximum input current is twice the minimum input current. Also, the peak output current is twice the output current at the end of the off-time. Since designs typically are done off of output specifications, the below calculation will start with the output current. The average output current is the time average of the off-state current, or:

Iout,max = 2*Iout,min

$$\text{Iout,ave} = (1\text{-D}) * \frac{Iout,\max + Iout,\min}{2} = (1\text{-D})*1.5*\text{Iout,min}$$

The average input current is the time average of the on-state current, plus the average output current, or:

Iin,max = 2*Iin,min

$$\text{Iin,ave} = \text{Iout,ave} + \text{D}* \frac{In,\max + Iin,\min}{2} = \text{Iout,ave} + \text{D}*1.5*\text{Iin,min}$$

Using the inductances, where Ltotal is the effective total inductance seen during the off-time:

$$\text{Toff} = \frac{Ltotal * (Iout,\max - Iout,\min)}{Vout - Vin} = \frac{Ltotal * Iout,\min}{Vout - Vin}$$

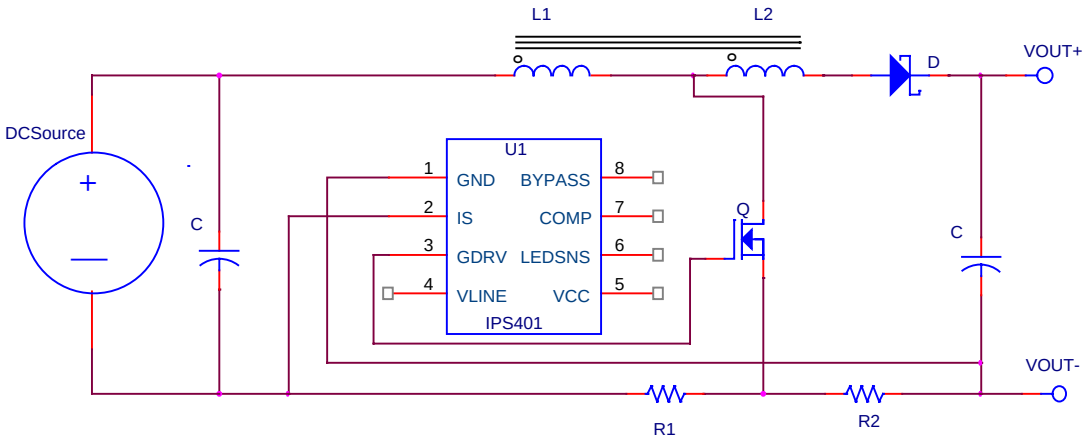
$$\text{Ton} = \frac{L1*(Iin,\max - Iin,\min)}{Vin} = \frac{L1*Iin,\min}{Vin}$$

$$\text{Freq} = \frac{1}{Ton + Toff}$$

$$\text{Power} = 1.5 * L1 * \text{Iin,min}^2 * \text{Freq}$$

Current sensing

The IPS401 requires that the input and output current be sensed, and sensed at the same scale (continuous current waveform) in order to find the "halfway points"). A single resistor will not work here, because neither the input nor output current is a straightforward continuous sawtooth waveform. An additional current sense resistor is needed to allow the different on-time and off-time current amplitudes to be combined into a well-behaved sawtooth. An example of that wiring is shown below. Note that the ground pin for the IPS401 is the output ground. Since this is a boost configuration, the input current will be greater than the output current. The IS (switched current sense) pin senses a negative voltage with respect to chip ground. During the on-time, there will be no current in R2, and the on-state current will be sensed by the voltage drop across R1. During the off-time, there will be no current through the FET, and the current will be sensed by the voltage drop across R1+R2. For most uses of this configuration, R2 is equal to R1 times the turns ratio.



Tapped boost discussion

A tapped-boost transformer will be a little larger than the boost inductor for the same output power. Another difference in component choice between the two topologies is the voltage rating of the output diode. In the boost, the output diode sees a reverse voltage equal to the output voltage. In the tapped boost, the reverse voltage is the output voltage plus the input voltage times the turns ratio. Conversely, and to the benefit of the tapped boost topology, the maximum voltage across the FET is the input voltage plus the output voltage minus the input voltage divided by one plus the turns ratio. As an example of these statements, using again a turns ratio of 10, an input voltage of 12 volts and an output of 450 volts: the maximum output diode reverse voltage will be 450 + 10*12 = 570 volts. The maximum FET voltage will be $12 + \frac{(450-12)}{(10+1)}$ = 51.8 volts. If the output power is such that R1 is 0.2 ohm, then R2 is 2.2 ohms.

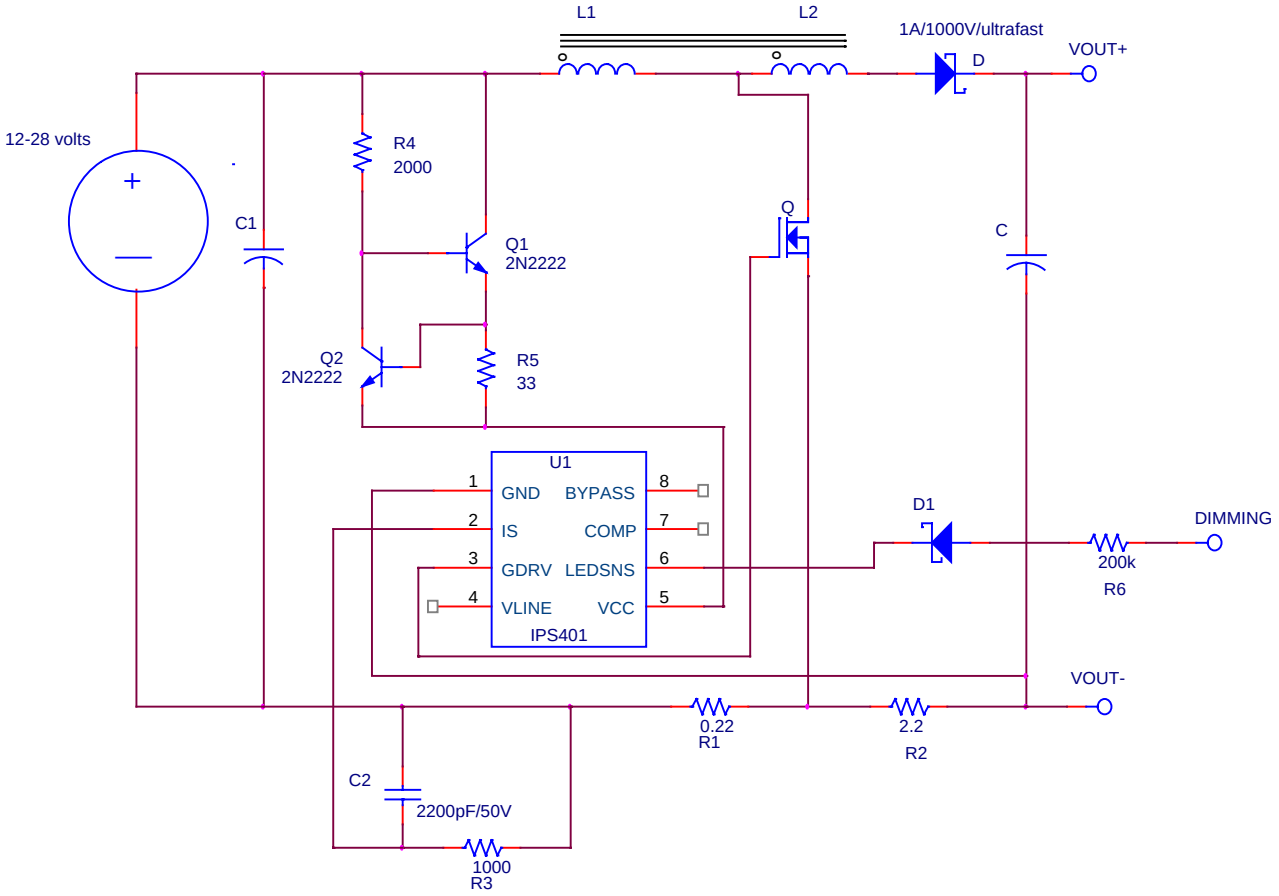
Detailed tapped boost design: 36W, 12-28V DC input, 450V DC out

A 10-to-1 turns ratio was chosen as a compromise between getting a duty cycle centered on 50% and reverse voltage on the diode. The primary inductance chosen is 165 microhenries. The expected component stresses in this design are:

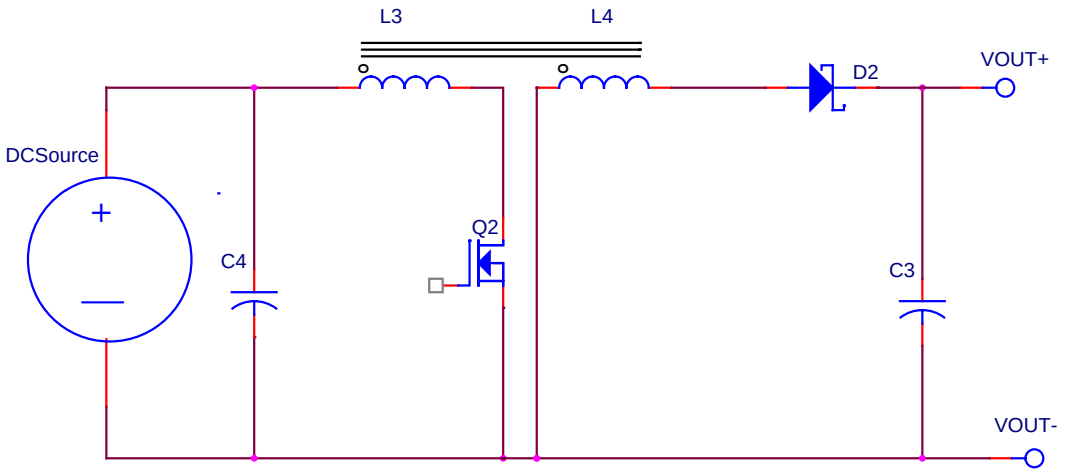
Maximum FET voltage (28 V input) = 70 volts
Maximum FET current (12 V input) = 5 amps
Maximum diode reverse voltage (28 V input) = 770 volts
Maximum frequency = 88 kHz

Transformer design

A PQ3230 ferrite core is a reasonable choice to keep the flux density to 0.2 tesla. 26 turns of 16 AWG wire on L1 and 260 turns of 30 AWG wire on the L2 fill the window area when using a bobbin. The copper is allocated in about a 70/30 split between the two windings (L1 gets more window area because it conducts during both the on-time and the off-time). The wound transformer is gapped to 165 microhenries L1 inductance (equivalent to 20 millihenries of total inductance with the two windings in series). Due to the comparatively low operating frequency, the lowest cost inductor would possibly be an iron powder variety.



Flyback Topology



In some cases, inrush current through the boost or tapped boost inductor to the large output capacitor when the input voltage is applied, can be a problem. Some applications need to be able to shut off the power from the input if there is a short on the output. Or the output voltage needs to be lower than the input. At times like these, a flyback topology might be the best selection. The buck and tapped buck topologies (not discussed here) can also be considered for the low output voltage case. For a review of the current sense resistor issues, please refer to the application note AN-IPS-07 http://www.in-plug.com/applinotes/AN-IPS-07_rev2_April07.pdf.

Flyback equations

The definitions of the variables are: I1p = switch current at the start of the on time, I2p = switch current at the end of the on time, I1s = secondary current at the beginning of the on time, I2s = secondary current at the end of the on time, Lp = primary inductance, N = turns ratio primary to secondary, Ls = secondary inductance, ton = switch on time, toff = switch off time, f = frequency, P = input/output power (assume 100% efficiency), Vo = output voltage, Io = output current, Vin = input voltage. The defining equations are then:

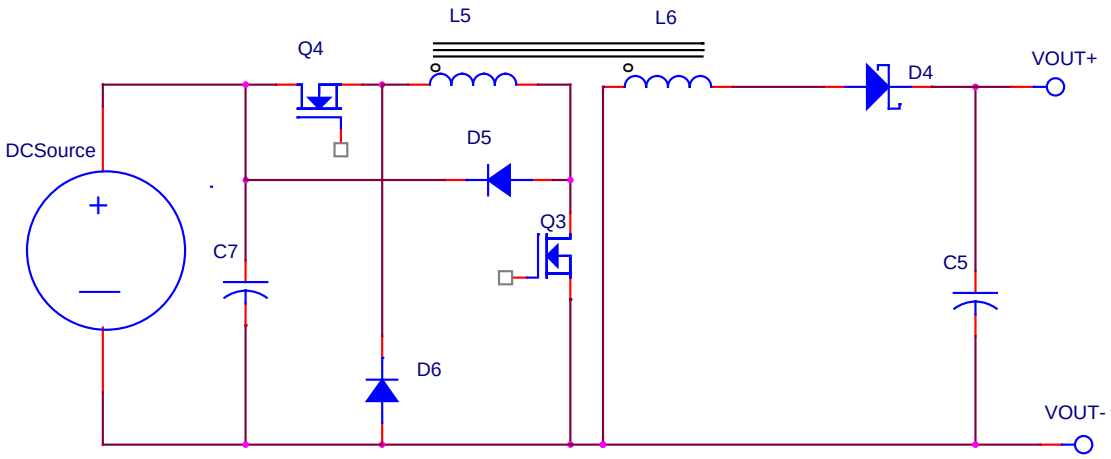
2*I1p = I2p
2*I1s = I2s
P = Vo * Io
P = 0.5*Lp*(I2p^2 - I1p^2)*f
P = 0.5*Ls*(I2s^2 - I1s^2)*f
F = 1/(ton+toff)
Ton = Lp *(I2p – I1p) / Vin
Toff = Ls *(I2s – I1s) / Vo
Lp = N^2 * Ls

If all these equations are solved simultaneously, the following result can be obtained:

I1p = 2*Io*[Vo +(Vin/N)]/[3*Vin]

Note that this current is independent of the choice of inductance. The assumption here is that the designer already knows Lp, N, Ls, Vin, Vo, and Io. Computing this value and back-substituting into the equations to get I2p, f, ton, toff, I1s, and I2s gives the complete description of the operating point.

Like all flyback power supplies, a flyback requires some amount of snubbing of the voltage spike on the FET drain in order to keep the voltage rating of the FET to an affordable number. At some point, it may be desirable to go to a "two switch flyback", which can reduce the voltage stress on the switch at the expense of using two switches, two diodes, and a high-side driver (magnetic or semiconductor). Pictured below is an example of the two switch approach. Note that the switches are driven on/off simultaneously, and all leakage inductance energy is returned to the input bus.



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