IN-PLUG® series: IPS102

Critical Mode PFC Controller
Low Cost, High Efficiency

INTRODUCTION

PRELIMINARY REV. 5

DESCRIPTION

The IN-PLUG® IPS102 is a primary-side switching controller which provides simple yet high performance active power factor correction (PFC). The IPS102 is intended for switch-mode power supplies (SMPS) up to 200W that require a minimum board area, reduced component count, and high efficiency.

A PFC forces a SMPS to draw an input current proportional to the instantaneous AC line voltage, thus resulting in excellent power factor and low line harmonics generation.

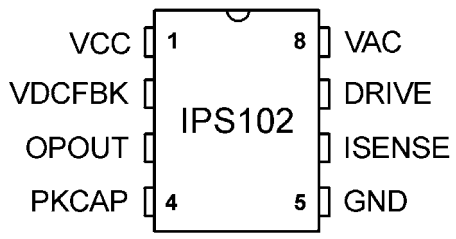
The output of the PFC is a regulated DC voltage. When using a boost topology this output voltage slightly exceeds the peak line voltage and is generally too high to be used as is, as well as not being isolated from the utility power. This is why a PFC is usually followed by either a DC/DC converter or uses a flyback topology in order to provide one or more isolated output(s) at the required voltage(s).

AAI offers the following solutions for the DC/DC converter:

- Flyback converters (see IPS1x series)
- Secondary side feedback controllers (see IPS 2x series)
- Push-pull converters (see IPS201 controller)
- Automotive converters (see IPS 31x series)

Other ICs and discrete solutions can be used as well.

PIN CONFIGURATION:



FEATURES

- Simple and easy to use.
- High efficiency over 96% (in optimized designs)
- Minimum external component count for lowest cost.
- 3-input current-mode multiplier ensures outstanding performance at any line voltage and any load.
- Under voltage protection.
- Voltage error amplifier with provision for loop stability compensation.
- Cycle to cycle current limiting.
- Thermal shutdown.
- Capable of driving a broad range of FETs.
- Self oscillating at frequencies up to 300KHz

BACKGROUND

Many countries impose regulations on the allowable power line harmonics that an electrical device can draw from the utility. The regulations vary with the rated power of the device as well as the type of device (lighting fixture, television, personal computer, etc). In addition to the compliance with power factor and line harmonics regulations, using a PFC offers other advantages like:

- Reducing the utility bill by making the actual power drawn from the line almost equal to the apparent power billed by the utility company
- Enabling more power to be drawn from the wall outlet or line circuit breaker without exceeding the limits set by UL or other safety agencies

APPLICATIONS

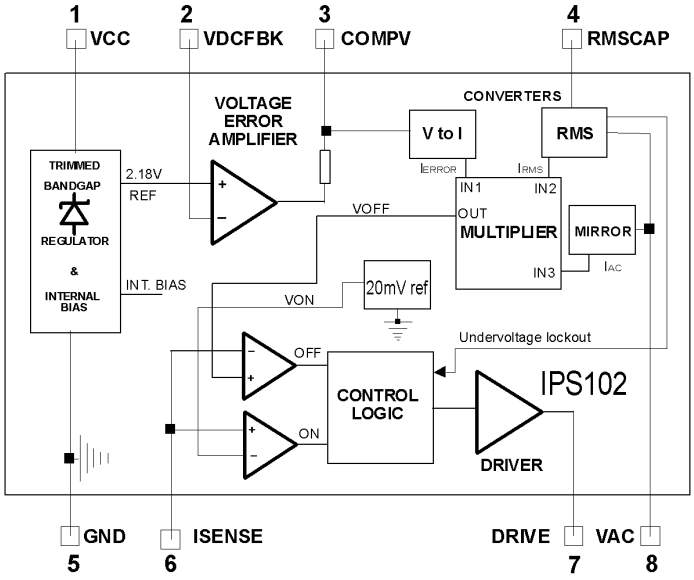
- SMPS
- Televisions and video displays
- Personal computers
- Electronic ballast
- Lighting fixtures

ORDERING INFORMATION

Part Number/Tube	Part Number/Tape&Reel	Package	Temperature Range	
IPS102C-D-G-LF	NA	8-Pin PDIP	0°C to +70°C	Commercial
IPS102I-D-G-LF	NA	8-Pin PDIP	-40°C to +85°C	Industrial
IPS102C-SO-G-LF	IPS102C-SO-G-LF-TR	8-Pin SOIC	0°C to +70°C	Commercial
IPS102I-SO-G-LF	IPS102I-SO-G-LF-TR	8-Pin SOIC	-40°C to +85°C	Industrial

For additional part number, packaging, and ordering information, please refer to the second-to-last page of this datasheet.

FUNCTIONAL BLOCK DIAGRAM



BASIC APPLICATION SCHEMATIC

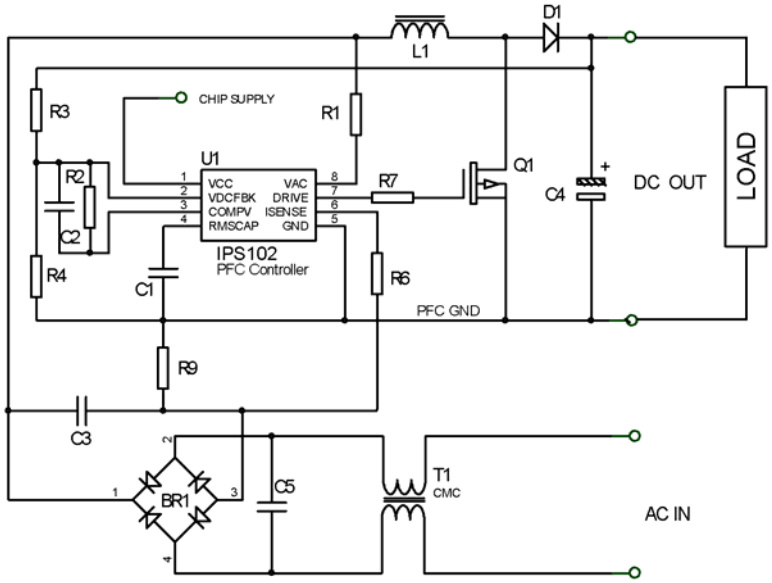


Figure 1

BASIC APPLICATION WITH DC/DC FEEDBACK CONTROL

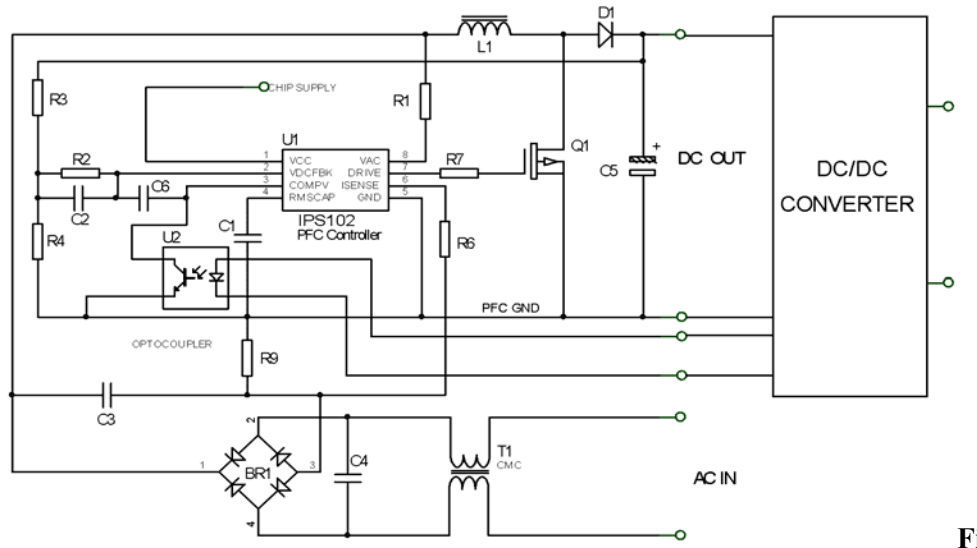


Figure 2

Note: This diagram displays a double feedback control. The resistor bridge R3/R4 can be set to safely guarantee a maximum output voltage while the feedback control signal from the DC/DC block through the optocoupler would manage the output voltage regulation.

PIN DESCRIPTION

Number	Name	Description
1	**VCC**	IC supply pin --The circuit contains a shunt regulator that behaves like a 10V zener. During start-up the IC draws very little current. Operations start when the "zener" value is reached and stop should the VCC voltage becomes less than approximately 8V.
2	**VDCFBK**	Voltage feedback input pin -- Negative feedback of the voltage error amplifier which positive input is internally connected to a 2.06V trimmed reference. It is used to regulate the voltage across the storage output capacitor to a value slightly above the maximum line peak voltage.
3	**VCOMP**	Voltage loop compensation pin -- This is the output of the voltage error amplifier and is used for loop feedback compensation purposes. Also used as an optional feedback loop to regulate the output of a DC/DC converter fed by the PFC controller (see Fig. 2)
4	**RMSCAP**	RMS capacitor pin -- The capacitor connected between this pin & GND generates a current proportional to the RMS value of the AC line voltage which feeds the multiplier circuit to maintain the loop gain constant at different line voltages thus preventing loop instabilities which could occur with other arrangements.
5	**GND**	Ground
6	**ISENSE**	Inductor current sensing pin -- This pin is used to measure the current flowing through the inductor which is forced by the PFC controller to be proportional to the instant AC line voltage. The power MOSFET is automatically driven in a self-oscillating mode to restart a new cycle when the current in the inductor has dropped below the near-zero reset threshold.
7	**DRIVE**	MOSFET gate drive pin -- The internal buffer connected to this pin can drive a broad variety of power MOSFETs and IGBTs. A series resistor is sometimes added to improve the EMI signature.
8	**VAC**	AC voltage pin -- This pin is used to sense the instantaneous AC line voltage through a series resistor that performs a voltage to current conversion. The resulting current feeds the multiplier in order to force the peak current in the inductor to be proportional to the instant AC line voltage.

OVERVIEW

Without PFC, most SMPS simply rectify the AC voltage to charge a relatively large capacitor. This results in huge spikes drawn from the line which generates harmonics and degrades the power factor to 0.5 – 0.7.

With the IPS102, the power factor exceeds 0.95 and the harmonic distortion could be less than 5%. The IPS102 is also a very efficient pre-regulator that charges a storage capacitor at an adjustable regulated DC voltage. This feature can be used to build very high-efficiency and low-cost isolated SMPS featuring single or multiple outputs in the range of 50-500W.

OPERATING DESCRIPTION:

3-input current multiplier:

The heart of the IPS102 PFC controller is a 3-input current-mode multiplier. This multiplier is key in monitoring a constant loop gain that is the only way to ensure a good stability and response over a broad range of input AC voltages and output loads.
The first multiplier input is fed by I_{AC}, a current proportional to the instant AC line voltage. This information is used to force the current drawn from the AC line to be proportional to the instant line voltage thus resulting in a power factor close to unity. The SMPS then behaves like a resistive load whith an impedance that varies according to the RMS line voltage and the load thanks to the other action of the two multiplier inputs.
As shown in Fig. 1, a resistor (R1) connected between V_{AC} and the rectified AC line voltage, performs the V to I conversion that generates $I_{AC.}$ The value of R1 is usually 1 MΩ.
The second multiplier input is fed by I_{RMS} , a current proportional to the AC line RMS value. This current is derived from I_{AC} by a dedicated RMS converter using only a non-critical external capacitor (C1).
The value of C1 is usually 1 uF for 50 / 60Hz operations. A much lower value would result in a more harmonic distortion. The purpose of feeding the I_{RMS} is to reduce the loop gain at high voltages. It would otherwise become excessive and create stability problems.
The third multiplier input is fed by a current proportional to the error amplifier output voltage. The purpose is to smoothly change the RMS value of the sinusoidal current drawn from the AC line, to match the power demand and maintain a good regulation of the output voltage.

Voltage error amplifier:

The IPS102 includes a voltage error amplifier with a non-inverting input connected to an internally trimmed 2.06V reference. Its inverting input is the VDCFDBK pin. The error amplifier output is the VCOMP pin and is also internally connected to the V-to-I converter feeding the multiplier as discussed before. As indicated in the typical application schematic of figure 1, the VDCFDBK and VCOMP are used for the following purposes:

(a) voltage divider R3, R4 used to set the value of the regulated DC output voltage:

DC out = 2.06 x (R3 +R4)/R4 (see Fig. 1)

(b) the loop feedback compensation network R2, C2, C6 (see Fig. 1) provides a suitable network for most applications. More complicated schemes are possible for demanding applications where transient response is paramount.

MOSFET current control:

The IPS102 is most typically used to control a boost converter that operates from raw rectified AC. It uses a high-Q inductor operating in critical mode to generate a regulated DC output that always slightly exceeds the peak value of the AC input voltage. The minimum current in the inductor is zero. When zero inductor current is detected at the ISENSE pin, the FET is turned-on via the DRIVE pin. The maximum current in the inductor is set by the output of the multiplier and will increase with the output power demand. At startup, when VCC is established, there is no inductor current and the control logic turns the MOSFET on. The current in the inductor (and also in the MOSFET) is sensed by R9 which value along with L1 defines the power handling capacity of the PFC.

When the current reaches the peak value set by the output voltage of the multiplier, the MOSFET is switched off and the current in the inductor, still sensed by R9, decreases as the inductive energy is dumped into the storage capacitor. When the current reaches zero, the control logic turns the MOSFET on again. The system is therefore self-oscillating and does not require any dedicated oscillator. It should be noted that the ZEROD signal is only sensed while the FET is 'off', and is ignored while the FET is 'on'.
Please note that the frequency varies with the load and the line voltage, but against common belief:
- its variation usually stays in a 2:1 range,
- its jitter is favorable to the EMI signature,
- it decreases when the load increases which is excellent for the efficiency of the PFC.

MOSFET driver:

The MOSFET driver has been sized to be capable of driving power MOSFETs featuring a total gate charge up to 80nC.
Due to the continuous mode of operations of the inductor, the MOSFET must be driven with a reasonably (but not excessively) low impedance, to minimize switching losses at both turn-on and turn-off without generating excessive EMI.
In term of Ron, the driver's output devices are as follow:
- P-channel Ron: 30 Ω typical
- N-channel Ron: 20 Ω typical

A series resistor should be added to the DRIVE pin between DRIVE and the MOSFET gate to further reduce EMI and minimize the noise injection which could result from Miller-capacitance kick-back during transient conditions. This also limits the possibility of fast transients capacitively coupling from the FET into the DRIVE pin and errantly forcing it below ground, which can cause latchup.

Examples of suitable MOSFETS:
- **IXYS PolarHT™ and Polar HV™** MOSFET series: IXTY1R4N60P, IXTY2N60P, IXTY3N60P
- **Fairchild** MOSFET series: FQPF1N60, FQPF 2N60, FQPF 3N60.
- **Infineon COOLMOS™** series: SPD01N60S5, SPD02N60S5, SPD03N60S5.
- **Motorola** MOSFET series: MTP1N60, MTP2N60, MTP3N60.
- **SGS-Thomson** MOSFET series: STD1NB60, STD2NB60, STD3NB60.
- **Etc…**

Notes:
- Due to the rapid evolution of MOSFET technologies, please check for current models when designing a new SMPS.
- **PolarHT™ and Polar HV™** are trademarks of IXYS corporation

COOLMOS™ is a trademark of Infineon.

Thermal shutdown:

An internal temperature sensing protection circuit disables the MOSFET gate drive when the temperature exceeds a typical value of 150°C. This circuit has sufficient hysteresis to prevent relaxation. Normal operations therefore only resume when the junction temperature has dropped below approximately 120°C.

Shunt bandgap regulator:

The IPS102 internal trimmed bandgap shunt regulator behaves like a 10V zener but also provides the 2.06V reference for the voltage error amplifier, and the various internal bias current and voltages required by the different blocks.
During start-up, the current consumption in the regulator is very low, typically 100µA, allowing many possible schemes to power the IPS102. Once the "zener" value is reached, the MOSFET gate drive is enabled and normal operation starts. When enabled, the typical chip consumption is 660 µA plus the current necessary to drive the MOSFET which depends on the MOSFET's total gate charge and the frequency of operation (linked to L1 inductance value).

The VCC voltage is allowed to drop below the "zener" value during normal operations but the circuit will reset itself and re-enter start-up mode should the VCC drop below approximately 8 volts.
The shunt regulator is sized to handle up to 50mA, which is especially useful to power the IPS102 with few components only. Be careful however not to exceed the package rated power dissipation (see table on page 8).

How to power the IPS102:

There are several ways of supplying power to the IPS102 which depends on whether the PFC is used as a stand-alone block or is followed by a DC/DC converter or other blocks using additional ICs which must be energized as well.

Stand-alone applications

Simple RC network:

The simplest technique well suited for 120V AC (domestic US and Japan) uses an RC network connected between DC out and GND. R5 should be sized to deliver enough Icc current for normal operation without wasting power.

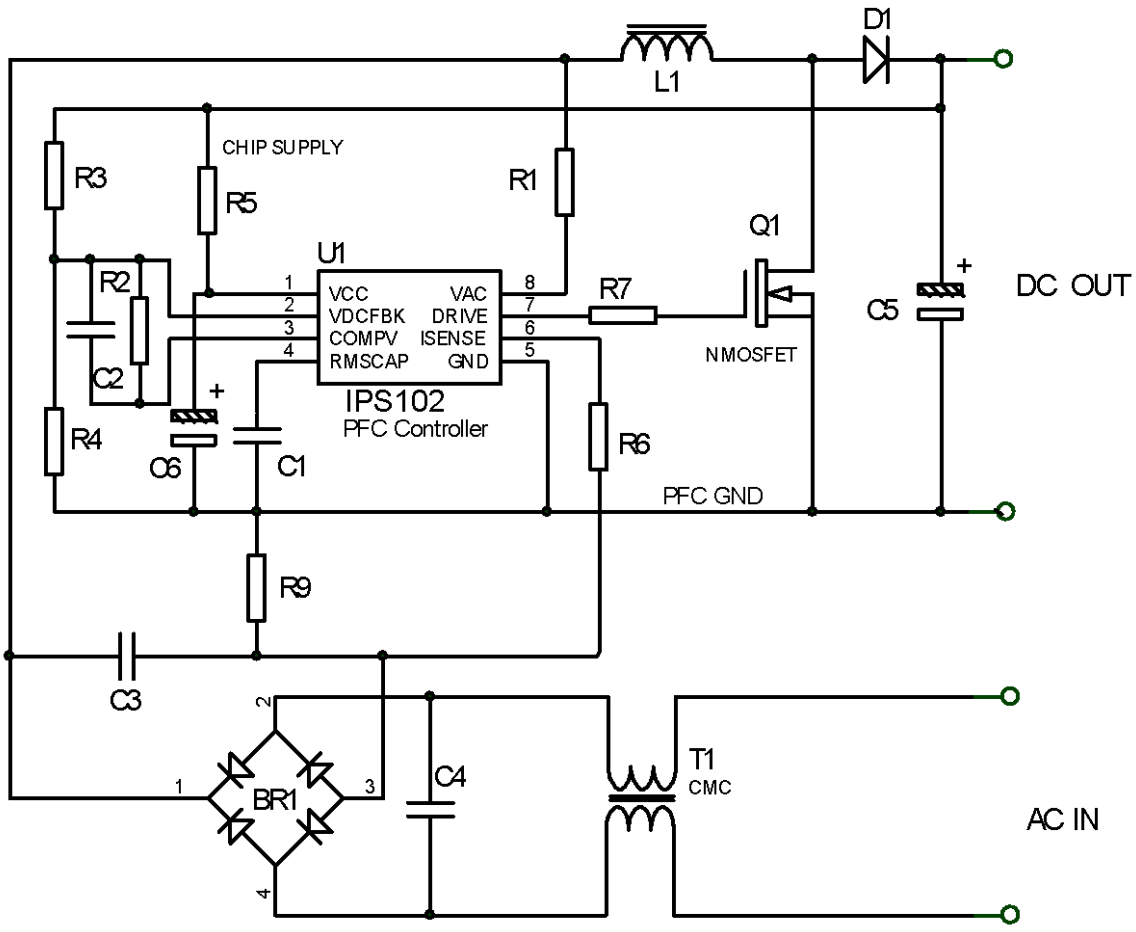


Figure 4

Auxilliary winding:

The most efficient technique suitable for international applications (85V- 265V AC) uses an auxillairy winding on the switching inductor TX1. The turn-ratio between the principal winding and this auxilliary one is usually between 5 and 15. The wire size should be suitable for 20mA RMS which is quite small.

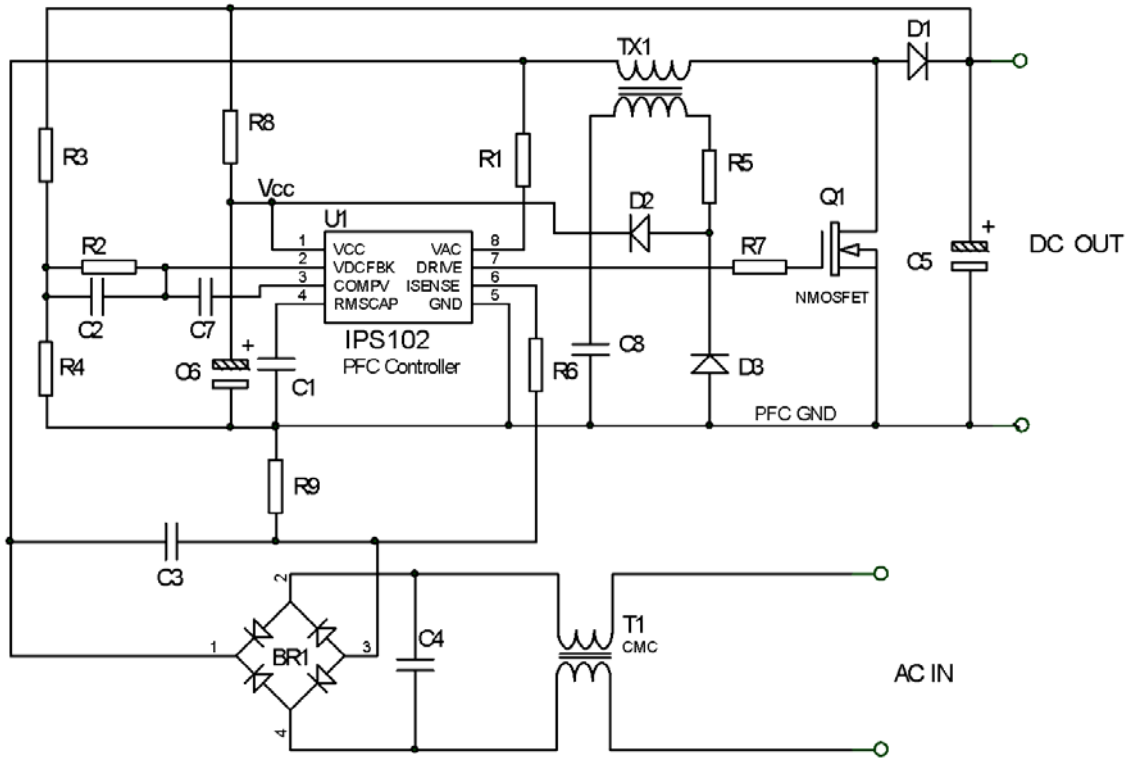


Figure 5

Applications with DC/DC converter:

The auxilliary winding on L1 can be saved and the VCC supply for the the IPS102 is then provided by the DC/DC converter circuitry. The current provided by AAI patented snubber and R9/C7 networks is divided and derived into R13/C10 and R5/C11 to feed flyback and feedback controllers respectively.

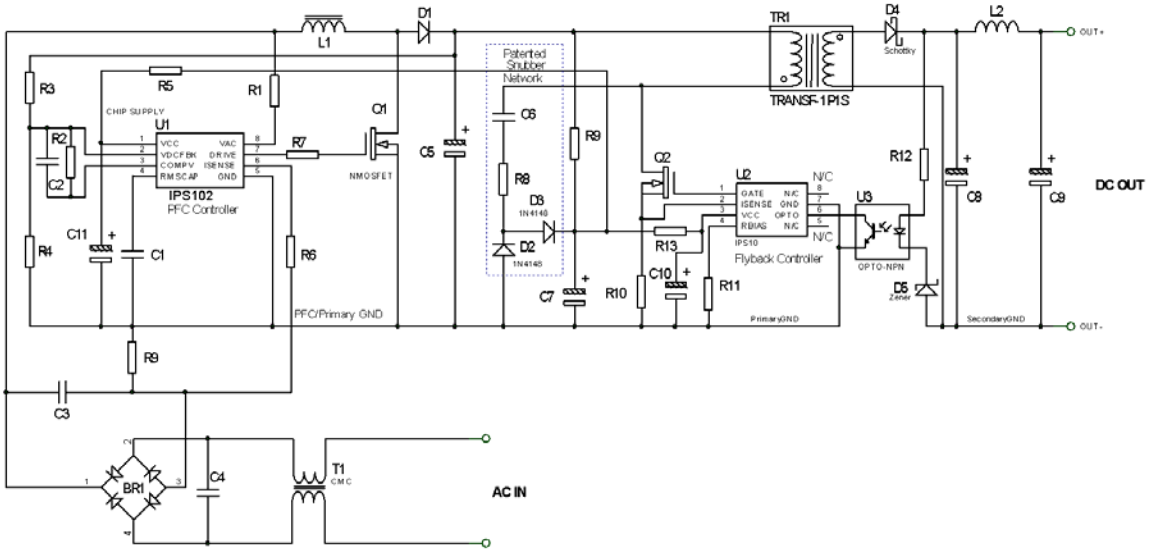


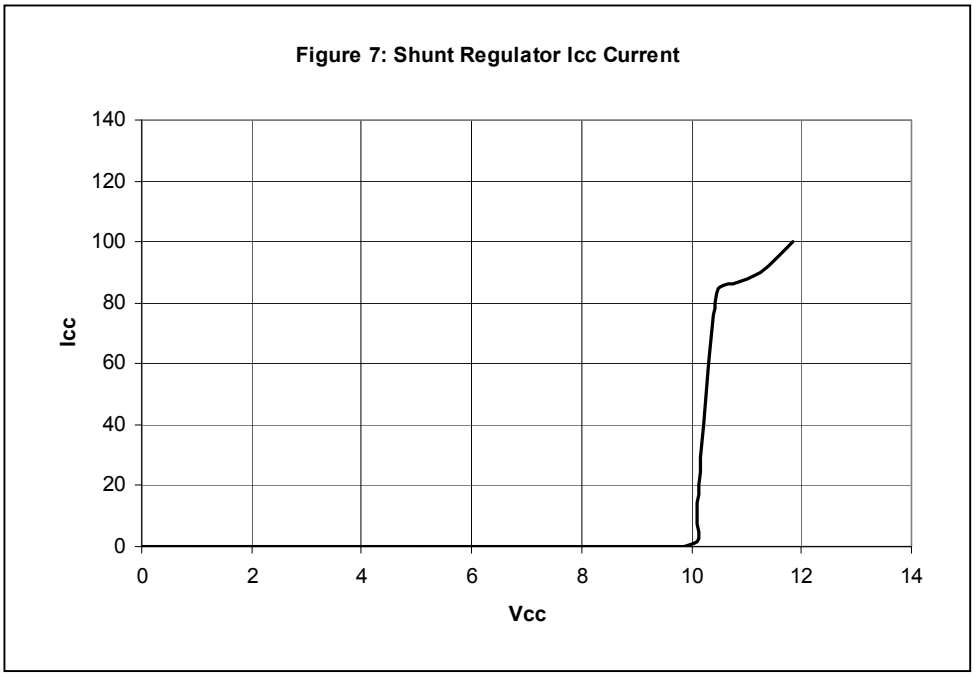
Figure 6

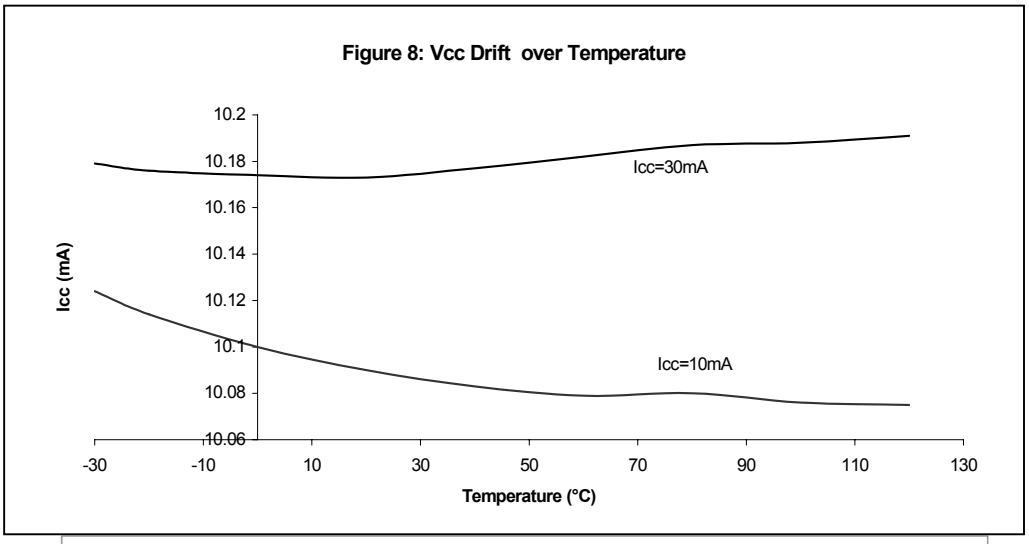
ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING		
CHARACTERISTIC	**VALUE**	**UNITS**
Shunt regulator max I_{CC} non-repetitive current - see fig 7-	60	mA
Peak drive output current	Source=100, Sink=200	mA
ISENSE input voltage	0 / - 10	V
VAC maximum input current	700	µA
Junction to case thermal resistance $R_{\theta J-C}$	PDIL = 42, SOIC = 45	°C / W
Junction to PCB thermal resistance $R_{\theta J-A}$	PDIL = 125, SOIC =155	
Power dissipation for T_A <= 70°C	PDIL = 640, SOIC = 500	mW
Operating junction temperature	- 40 to 150	°C
Storage temperature range	- 55 to 150	
Lead temperature (3 mm from case for 5 sec.)	260	

PARAMETER	TEST CONDITIONS	PARAMETERS			UNITS
	@ 25°C unless specified	MIN.	TYP.	MAX.	
Supply, bias & circuit protection					
Shunt regulator voltage (V_{CC})	ICC = 10 mA	9.7	10.0	10.3	V
Shunt regulator dynamic resistance	1 to 30 mA	2	4	6	Ω
Shunt regulator peak repetitive current (I_{CC})		-	-	50	mA
Start-up current (I_{CC})		-	100	150	μA
Under voltage lock-out (V_{CC})		V_{CC} – 2.1	V_{CC} - 1.8	V_{CC} - 1.4	V
Min I_{CC} to ensure continuous operation	4A, 600V, 20 nC MOSFET , L= 7 mH	-	3	-	mA
Thermal shutdown trip temperature		-	150	-	°C
Multiplier					
Maximum operating voltage across ISENSE resistor	See note2	-1.3	-1.2	-1.1	V
COMP voltage range		0	-	3	V
VAC input current operating range	I_{CC} = 1 to 10 mA Temp = 0 to 70°C	20	-	600	μA
RMS capacitor		-	1	-	μF
Error amplifier					
Reference voltage		2.01	2.06	2.10	V
Open loop gain		-	85	-	dB
3 dB response		-	200	-	Hz
Phase margin	Unity gain	65	-	-	Degrees
Output impedance		-	30	-	KΩ
DRIVE to MOSFET gate					
'high' gate driver saturation	10 mA (source)	-	0.3	0.5	V
'low' gate driver saturation	10 mA (sink)	-	0.2	0.35	V
Gate pull-down resistor	(internal)	30	45	65	KΩ
Rise time (10% to 90%)	390 pF load	-	100	200	ns
Fall time (10% to 90%)	390 pF load	-	50	100	ns
Max recommanded total external MOSFET charge		-	-	50	nC
Zero current detect			20		millivolts

Note1: Electrical parameters, although guaranteed, are not all 100% tested in production.
Note2: To avoid damage to the ISENSE pin by the in-rush current, size R6 to limit the input current into the IC to 30mA. 1Kohm to 33Kohm are suitable values for most applications.





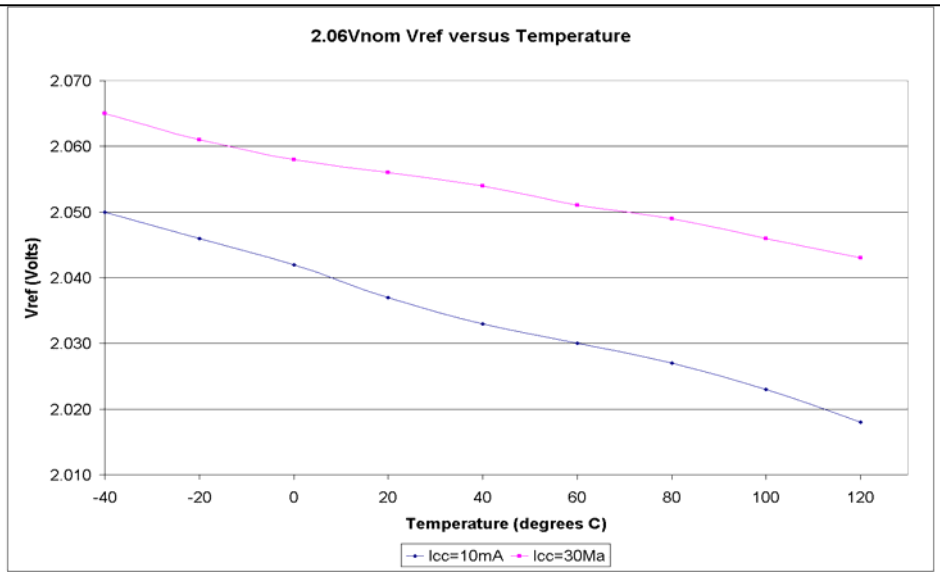


Figure 9. Vref versus Temperature

Figure 10: Start-Up Current Drift over Temperature

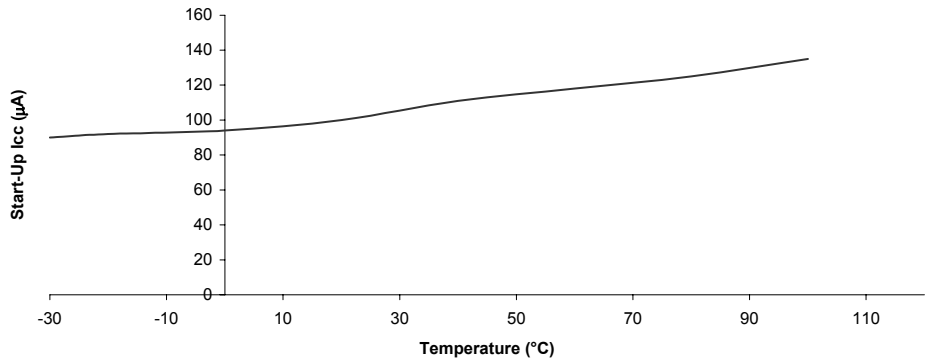
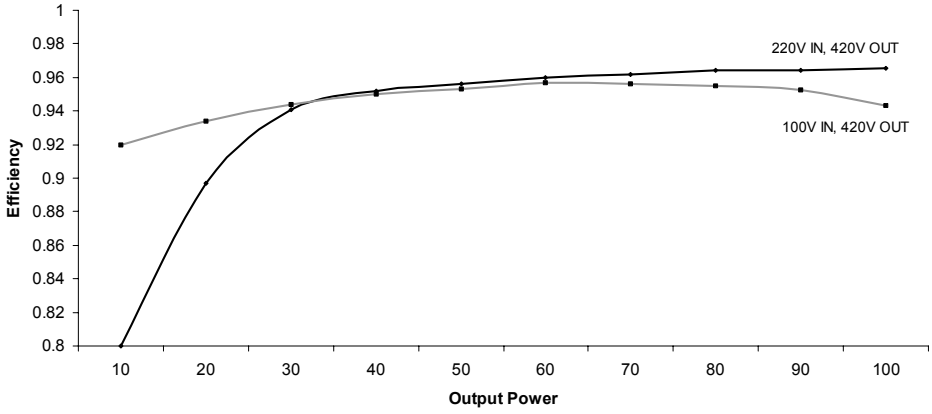


Figure 11: Efficiency versus Output Power



EXAMPLE OF POWER FACTOR CORRECTION: Universal Input, 400V DC, 60W output (TX1= PQ2620,Np=155,Nvcc=12,Lp=3.5millihenries)

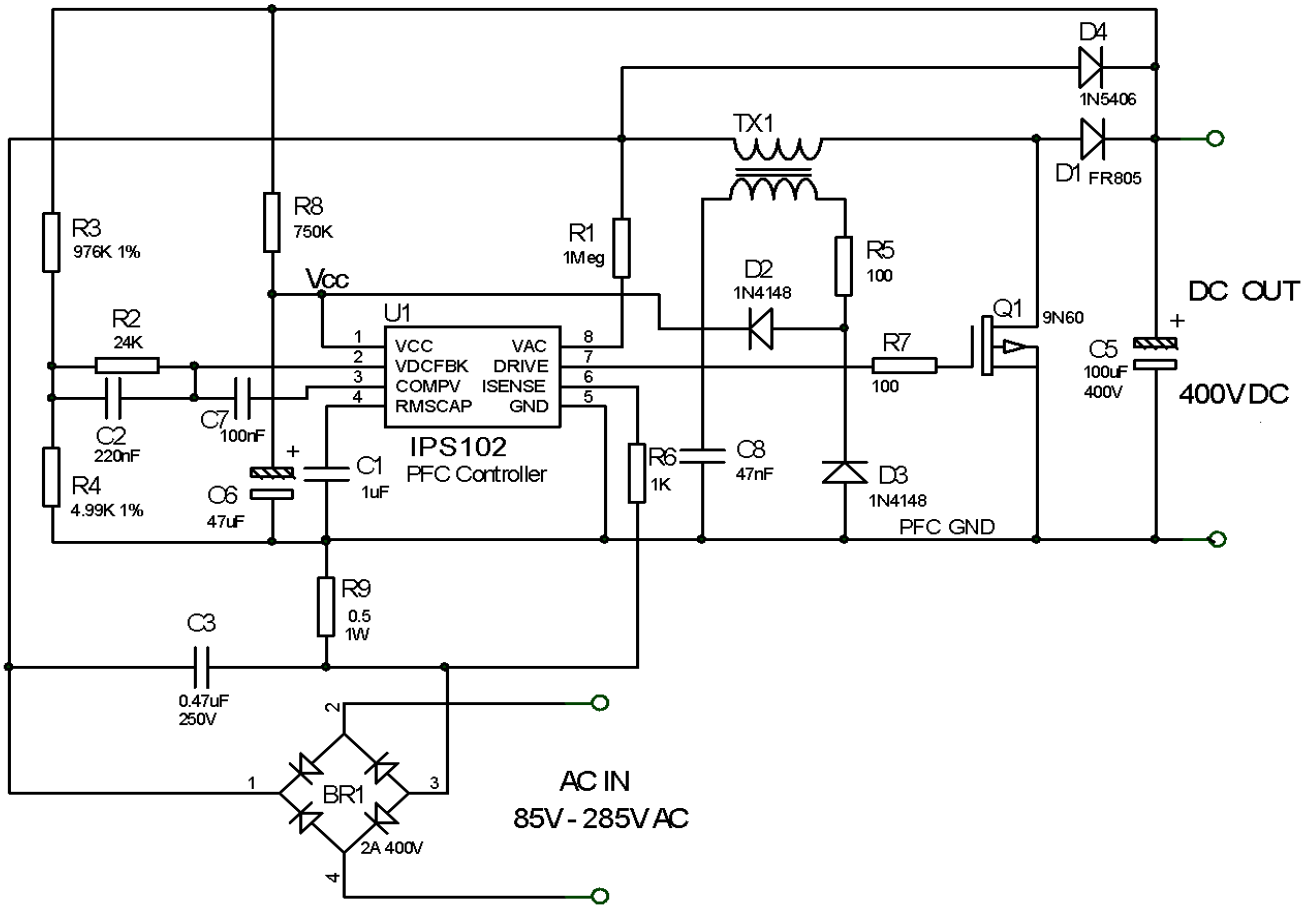


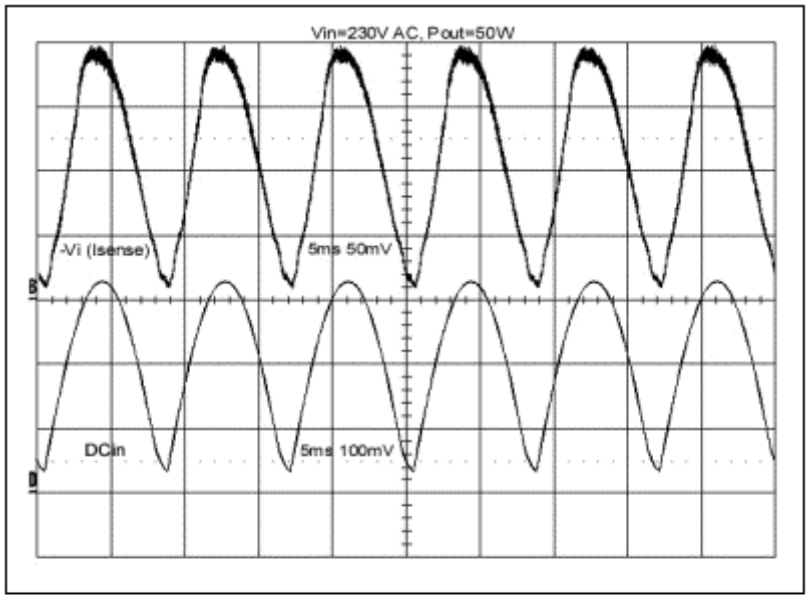
Figure 12
Note: 1mH to 10mH inductors (TX1) could be used depending on conditions and targeted characteristics.

APPLICATIONS NOTES

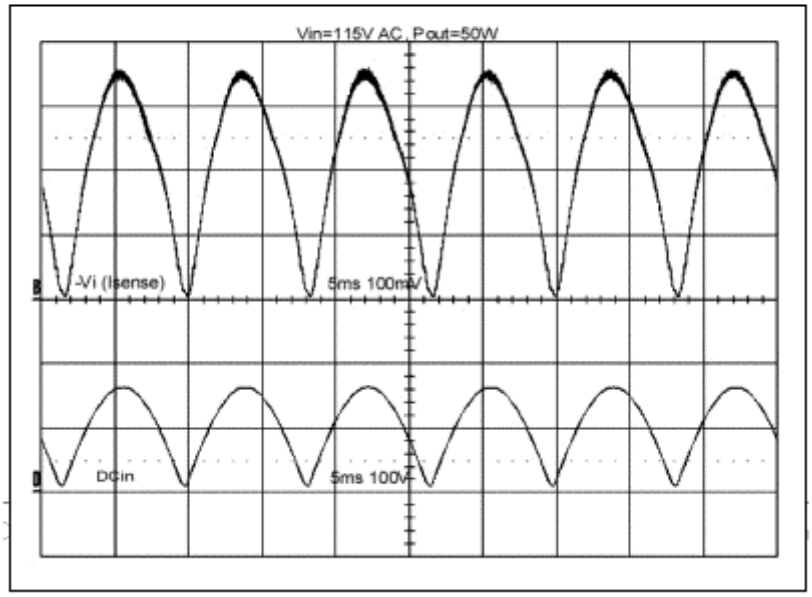
TESTING/START-UP

The voltage across the main ISENSE resistor must be less than the zero detect threshold for the chip to reliably turn on the FET gate. If testing or operating the chip with a constant-current load, this could cause a startup problem. The initial input current through the inductor and output diode before the chip powers-on could be sufficient to be above the sense voltage and prevent the chip from starting. This is less likely with a resistive load, although the problem can still occur if the initial input voltage is high enough to cause sufficiently high ISENSE voltage to be generated before the chip starts.

Example line current waveforms



Vin= 230V, Pout=50W



Vin= 110V,Pout=50W

PACKAGE DIMENSIONS AND MARKING

The IPS102 is available in plastic 8-pin DIP and plastic 8-pin SOIC packages. Refer to the latest version of specification AAPS001 (ASIC Advantage's "Package Numbering, Marking, and Outline Standard", available at www.asicadvantage.com) for specific information concerning the package dimensions and package marking.

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