IN-PLUG® series
Low Cost, High Efficiency, Low Power
Synchronizable Flyback Controller IPS16

PRELIMINARY DATASHEET REV2

INTRODUCTION

DESCRIPTION

The IN-PLUG® IPS16 has been designed for low-cost, high efficiency Switch Mode Power Supplies used in CRT monitor and TV applications. It is an enhanced version of the IPS15 which original functions have been retained. This includes soft start, shunt-regulator, precision oscillator, PWM with its associated comparator and loop compensation components as well as all the necessary biasing and protection circuitry (on-chip sensing thermal shutdown, under-voltage, line over-voltage and over-current).

It has also been optimized for stand-by applications where the SMPS has to deliver a small amount of power while being required to comply with the tightest “green” regulations.

Additional resetable oscillator for horizontal scan synchronization features, suitable for CRT monitor and TV SMPSs has been added.

The IPS16 is powered through a novel patented network which replaces the usual snubber network. AAI will grant one non-exclusive royalty-free licence to use this arrangement for each IPS16 purchased by Customers, either directly from the company or through approved sources.

The IN-PLUG® IPS16 can drive a large variety of power MOSFETs hence providing the maximum flexibility at the lowest possible cost.

The IPS16 ultimately features a minimum power consumption in “light load” conditions by entering a cycle skipping mode.

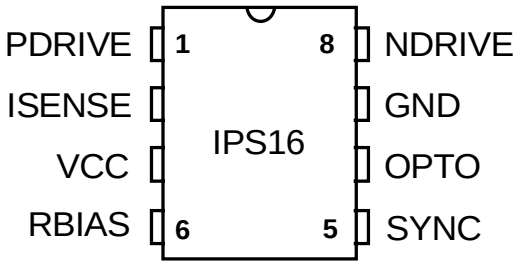
APPLICATIONS

SMPS for CRT & TV Monitors

FEATURES

- Very cost-effective solution to design SMPS used in CRT and TV Monitor applications.
- Enters a "Cycle skipping" mode in "light load" conditions for ultra green low power requirements
- Wide range PWM for stable operation at any load and line voltage.
- EMI noise reduction thanks to:
  - Adjustable operating frequency.
  - Separate MOSFET N & P drives
- Lower quiescent current (max. 50% of the IPS15)
- Power shut-down for standby modes.
- Cycle to cycle over-current protection
- Under-voltage lock-out
- Synchronizable by external signal

PIN CONFIGURATION: DIP-8 / SOIC-8



ORDERING INFORMATION

Part No.	ROHS / Pb-Free	Package	Temperature Range	
IPS16C-D	-G-LF	8-Pin PDIP	0°C to +70°C	Commercial
IPS16I-D	-G-LF	8-Pin PDIP	-40°C to +85°C	Industrial
IPS16C-SO	-G-LF	8-Pin SOIC	0°C to +70°C	Commercial
IPS16I-SO	-G-LF	8-Pin SOIC	-40°C to +85°C	Industrial

For detailed ordering information, see page 16

BASIC APPLICATION SCHEMATICs

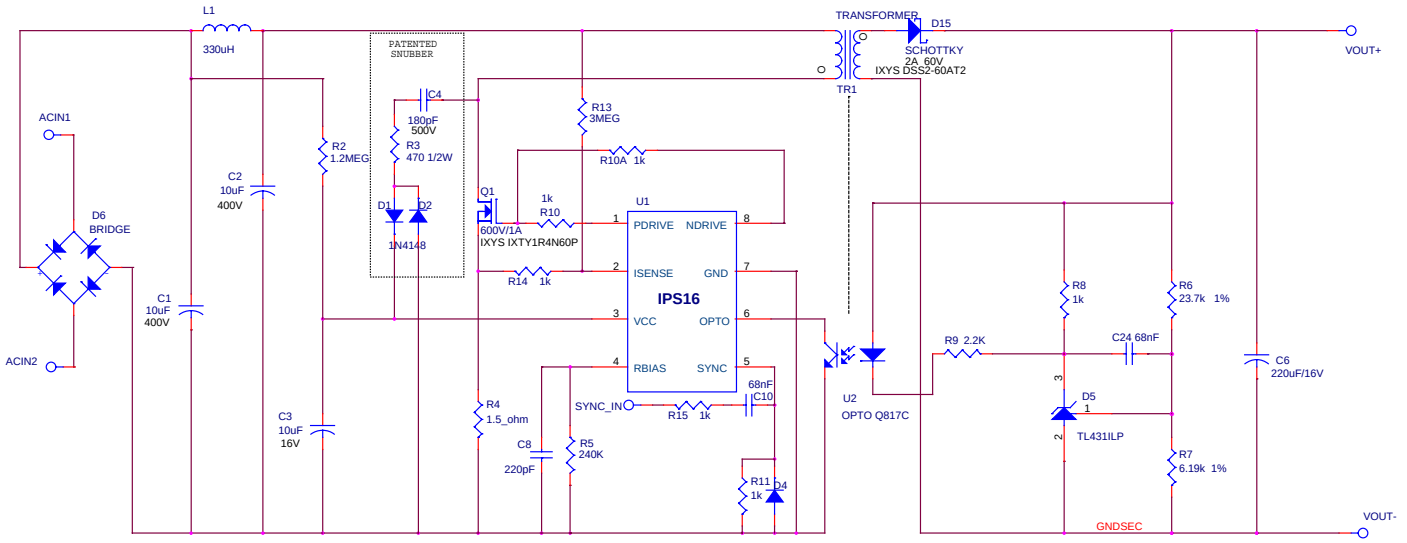


Figure 1 (Isolated solution)

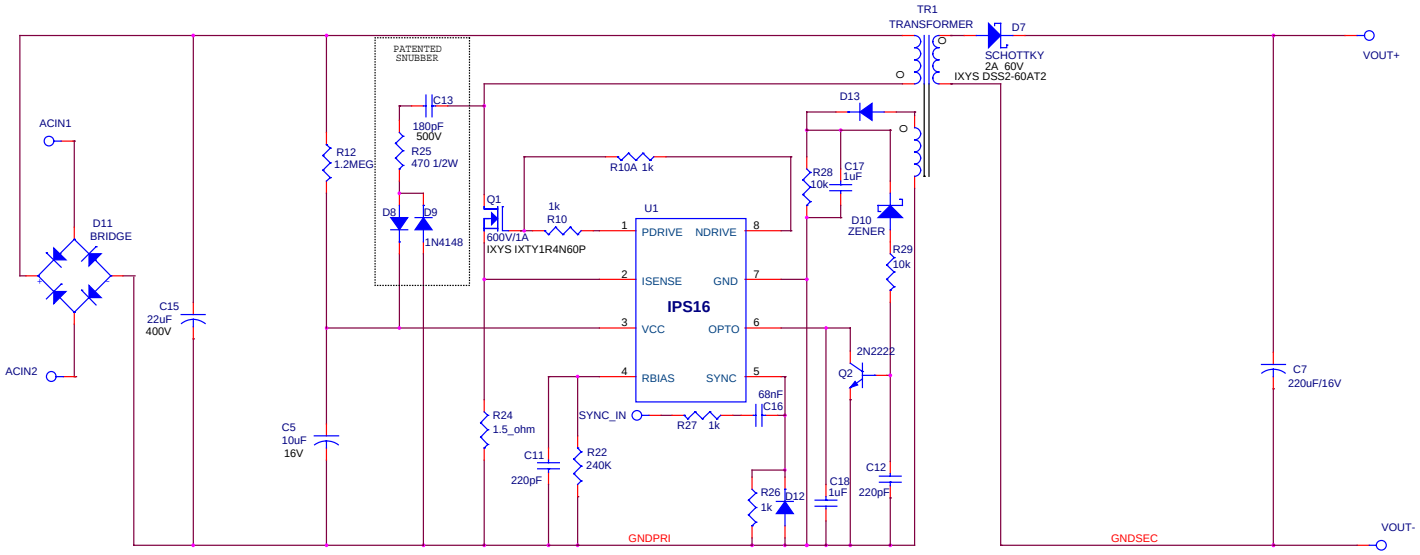


Figure 2 (Bias winding feedback)

FUNCTIONAL BLOCK DIAGRAM

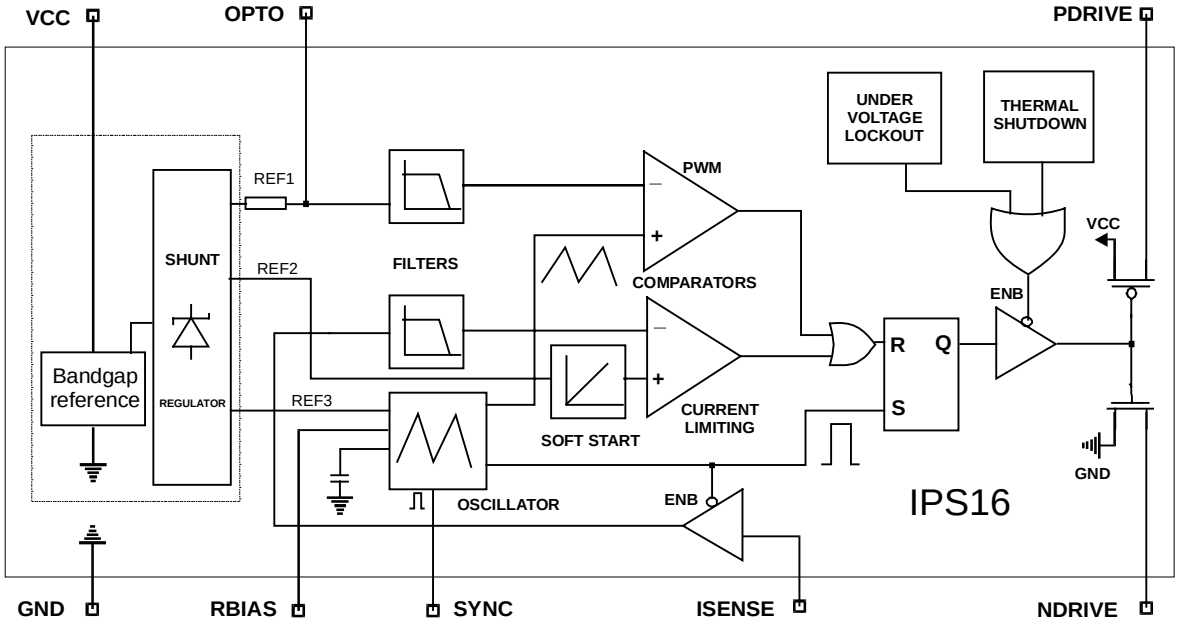


Figure 3

PIN DESCRIPTION

Number	Name	Description
1	**PDRIVE**	Internal P drive terminal to be connected to the gate of the outside power MOSFET. (The rising edge can be adjusted with an external resistor)
2	**I_{SENSE}**	MOSFET current sensing. Any voltage over 700 mv @ 25°C on this pin will stop gate pulses.
3	**V_{CC}**	IC positive supply. The chip behaves like a 9.5 volts nominal zener diode.
4	**R_{BIAS}**	Connection to external R_{BIAS} resistor to set the operating frequency.
5	**SYNC**	Synchronization pulse input to reset and synchronize the oscillator. (level "1" is active)
6	**OPTO**	This input should be connected to the optocoupler
7	**GND**	Ground.
8	**NDRIVE**	Internal N drive terminal to be connected to the gate of the outside power MOSFET. (The falling edge can be adjusted with an external resistor).

IN-PLUG® IPS16 SERIES FUNCTIONAL DESCRIPTION

The **IPS16** is a PWM controller for Switch Mode Power Supply designed for CRT and TV Monitor applications. It has been optimized to reduce the external component count. The principal features are:

- Low start Current;
- “Cycle skipping” in "light load" conditions for ultra green low power requirements;
- Low quiescent Current (half of IPS15);
- Shunt regulator to allow the maximum flexibility to power the chip.;
- Protections against overheating (on-chip sensing), under-voltage and over-voltage;
- Precise oscillator with externally adjustable frequency. The oscillator frequency is level synchronizable with an external pulse applied on pin SYNC (SYNC=1);
- Dual mode feedback control (optocoupler or bias winding);
- On-chip filters for the loop compensation and the over-current sensing;
- Soft start to protect the MOSFET;
- Separate MOSFET P and N drivers to adjust rising and falling edge independently.

The shunt regulator operates like a zener diode, keeping the chip supply voltage around 9.5 volts. At start-up the chip stays in stand-by mode until the voltage of VCC reaches about 9.5 volts. During this phase, the consumption is of the order of 120 µA. When the 9.5 volts are reached, the driver starts providing gate pulses. The chip will go back to the stand-by mode if the supply voltage decreases down to ~8 volts. The overall chip consumption in normal operation is about 600 µA, not counting the current required to drive the MOSFET gate.
The IC gets the start current from a resistor connected to the rectified line voltage (~150 µA) then, after the first gate pulse, AAI patented modified snubber network (*) or a bias winding from the transformer provides the additional current to keep the chip running (see figure 6 for details).
The opto pin is pulled to VCC through an internal resistor, allowing a maximal duty cycle of 25 % in free running oscillator conditions. The oscillator can be reset by an external signal (this function is especially adapted for TV and CRT Monitor horizontal scan synchronization) and during this synchronization phase, the duty cycle is allowed to reach up to 90%.

Please note that for correct operations, the frequency of the synchronization signal should be greater than the selected free running frequency defined by Rbias.
During start-up and in free running oscillator conditions, the duty cycle is controlled by the internal soft start unit which smoothly increases the MOSFET current up to its maximum. The maximum MOSFET current corresponds to 700mV developed across the current sense resistor connected to the ISENSE pin.
When the expected output voltage is reached, the optocoupler's led is driven, and the opto pin voltage decreases, reducing the duty cycle to a controlled value. The current limiting protection operates by turning-off the MOSFET when the ISENSE pin voltage exceeds ~700 mv. This ensures cycle-to-cycle protection of the MOSFET and provides a mean of operating the power supply in constant-power mode.
In “light load” condition, the IPS16 enters a cycle skipping mode to keep the power consumption to a minimum. When the IPS16 is synchronized, the IC assumes that the application is in normal operating condition and the cycle skipping feature is disabled.

OUTPUT POWER CAPABILITY			
Part Number	**Package**	**230V AC or 115V AC w/ Doubler**	**85 – 285V AC**
IPS16	**DIP-8 / SOIC-8**	**Up to 70W (1)**	**Up to 30W (1)**

(1) Note: Governed by size and package of external MOSFET

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING		
Characteristics	**Value**	**UNITS**
Shunt regulator max I_{CC} (pin 3) - see fig 5-	**80**	**mA**
All analog inputs (pin 2, 4, 5, 6, 8)	**Min= -0.3, Max= +6.3V**	**V**
Peak drive output current (pin1, pin10)	**Source=100, Sink=170**	**mA**
Junction to case thermal resistance $R_{\theta J-C}$	**PDIL = 42, SOIC = 45**	**°C / W**
Junction to PCB thermal resistance $R_{\theta J-A}$	**PDIL = 125, SOIC =155**	
Power dissipation for T_A <= 70°C	**PDIL = 640, SOIC = 500**	**mW**
Operating junction temperature	**- 40 to 150**	**°C**
Storage temperature range	**- 55 to 150**	
Lead temperature (3 mm from case for 5 sec.)	**260**	

ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETER	TEST CONDITIONS	PARAMETERS			UNITS
	@ 25°C unless specified	MIN.	TYP.	MAX.	
Supply, bias & circuit protection					
Shunt regulator voltage	ICC = 1 mA	9.2	9.7	10.5	V
Shunt regulator dynamic resistance	1 to 30 mA	2	3	5	Ω
Shunt regulator max peak repetitive current		-	45	-	mA
Min I_{CC} to start oscillator		-	-	80	µA
Under voltage lock-out		V_{CC} – 2.2	V_{CC} - 1.5	V_{CC} - 1.4	V
Min I_{CC} to ensure continuous operation	1A, 600V, 5 nC MOSFET	1.1 (20KHz)	3.2 (80KHz)	4.9 (150KHz)	mA
Current limiting sensing voltage		640	685	730	mV
Temperature coefficient of current limiting		-	-	50	µV/°C
Soft/start duration	0 to 700mV	-	20	-	clock cycles
Leading edge blanking		200	-	450	ns
Thermal shutdown trip temperature	(on-chip sensing)	-	150	-	°C
Oscillator & PWM					
Range of nominal operating frequencies (Fno)		12	90	200	KHz
RBIAS values for above frequencies (see figure 4)					KΩ
Oscillator stability with supply & temperature (see figure 6)	I_{CC} = 1 to 10 mA Temp = 0 to 70°C	-	-	3	%
Maximum duty cycle	SYNC input = GND	-	25	-	%
Minimum duty cycle	SYNC input = GND	-	0	-	%
SYNC switching threshold			0.5		V
Width of Input SYNC *	(duration of SYNC high)	500			nsec

(*) see the SYNC IMPLEMENTATION section for more information

Error amplifier					
Sensitivity in mV / % of PWM	SYNC input = GND	-	50		millivolts per percent
Voltage for max duty cycle (On OPTO pin)	SYNC input = GND	-	4	-	V
Voltage for min duty cycle (On OPTO pin)	SYNC input = GND	-	0.5	-	V
Input Impedance (OPTO Pin)		-	60	-	KΩ
Threshold voltage to enter cycle skipping mode (OPTO Pin)	SYNC input = GND	-	1.25	-	V

ELECTRICAL CHARACTERISTICS (cont'd)

P & N Outputs to MOSFET gate	TEST CONDITIONS	PARAMETERS	UNITS		
PARAMETER	@ 25°C unless specified	MIN.	TYP.	MAX.	
Gate drive swing (PDRIVE)	10 mA (source)	-	-	1	V
Gate drive swing (NDRIVE)	10 mA (sink)	-	-	0.6	V
Gate pull-down resistor	(internal)	280	400	520	KΩ
PDRIVE Rise time (10% to 90%)	240 pF load	-	42	-	ns
NDRIVE Fall time (10% to 90%)	240 pF load	-	18	-	ns

Note: Electrical parameters, although guaranteed, are not all 100% tested in production.

Figure 4: Frequency vs Rbias

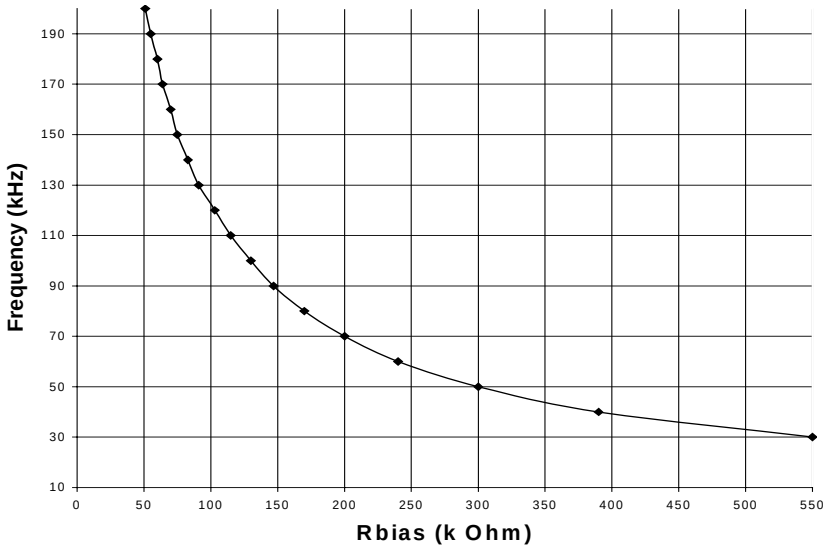


Figure 5: Shunt regulator Icc current

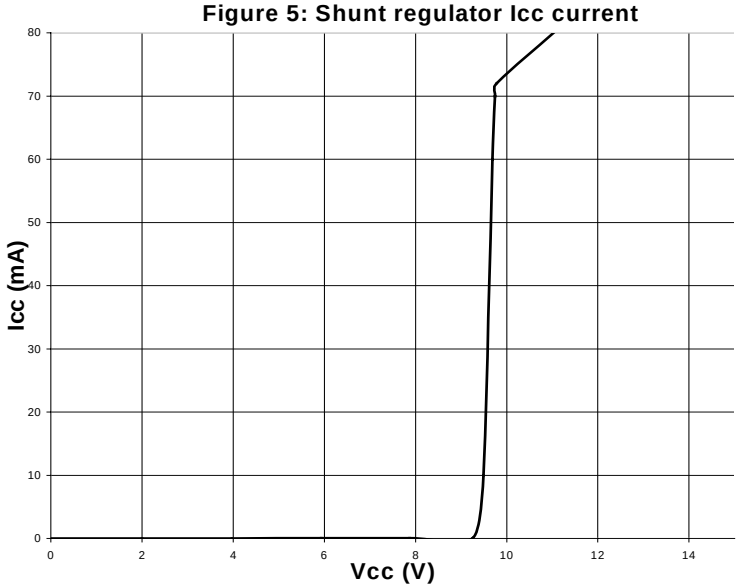
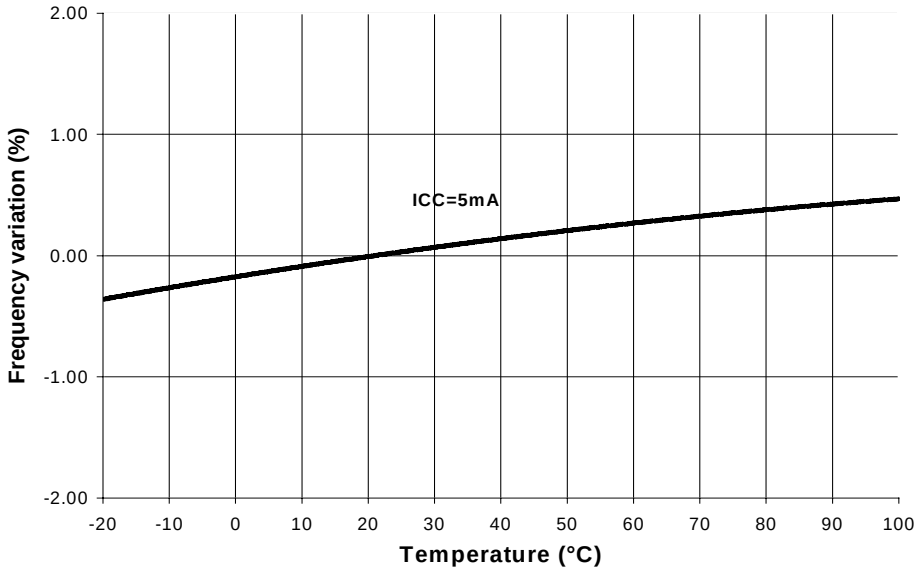


Figure 6 Frequency drift vs temperature



PATENTED SNUBBER NETWORK*:

AAI patented snubber network is the solution of choice to energize the IPS16 when the transformer doesn't have any bias winding or when the application requests a smaller or more cost-effective transformer. AAI patented snubber has been refined to both clamp the spikes that could damage the MOSFET and to derive the lost energy to supply the IPS16.

As shown below in figure 7, Rstart-up provides the start-up current for the chip that charges C2. Once the chip supply voltage is high enough, the gate drive starts and the chip is then powered by AAI's modified patented snubber network.

The snubber values may have to be optimized for the specific operating conditions:

- R1 could be reduced to 100 ohms and sometimes eliminated.
- C1 could be increased to 200pF and sometimes more.

For 20W or more applications, and depending on the characteristics of the transformer, essentially leakage inductance and distributed capacitance, the patented snubber has to be complemented by a second snubber or by a clamping diode to protect the MOSFET against very large spikes.

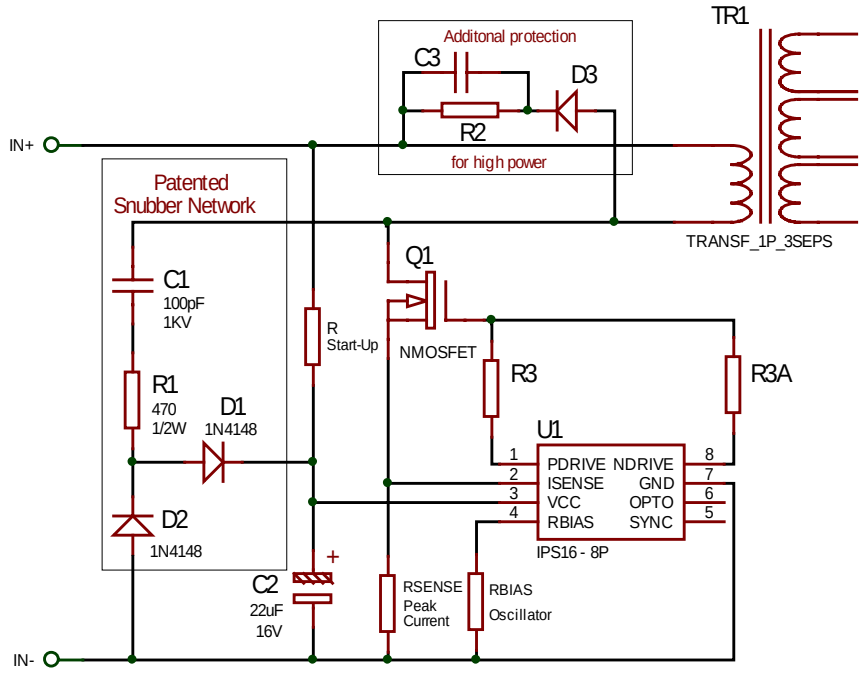


Figure 7

(*) US Patent # 6,233,165 by ASIC Advantage.

Optocoupler Feedback:

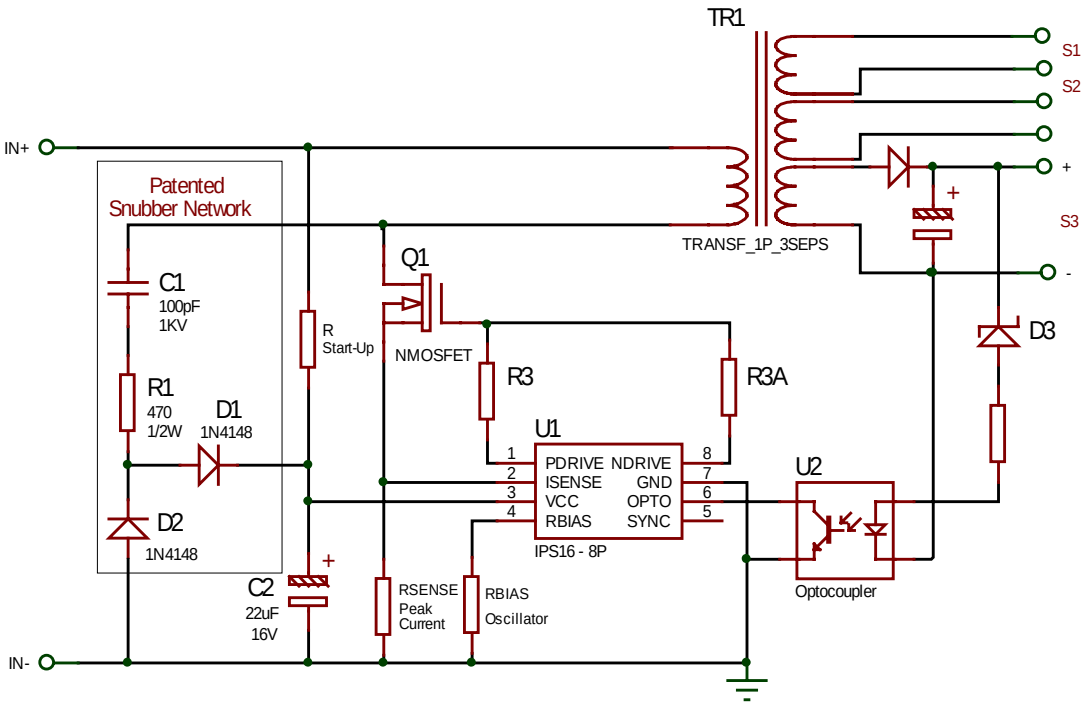


Figure 8

Bias winding feedback:

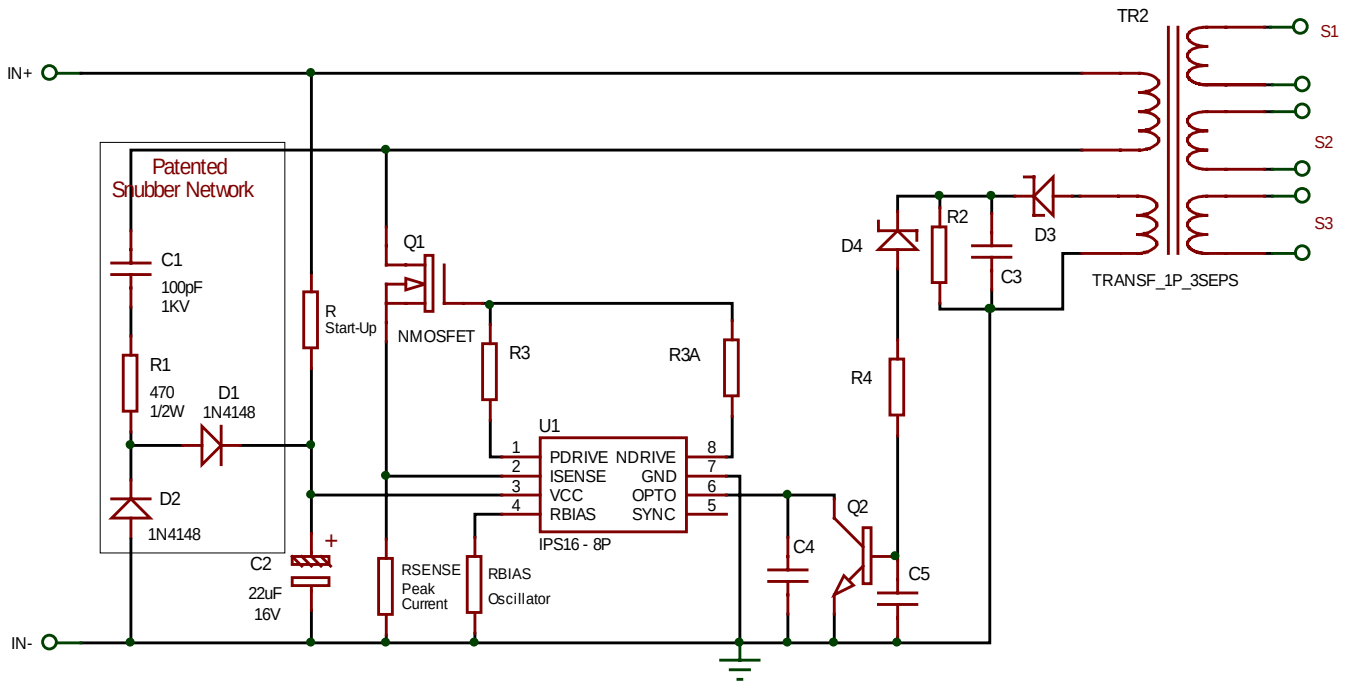


Figure 9

SYNC IMPLEMENTATION

TRANSFORMER ISOLATED SYNC

The application schematics in this datasheet show a direct-drive connection from the source of the sync pulse train to the IPS16. This implies that the IPS16 and the sync source are not galvanically isolated. An alternative approach is shown below. This uses a pulse transformer with capacitors on each side to eliminate and restore any DC offset. The example mentions a 3-to-1 turns ratio in the transformer. This is derived from the assumption of a sync source operating between 0 and 5 volts, and the SYNC pin threshold being approximately 0.5 volts. The choice of a seemingly low value of the capacitor connecting the transformer to the SYNC pin is intended to provide a pulse with a short duty cycle (a short duration in the high state) so as to allow as wide as possible duty cycle variation due to OPTO feedback, even if the duty cycle of the signal from the 5V driver is high (i.e. 50%). A pulldown resistor is shown from SYNC to GNDPRI to guarantee that in the absense of sync pulses that SYNC is pulled low (i.e. is 'off') and the IPS16 will operate in free-run mode at the frequency set by the resistor on the RBIAS pin.

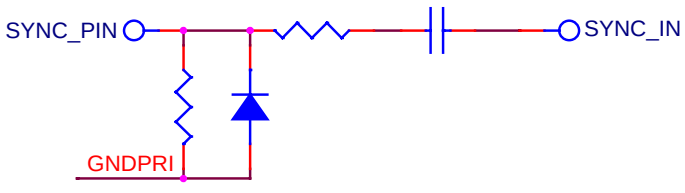


Figure 10 Non-isolated SYNC circuitry

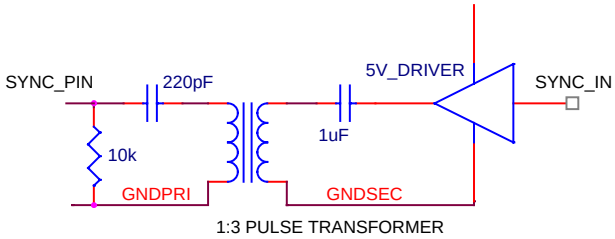


Figure 11 Isolated SYNC circuitry

GENERAL CONSIDERATIONS CONCERNING SYNC

It is important to realize that whenever the SYNC pin is high, the FET gate drive is low. The intended implementation of the drive to the SYNC pin is that it be a small duty cycle compared to duty cycle variation needed to compensate for changes in the input voltage and output load. Also be aware that the internal logic of the IPS16 is such that when the SYNC signal transitions from high to low, this is when the gate drive of the FET begins (i.e. goes from low to high). The signal to the SYNC pin needs to monotonically cross through the 0.5v swtiching threshold in both the rising and falling direction (no 'plateaus' or 'reversals') to ensure a stable gate drive signal.

The intended approach to implementation is that the free-running (SYNC pin held continuously low) frequency set by the RBIAS resistor should be lower than the frequency of the SYNC signal. Another way of saying this is: the SYNC signal can only increase the operating frequency above the free running frequency (it can't decrease it). During startup the duty cycle is controlled by the internal soft start circuitry until the OPTO signal begins to take charge of the feedback loop. Also, the cycle-skipping feature is disabled in the presence of SYNC pulses. In all cases, if the ISENSE pin reaches 700 millivolts or greater, the gate drive is turned off (to provide cycle-by-cycle current limiting and overpower protection to the FET and the rest of the power supply).

To stay in the useful operating range of the internal PWM circuit (running off a comparison of the oscillator/SYNC and the OPTO pins) it is suggested that the ratio of the SYNC frequency to the free running frequency should not exceed a factor of 5. Similiarly, due to internal delays in the chip and the minimum pulse width of the SYNC signal, the maximum useful SYNC frequency is about 300kHz. This is similar to the maximum operating frequency of other members of the IPS1x family.

GOOD DESIGN PRACTICES

IPS16 and loop stability:

The IPS16 is intrinsically very fast and doesn't participate to the loop stability. It only involves a comparator that doesn't bring any gain and exhibits a negligible phase shift.
It has been designed on purpose to allow its utilization in a large range of applications:
(a) Operating at frequencies up to 200 kHz and above,
(b) Involving very different types of loop stability from "cycle skipping" where the loop is not compensated at all, to good stability achieved through the utilization of a TL431 and finally superior transient response when using half of the IPS25 feedback controller.
The loop compensation is entirely achieved on the load side and the feedback is performed by an optocoupler which gain and dynamic response play an important role in the loop stability.

Precaution in selecting the optocoupler:

The optocoupler must be **using a Phototransistor** and **NOT** a Photodarlington. Most optocouplers of this type are offered in a wide range of coupling efficiency, also called current transfer ratio (CTR). Even the cheapest ones have a guaranteed transfer ratio of the order of 100% meaning that 1mA of current in the IR LED creates approximately 1mA of current in the receiving phototransistor. The user should be able to design the loop to be stable even though the actual transfer ratio differs by more than a factor of 3 (example from 100% to 300% or 50% to 150%).
Unfortunately optocouplers were not designed for low-current applications and this results in very bad speed and saturation characteristics for the phototransistor which could become incredibly slow and create severe loop stability problems should it be allowed to saturate hard in the application (the optocoupler could cause the IPS16 to skip cycles due to the long time required by the opto transistor to go out of saturation).
Using the example in figure 12, the OPTO pin electrically looks like a 5 volt source in series with a 50k. This means that the maximum current needed to pull down the OPTO pin is about 100 microamps. If the optoisolator in this example is assumed to have a 25% CTR (current transfer ratio) at this output current, then the current through the secondary side photo diode will be a maximum of 400 microamps. The voltage drop across the photodiode will be

about 1 volt, and the voltage across the 2.2k resistor R9 will be 0.4 milliamps x 2.2k = 0.88 volts. This means the current through the 'bypass' resistor R8 will be 0.88 volts / 1k = 0.88 milliamps, and the current though the TL431 will be 0.4 + 0.88 = 1.28 milliamps. This exceeds the specified 1.0 milliamp datasheet minimum shunt current for the TL431, so the implementation should operate reasonably.
Note that the output voltage is 12 volts as defined by R6 and R7 and 2.5V at the Pin #1 of the TL431.

Loop stability with the TL431:

The TL431 has an enormous DC gain and will not ensure stability unless specific loop-compensation components such as a RC network are added as indicated below.

The RC network should have a cut-off frequency at 100Hz to roll-off the gain at low frequencies but **reach a plateau around 100Hz** and have enough AC gain at twice the line frequency and achieve a good line ripple rejection.
This is achieved by the loop compensation network **C24, R6** of figure 1. The gain rolls off until the impedance of C24 reaches the value of R6. At much higher frequencies, the gain continue to roll-off due to the natural frequency response of the TL431.
The goal is to reach a very low gain at the switching frequency.

If the addition of C24 & R6 with values as shown results in gain is too low, the values of R6 & R7 should be reduced in proportion to lower the impedance at Pin #1 of TL 431. Alternately, if the gain is too high the values of R6 should be reduced and C9 re-adjusted accordingly to maintain the required cut-off frequency.
Criteria to calculate the network :
1) R6 must be much higher than the input resistance of TL431 constituted by R6//R7=5K → 23Kohm OK.
2) F=100Hz=1/(2 x 3.14 x R6 x C24) gives approximately 68,000 pF for C24.

Discontinuous operation:

Check discontinuous mode of operation of the transformer (see application note AN-IPS02 page 2 for details) to ensure that the Flyback SMPS is indeed operating in discontinuous mode in the entire range of Input Voltages and Output Current. The response of the SMPS drastically changes in continuous mode, it gets considerably slower which requires a totally different loop compensation technique. Remember that it is very difficult to ensure loop stability with a simple schematic when the SMPS is allowed to transition between Discontinuous and Continuous modes.

MOSFET driver protection:

The MOSFET driver has been sized to be capable of driving power MOSFETs featuring a total gate charge up to 100nC.
The MOSFET should be turned-on relatively slowly and turned-off much faster. These 2 parameters can be independently adjusted through the external resistors R10 (pin1) and R10A (pin8) (see figure 1).
The minimum value of these resistors should be 50Ω in order to reduce EMI and minimize the noise injection which could result from Miller-capacitance kick-back during transient conditions.
See application note AN-IPS-02 for EMI reduction techniques.

ADDITIONAL RECOMMENDATIONS:

For best results in low power off-line SMPSs with the **IPS16**, the following MOSFET features are recommended:

- Low gate charge (max 50 nC).
- 400 V breakdown voltage for domestic use (USA / Japan).
- 600V breakdown voltage for European use (800V when transformer leakage inductance is very small).
- 1, 2 or 3A depending on the maximum output power.

Examples of suitable MOSFETS:

- **IXYS PolarHT™ and Polar HV™** MOSFET series: IXTY1R4N60P, IXTY2N60P, IXTY3N60P
- **Fairchild** MOSFET series: FQPF1N60, FQPF 2N60, FQPF 3N60.
- **Infineon COOLMOS™** series: SPD01N60S5, SPD02N60S5, SPD03N60S5.
- **Motorola** MOSFET series: MTP1N60, MTP2N60, MTP3N60.
- **SGS-Thomson** MOSFET series: STD1NB60, STD2NB60, STD3NB60.
- **Etc…**

Notes:

- Due to the rapid evolution of MOSFET technologies, please check for current models when designing a new SMPS.
- **PolarHT™ and Polar HV™** are trademarks of IXYS corporation
- **COOLMOS™** is a trademark of Infineon.

TRANSFORMER CHARACTERISTICS:

(a) Transformer design:

E-core with suitable gap to prevent saturation or distributed-gap toroid. Primary inductance of 1.5 mH is very typical in 5 -10W applications with 5V output DC:
Turn ratio = 9 for 220V input or universal 85V – 265V.
Turn ratio = 7 for 100-120V AC input (Japan and USA)

(b) Transformer phasing:

Check the phase indicated in figure 1. Also refer to applications notes AN-IPS-01 and AN-IPS-02.

SNUBBER NETWORK:

With reference to figure 7, Rstart-up provides the start-up current for the chip. C2 is being charged through Rstart-up. Once the chip supply voltage is high enough, the gate drive starts and the chip is then powered by the patented snubber network.
The snubber values may have to be optimized for different specific operating conditions:

- R1 could be reduced to 100 ohms and sometimes eliminated.
- C1 could be increased to 200pF and sometimes more.

Depending on the characteristics of the transformer, essentially leakage inductance and distributed capacitance, the snubber network shown in figure 1, may not be efficient enough to reduce the voltage spikes when operating at 20W or above. Please refer to applications notes AN-IPS-01 and AN-IPS-02 design tips or EMI reduction techniques, or feel free to contact our technical support for assistance.

POWER SHUT-DOWN SOLUTIONS for STAND-BY REQUIREMENTS:

For low-power stand-by requirements, the primary circuitry can be shut-down by pulling the IPS16 VCC pin "LOW" through a 100Ω resistor.
This can be easily done using a:

- Simple switch
- PNP transistor
- NPN transistor

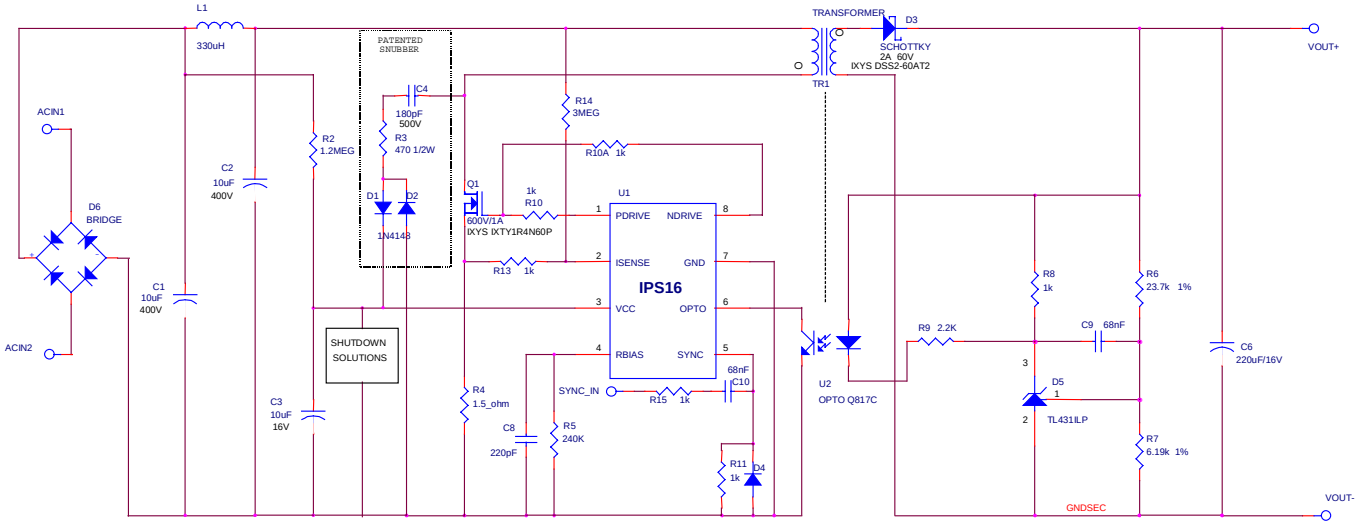
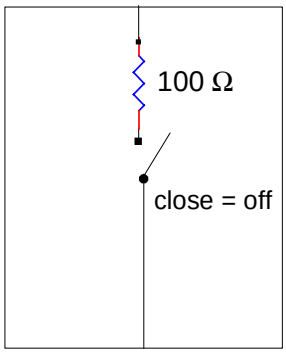


Figure 12

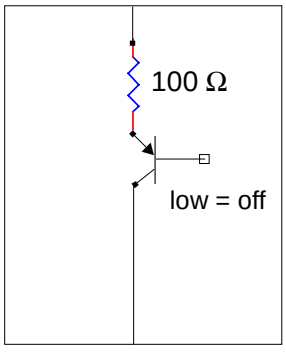
SHUT-DOWN SOLUTIONS:

When the "LOW" state is released, the VCC is naturally re-established, re-activating the IPS16.

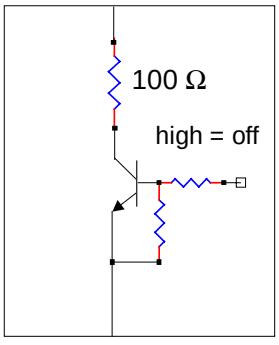
Solution 1:
simple switch, close = off
100Ω resistor
mandatory



Solution 2:
PNP transistor, low = off
(low = less than 4V)
100Ω resistor
optional

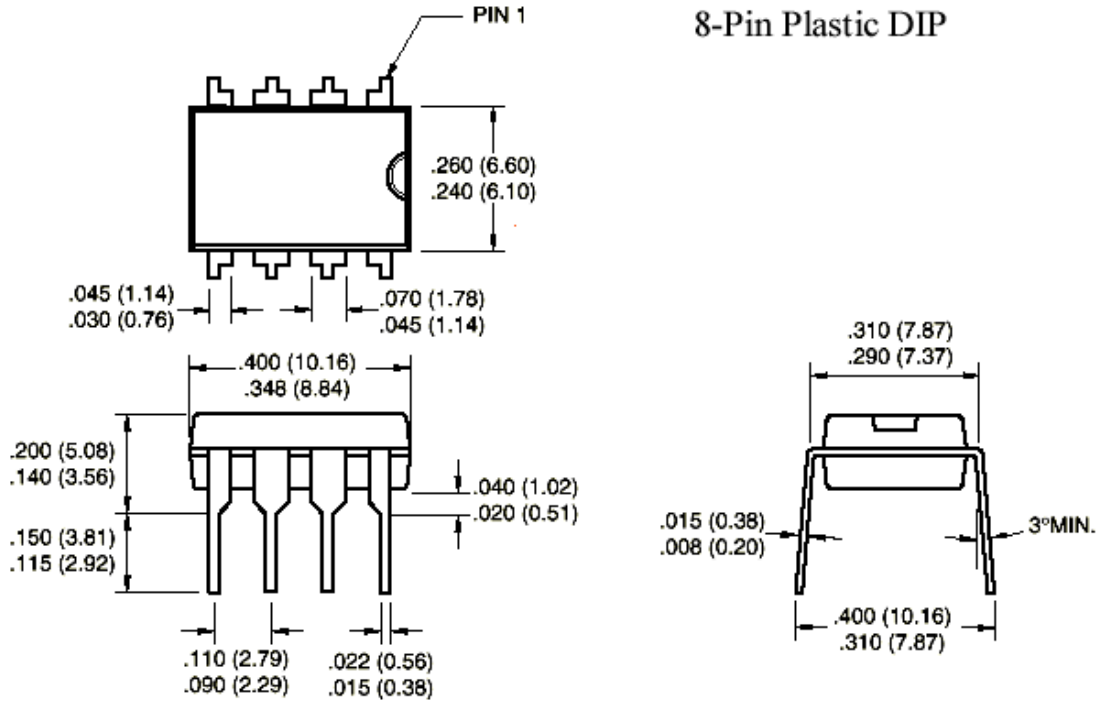


Solution 3:
NPN transistor, high = off
100Ω resistor
optional

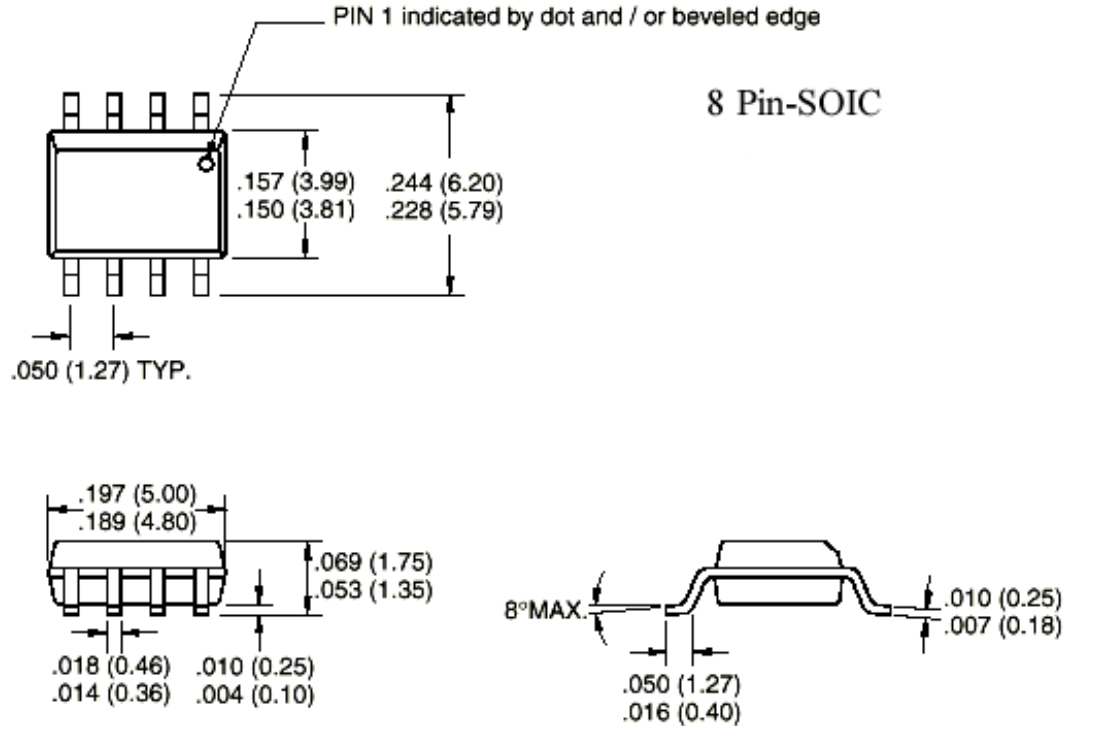


PACKAGE DIMENSIONS

PLASTIC DIP-8



PLASTIC SOIC-8



ORDERING INFORMATION

Part-Number

IPS XXXH C – YY – G-LF - TR

IN-PLUG® Controller Series

Flyback
Feedback
PFC
Push-Pull
LED Driver

Controller Type

Flyback: 10 series
Feedback: 20 series
PFC: 100 series
Push-Pull: 200 series
Automotive: 300 series
LED Driver: 400 series
"H" with hiccup overload protection

Tape and Reel

TR : Tape & Reel
TU : Tube
Note1 : Default or not specified is « tube ».
Note2 : Does not appear on package marking.

ROHS + Pb-Free

Package Type

D : DIP8
SO : SOIC8
(For production with a new date code, since January 2006, the package type does not appear anymore on package marking)

Temperature Range

C : Commercial (0, +70°C)
I : Industrial (-40°C. +85°C)
A: Automotive (-40°C. +125°C)
Note : Default or not specified is <commercial>

Example of Marking

Non-Green Package

Green ROHS + Pb-Free Package

(Note : For production with a new date code, since January 2006, the package type does not appear anymore on package marking)

This ordering information is for commercial and industrial standard IN-PLUG® controllers ONLY. For custom controllers or for military temperature range, call AAI's sales representative.

The following is a brief overview of certain terms and conditions of sale of product. For a full and complete copy of all the General Terms and Conditions of Sale, visit our webpage http://www.asicadvantage.com/terms.htm.

LIMITED WARRANTY

The product is warranted that it will conform to the applicable specifications and be free of defects for one year. Buyer is responsible for selection of, use of and results obtained from use of the product. Buyer indemnifies and holds ASIC Advantage, Inc. harmless for claims arising out of the application of ASIC Advantage, Inc.'s products to Buyer's designs. Applications described herein or in any catalogs, advertisements or other documents are for illustrative purposes only.

CRITICAL APPLICATIONS

Products are not authorized for use in critical applications including aerospace and life support applications. Use of products in these applications is fully at the risk of the Buyer. Critical applications include any system or device whose failure to perform can result in significant injury to the user.

LETHAL VOLTAGES

Lethal voltages could be present in the applications. Please comply with all applicable safety regulations.

INTELLECTUAL PROPERTY RIGHTS AND PROPRIETARY DATA

ASIC Advantage, Inc. retains all intellectual property rights in the products. Sale of products does not confer on Buyer any license to the intellectual property. ASIC Advantage, Inc. reserves the right to make changes without notice to the products at any time. Buyer agrees not to use or disclose ASIC Advantage Inc.'s proprietary information without written consent.

TRADEMARKS AND PATENTS

- IN-PLUG® is a registered trademark of ASIC Advantage, Inc.
- AAI's modified snubber network is patented under the US Patent # 6,233,165. IN-PLUG® Customers are granted a royalty-free licence for its utilization, provision the parts are purchased factory direct or from an authorized agent.

PROTECTION FOR CUSTOM IN-PLUG® SOLUTIONS

When AAI accepts to design and manufacture IN-PLUG® products to Buyer's designs or specifications, buyer has certain obligations to provide defense in a suit or proceeding claiming infringement of a patent, copyright or trademark or for misappropriation of use of any trade secrets or for unfair competition.

COMPLIANCE WITH LAWS

Buyer agrees that at all times it will comply with all applicable federal, state, municipal, and local laws, orders and regulations. Buyer agrees to comply with all applicable restrictions on exports and re-exports including obtaining any required U.S. Government license, authorization, or approval. Buyer shall pay any duties, levies, taxes, brokerage fees, or customs fees imposed on the products.

TITLE AND DELIVERY

All shipments of goods shall be delivered ExWorks, Sunnyvale, CA, U.S.A. Title in the goods shall not pass to Buyer until ASIC Advantage, Inc. has received in full all amounts owed by Buyer.

LATEST DATASHEET UPDATES

For the latest datasheet updates, visit our web page: http://www.in-plug.com/datasheets.htm.

WORLDWIDE REPRESENTATIVES

To access AAI's list of worldwide representatives , visit our web page http://www.in-plug.com/representatives.htm

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