AAC142, AAC143, AAC242, AAC243, AAC1042, AAC1043, AAC1042 AND AAC2043 CURRENT MODE PWM CONTROLLER

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SUMMARY

This application note regards the use and application of the AACx42/AACx43 series of current mode PWM controllers. This series of controller is similar to XX3842 series in general use but with improved features and characteristics.

REFERENCE

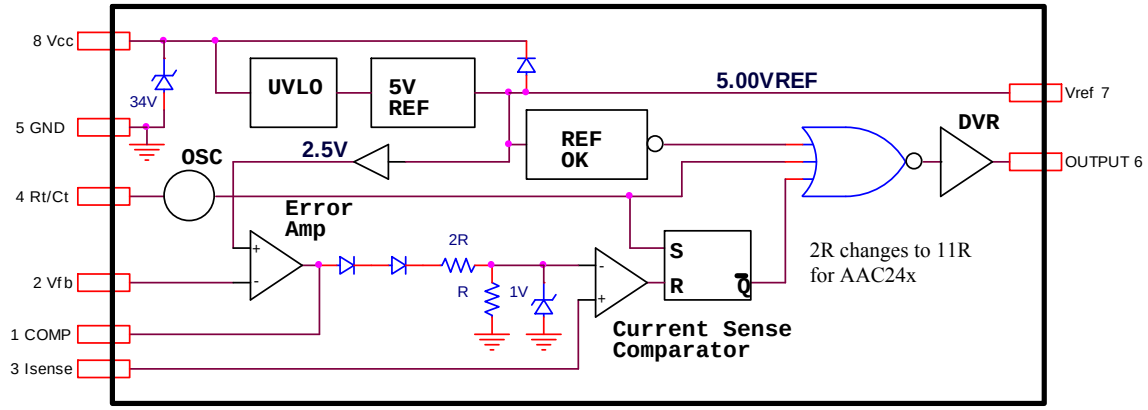
1. AAC142/143/242/243 Datasheet (available from www.asicadvantage.com)
2. AAC1042/1043/2042/2043 Datasheet (available from www.asicadvantage.com)
3. AAC142 Evaluation board (Available from AAI Marketing to qualified customers)

OVERVIEW

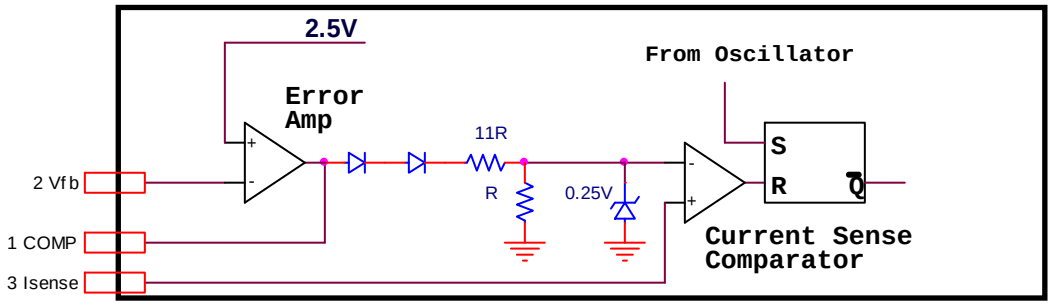
The AAI AACx42/x43 current mode PWM controllers can be used in a variety of configurations including Buck, Boost, Flyback, and Forward converters. Improvement over the original 3842 include Leading Edge Blanking, faster over-current sensing, better switching times, and lower power operation. The function block diagram for this series is shown in Figure 1(a).

Another improvement is included in the AAC242 and AAC243. These controllers have a lower current sense voltage range which reduces the power dissipation in the current sense resistor. This feature helps in improving converter efficiencies related to the current sense resistor by a factor of 4 from the standard 1 Volt range.
The AAC10xx and AAC20xx series include a depletion mode MOSFET for directly powering the controller during startup. The MOSFET is turned off when the Vcc is greater than the preset upper startup voltage point.

The controller contains a band gap reference which is trimmed to 5.0 ±0.1V. This reference is available externally on pin 8. Internally the 5V reference is scales to 2.5V and used as the reference input to the loop error amplifier. An oscillator is provided which uses an external resistor and capacitor to set the frequency and determine the dead time. The output of the error amplifier is offset by two diode drops and then divided by three (by 12 for ACC24x series) to provide the reference input to the PWM comparator. An under voltage lockout circuit is provided to ensure sufficient voltage is available to drive an external MOSFET.



(a)



(b)

Figure 1(a). AAC1x4x/2x4x Block Diagram.

The output pulse is formed from the combination of the oscillator start pulse and a termination pulse from the peak current comparator. The oscillator generates a narrow pulse related to the dead time which set a flip-flop and turns off the output for the width of the pulse. The flip-flop is reset when the current comparator output is high. The high occurs when the external current signal exceeds the error amplifier's scaled output.

If the under voltage lockout is qualified, then the oscillator pulse sets the flip-flop and the output of the driver goes high. The driver will stay high until the current sense comparator is triggered or the end of the on time from the oscillator. When the comparator triggers, the flip-flop is reset and the output is driven low. If the current does not exceed the error signal, the oscillator will provide a pulse to turn the output off for the dead time period.

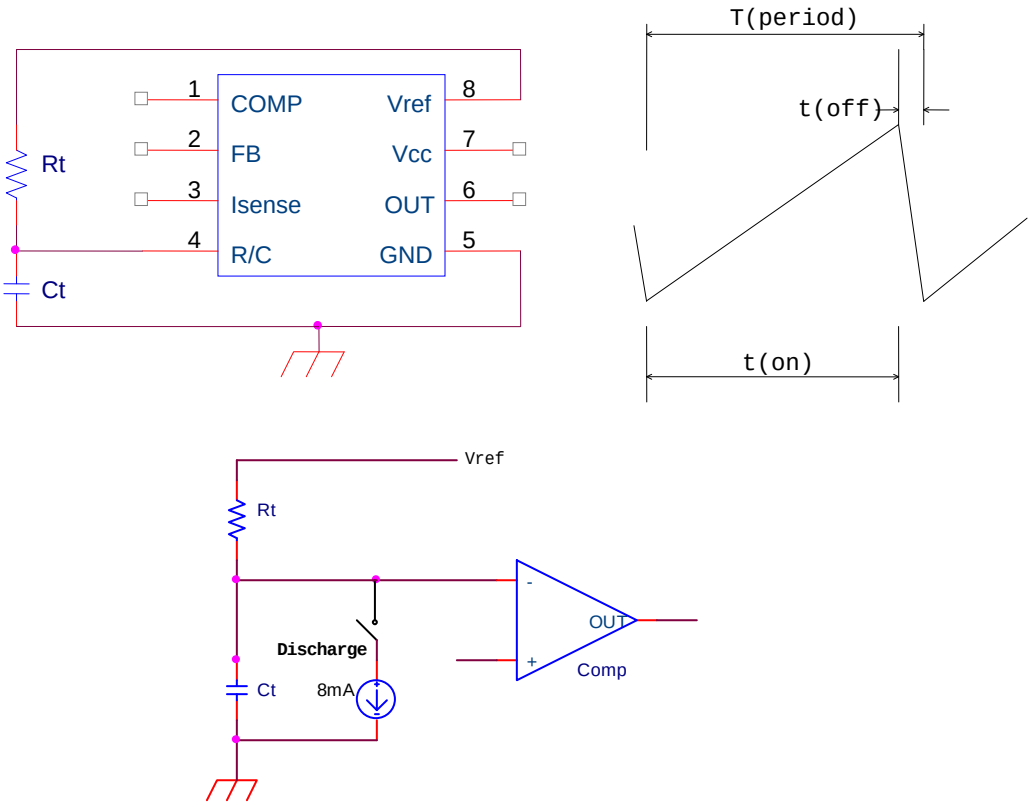


Figure 2. Oscillator Operation

Figure 2 shows the external components and the waveforms for the oscillator. The timing capacitor Ct is charged through Rt until an upper threshold is exceeded. This causes a reset pulse of 8.4mA to discharge the timing capacitor to a low threshold. The oscillator then starts the cycle over again. The overall period, t(period) is the total of t(on) and t(off). Dead time or t(off) can be set by selecting a capacitance value. As the capacitance value Ct is increased, the dead time is increased. The t(on) time is set by selecting a resistor value to charge the Ct already determined by the selection of Ct for the dead time. Figures 3 and 4 show the relationships between Rt and Ct for the oscillator. Rt should be in the range of 3k to 100K Ohms for best results. Capacitors greater than a few nf should be avoided.

Charge and discharge times are given by the following formulas:

$$T_C = 0.55 R_t C_t$$

$$T_D = R_t C_t \mathrm{Ln}[(0.0063R_t - 2.7)/(0.0063R_t - 4)]$$

$$\text{Frequency} = (T_C + T_D)^{-1}$$

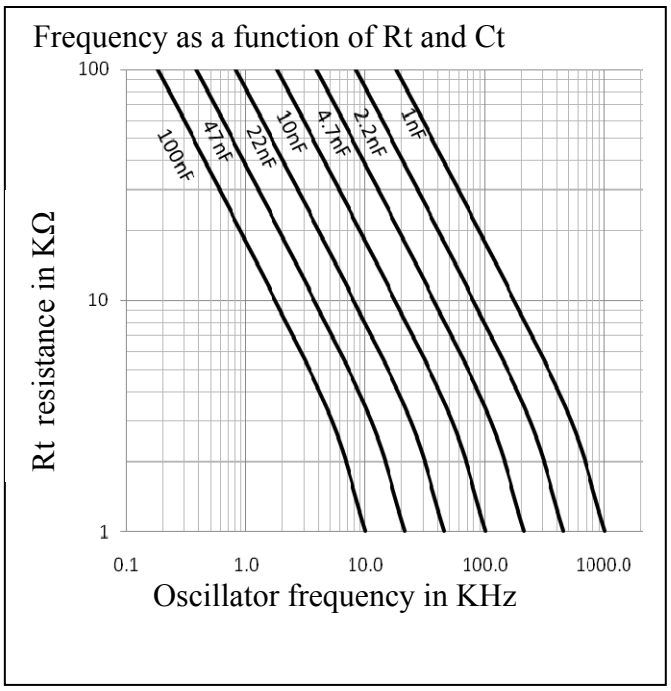


Figure 3. Oscillator Frequency verse Rt and Ct

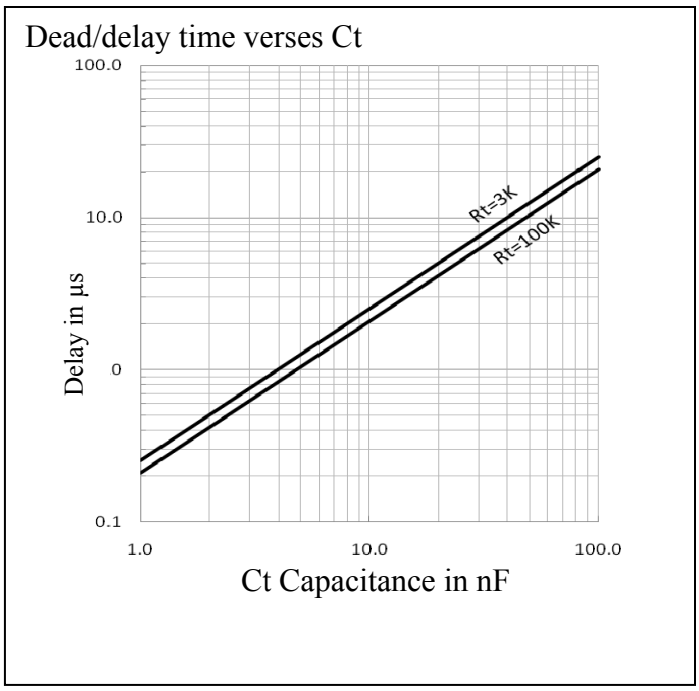


Figure 4. Dead time verses Ct

Leading edge blanking is included in the design but if the turn on transient is not completely eliminated, additional filtering can be added as shown in Figure 5.

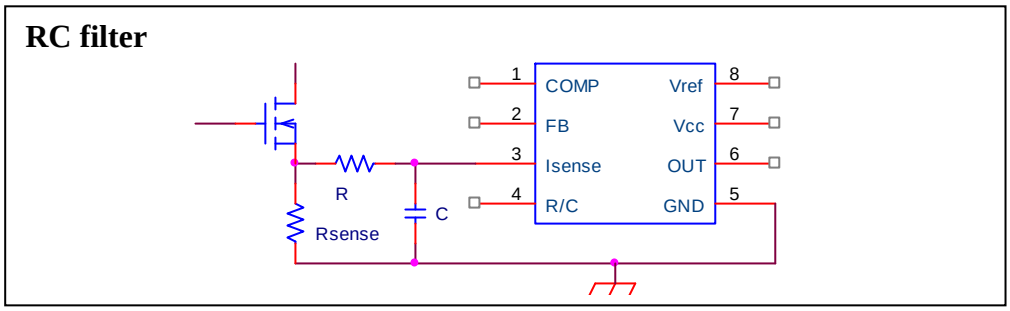


Figure 5. Filtering of Rsense signal

Peak current is set by the internal comparator with a fixed limit of 1V (0.25V for AAC24x). Raising the current sense pin (3) to 1V or higher (0.25V for AAC24x) will cause a termination of the output pulse regardless of the error amplifier output. The peak current is normally determined when the current sense pin exceeds the error amplifier conditioned output. Peak current is determined by the formula:

$\mathbf{I_{SENSE(PK)} = 1.0V/R_S}$ for AAC14x

$\mathbf{I_{SENSE(PK)} = 0.25V/R_S}$ for AAC24x

Peak current control requires slope compensation when duty cycle exceeds 50%. This can be added by using a circuit as shown in Figure 6. This can be implemented by adding a buffer transistor to the oscillator circuit and using a resistive summing circuit to provide the ramp necessary for slope compensation.

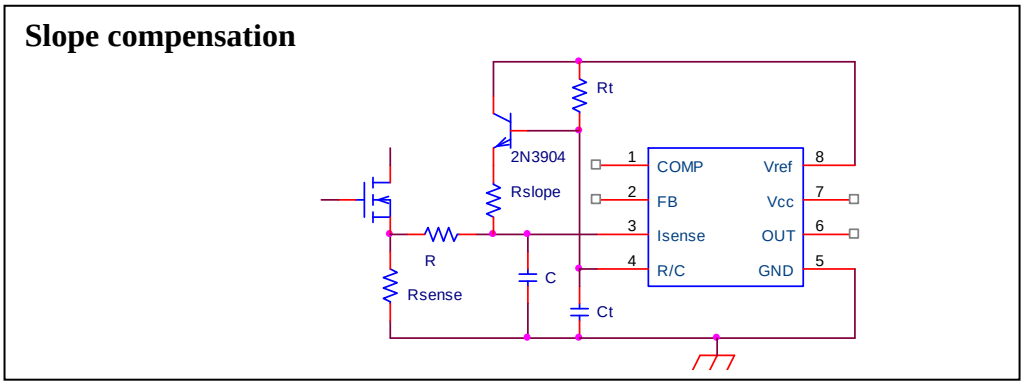


Figure 6. Adding Slope Compensation

Enable can be added to the controller by using circuits shown in Figure 7. The circuit in 7(a) is an on/off control without latching. The circuit in Figure 7(b) latches off the operation of the controller. Latched operation is normally used for fault conditions which require a full cycling of power to the supply to reset the latch.

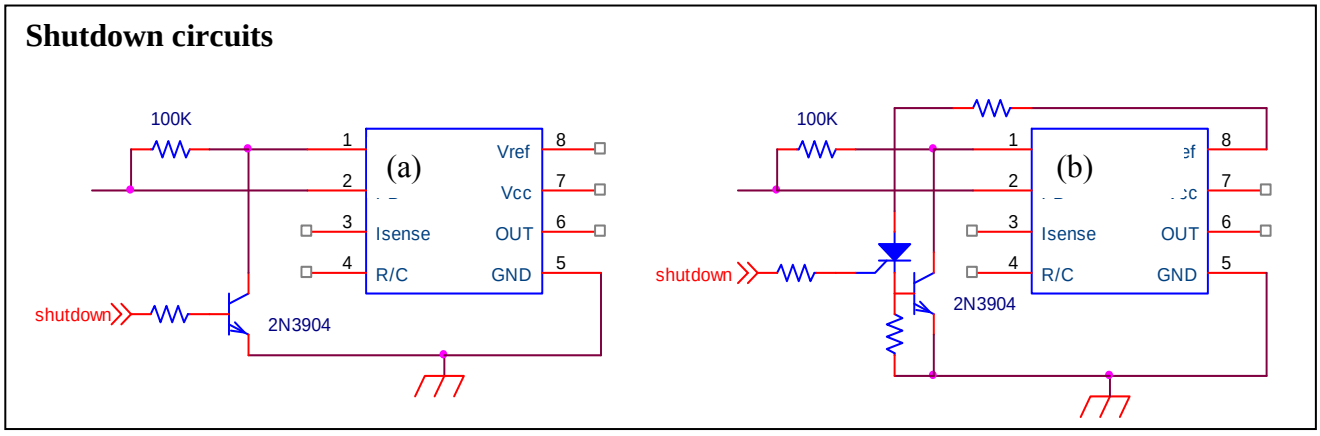


Figure 7. Shutdown circuits, (a) is a non-latching on/off control, (b) is a latching on/off control.

In applications where several controllers are used, it may be desirable to synchronize the operating frequency. This can be done using the technique shown in Figure 8. A narrow pulse is added into the timing circuit which will cause the oscillator positive threshold to be exceeded and forcing the start of a new cycle. To use this synchronization, all the oscillators should be set to a slightly lower frequency than the desired operation frequency. The synchronization pulse can only increase frequency. The value of

the resistor can be changed depending on the driving source but should be selected with the reset pulse being about 8mA.

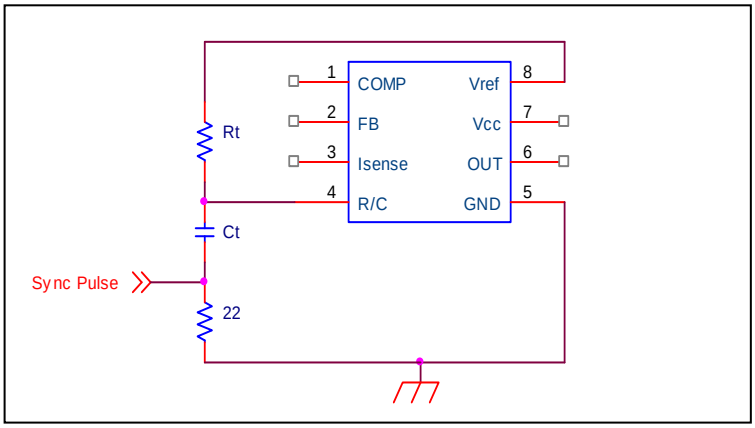


Figure 8. Synchronization of oscillators.