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Total Ionizing Dose Test Report

No. 22T-RT4G150-LG1657- K7RAS

February 15, 2022

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I. SUMMARY TABLE

Table. 1. Summary

Parameter	Tolerance
1. Gross Functionality	Passed 125 krad(SiO_2)
2. Power Supply Current	Passed 125 krad(SiO_2)
3. Input Threshold (VIL/VIH)	Passed 125 krad(SiO_2)
4. Output Drive (VOL/VOH)	Passed 125 krad(SiO_2)
5. Propagation Delay	Passed 125 krad(SiO_2) for 10% degradation criterion
6. Transition Time	Passed 125 krad(SiO_2)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-Tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports

Electrical parameters are measured pre-irradiation and post-irradiation using the burn in design and the Automatic Test Equipment (ATE) program. The report summarizes sample pins.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters.

Table. 2. DUT and Irradiation Parameters

Part Number	RT4G150
Package	LG1657
Foundry	United Microelectronics Corp.
Technology	65 nm
DUT Design	Burn in design with inverter string
Die Lot Number	K7RAS
Quantity Tested	6
Serial Number (Dose)	02937 (125 krad), 02963 (125 krad), 03018 (125 krad), 03020 (125 krad), 03032 (125 krad), 03043 (125 krad)
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias	Static at 1.2V/2.5V/3.3V/3.3V
IO Configuration	Single ended Differential Pair

B. Test Method

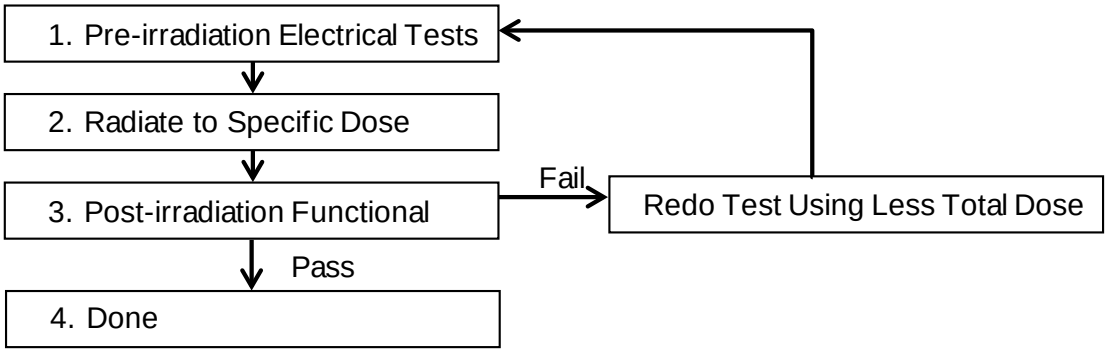

Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre and post-irradiation.

Fabric functionality coverage performed by the burn in design is summarized in table 2 below. In addition to the fabric coverage the supplemental test of propagation delay is also used to determine DUT functionality. These tests are performed pre and post-irradiation and recorded as a pass/fail.

Refer to appendix A for a graphical representation of fabric functional coverage blocks used to perform the functional tests.

Table. 3. Fabric Functional Coverage

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	Maximum output toggle rate(checker board) compared to reference
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
I/O Block	I/O utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

The core power supply current IDD, the I/Os power supply currents (IDDI_2.5/IDDI_3.3) and the charge pump and PLL power supply current (IPP_PLL) are also monitored during irradiation in real time.

The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential inputs, and is reported as a pass or fail, as part of the ATE test program. The output-drive voltage (VOL/VOH) is also measured on all pins on the MSIO MSIOD and DDRIO. This report contains the output-drive voltage measurements on selected IO pins used in the burn in design. LVTTL and LVCMOS 2.5V standard at different sourcing and sinking currents are reported.

A 2000 stage inverter string is used to measure the propagation delay. The propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. The propagation delay is monitored real time during irradiation and the time difference between positive switching edges of the clock and output are reported. Additionally, the transition characteristics (rise and fall) at the output of the inverter chain are measured pre and post-irradiation. Oscilloscope screen captures are shown in section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests mentioned in section II.C.

B. Power Supply Current

The core power supply current (IDD) is 1.2 V, the I/O bank power supply currents (IDDI) are 2.5 V (IDDI_2.5) and 3.3 V (IDDI_3.3). The charge pump and PLL power supply current (IPP_PLL) is 3.3 V. Figures 2-25 illustrate the plot of in-flux standby IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL versus total dose for every DUT. Tables 3-6 summarize the pre-irradiation and post-irradiation total current (static & dynamic) IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL.

Table. 4. Pre-irradiation and Post-irradiation I_{DD}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
02937	125 krad	0.3455	0.3650	5.64
02963	125 krad	0.3870	0.3962	2.38
03018	125 krad	0.2932	0.3133	6.86
03020	125 krad	0.3166	0.3320	4.86
03032	125 krad	0.3218	0.3398	5.59
03043	125 krad	0.3618	0.3695	2.13

Table. 5. Pre-irradiation and Post-irradiation $I_{DDI\_2.5}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
02937	125 krad	0.0105	0.0124	18.10
02963	125 krad	0.0110	0.0124	12.73
03018	125 krad	0.0098	0.0113	15.31
03020	125 krad	0.0093	0.0114	22.58
03032	125 krad	0.0096	0.0118	22.92
03043	125 krad	0.0093	0.0111	19.35

Table. 6. Pre-irradiation and Post-irradiation $I_{DDI\_3.3}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
02937	125 krad	0.0352	0.0378	7.39
02963	125 krad	0.0350	0.0381	8.86
03018	125 krad	0.0340	0.0367	7.94
03020	125 krad	0.0341	0.0383	12.32
03032	125 krad	0.0345	0.0376	8.99
03043	125 krad	0.0341	0.0368	7.92

Table. 7. Pre-irradiation and Post-irradiation I_{PP_PLL}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
02937	125 krad	0.0156	0.0170	8.97
02963	125 krad	0.0155	0.0162	4.52
03018	125 krad	0.0156	0.0161	3.21
03020	125 krad	0.0157	0.0180	14.65
03032	125 krad	0.0156	0.0168	7.69
03043	125 krad	0.0155	0.0154	-0.65

The following figures (2-25) show the in-beam monitoring of the currents mentioned above as a function of TID for the available DUTs.

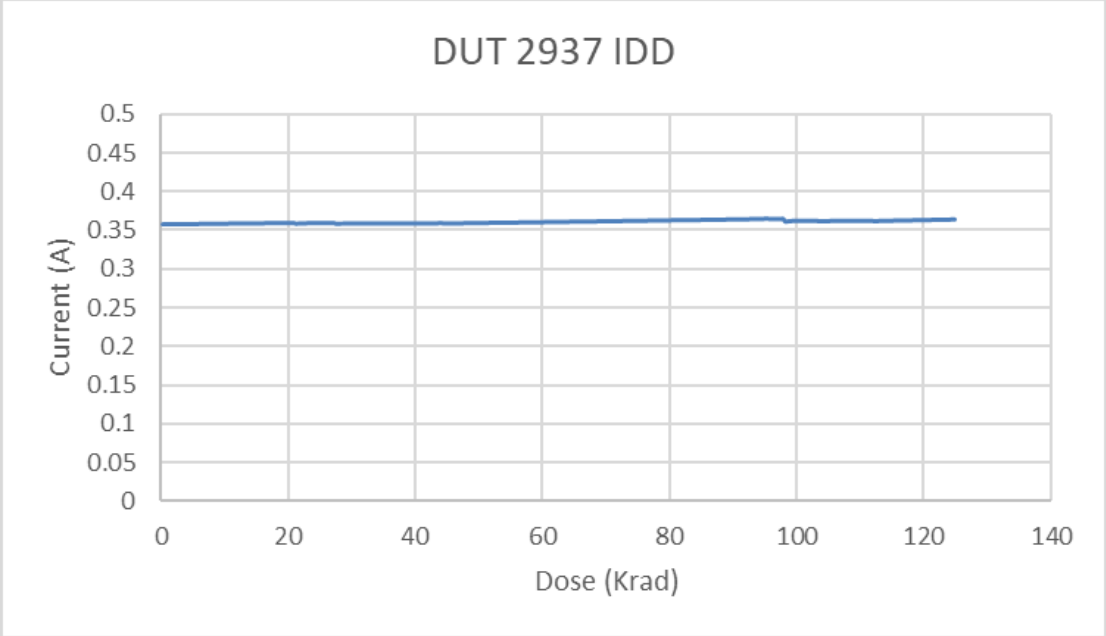

Fig. 2. DUT 02937 core power supply current (I_{DD}) versus TID

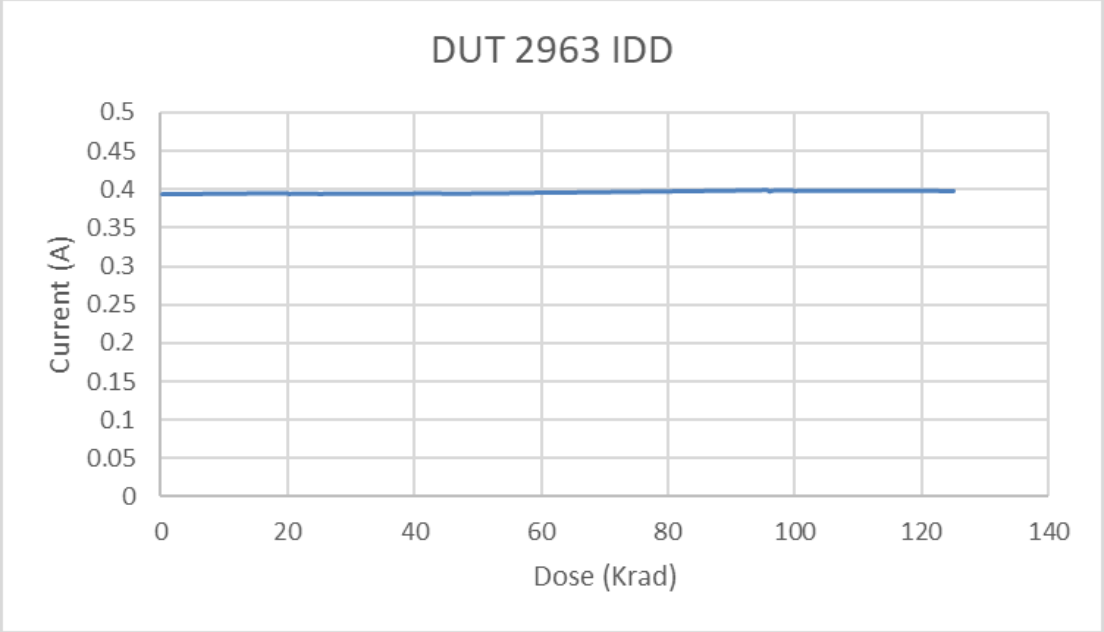

Fig. 3. DUT 02963 core power supply current (I_{DD}) versus TID

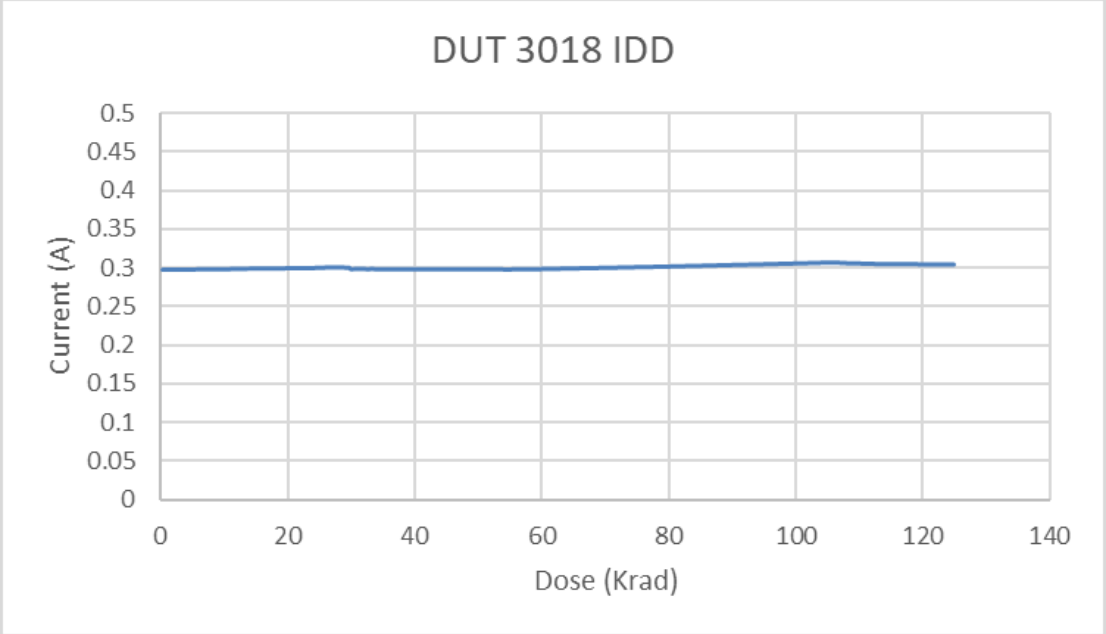

Fig. 4. DUT 03018 core power supply current (I_{DD}) versus TID

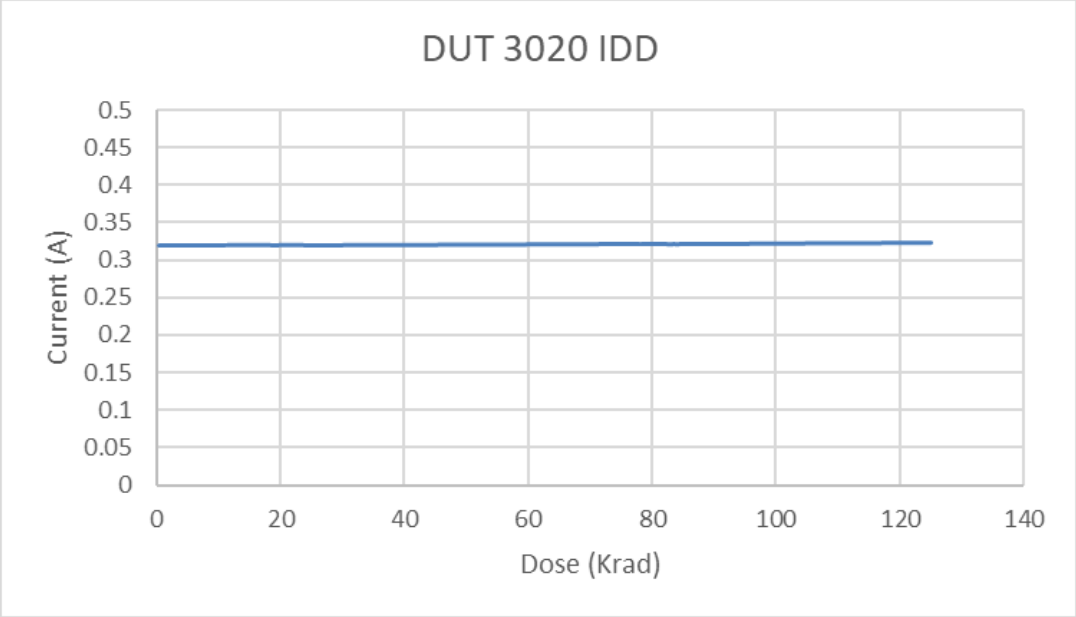

Fig. 5. DUT 03020 core power supply current (I_{DD}) versus TID

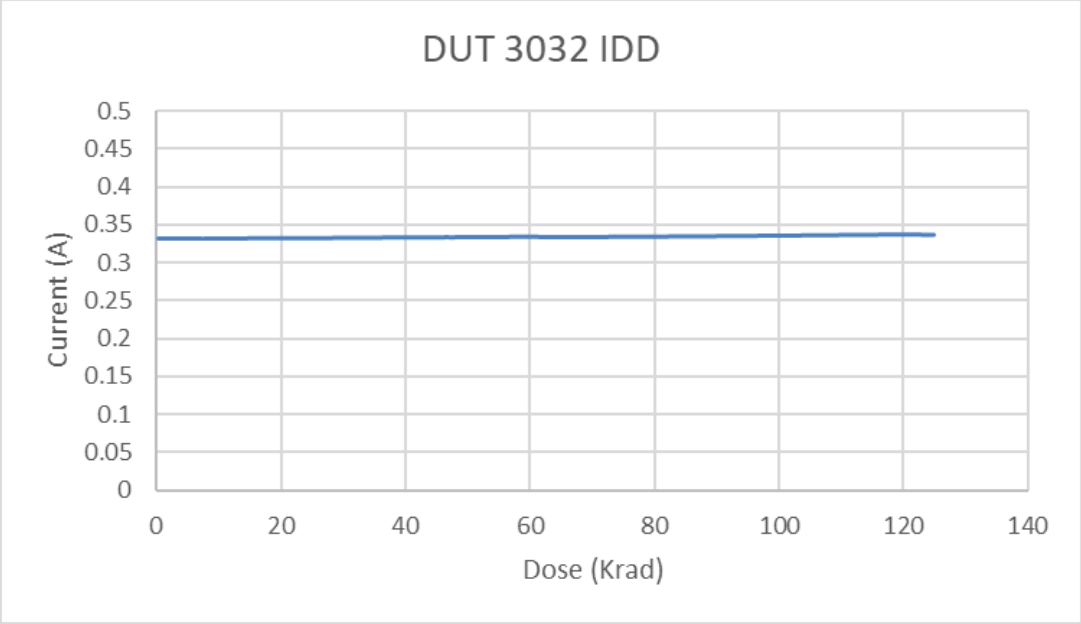

Fig. 6. DUT 03032 core power supply current (I_{DD}) versus TID

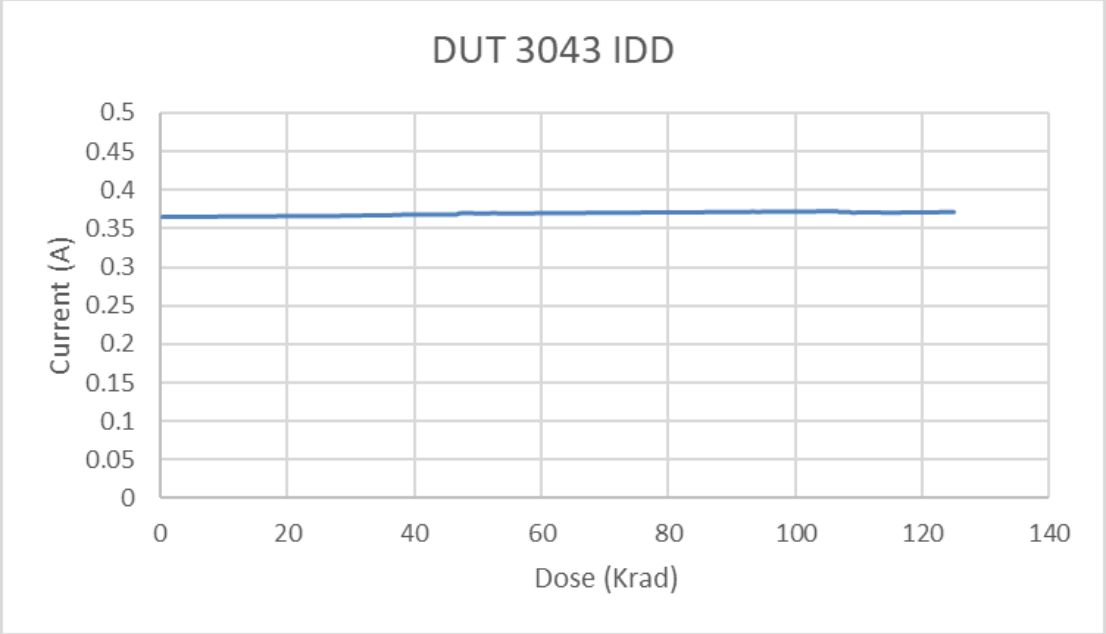

Fig. 7. DUT 03043 core power supply current (I_{DD}) versus TID

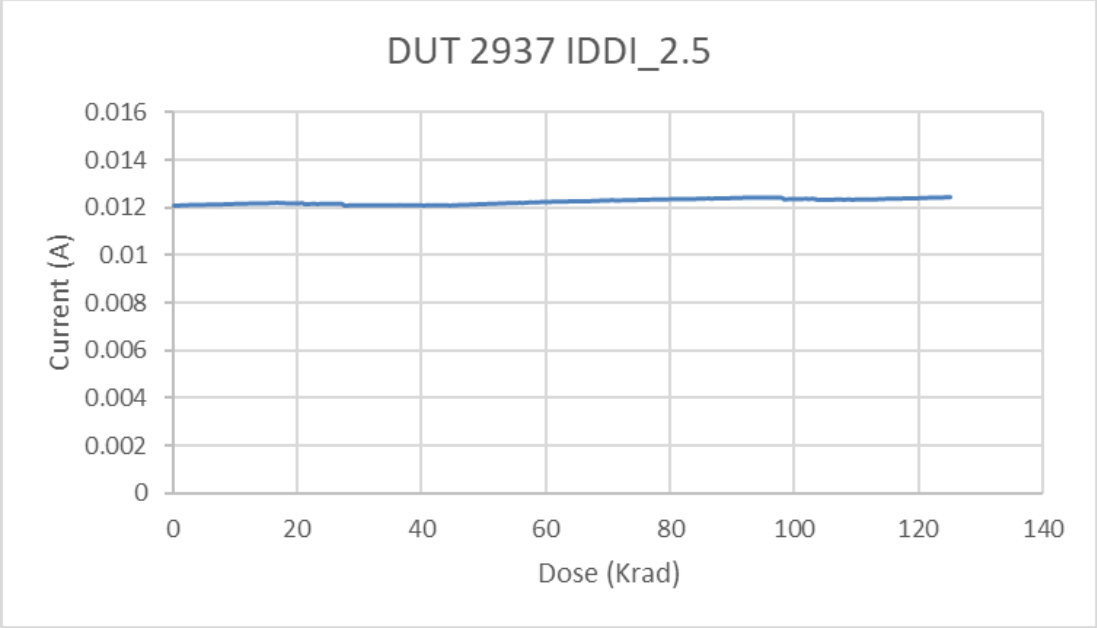

Fig. 8. DUT 02937 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

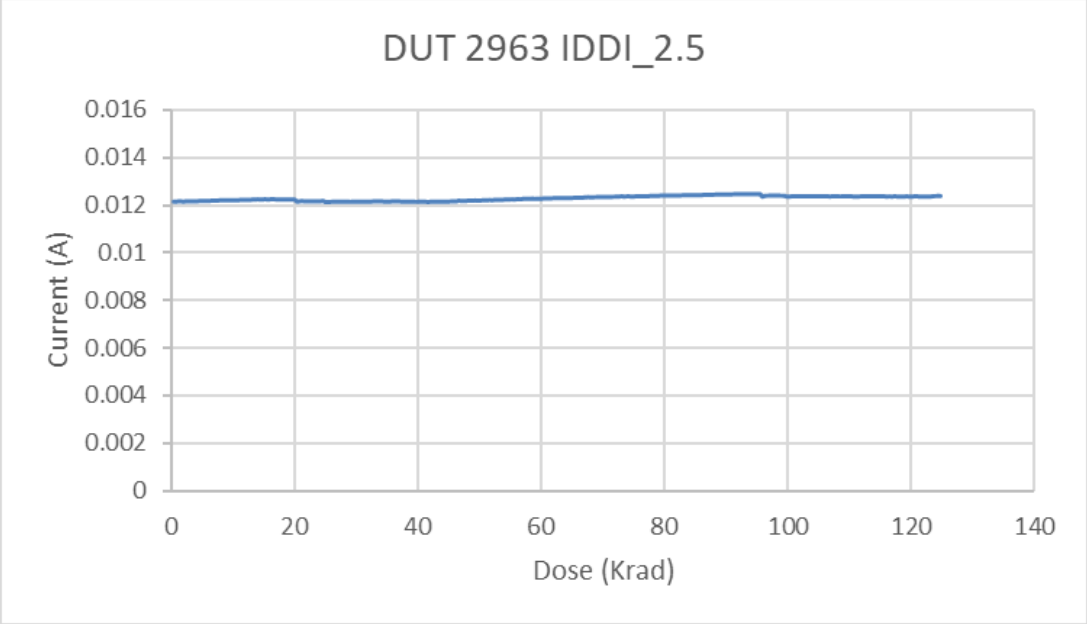

Fig. 9. DUT 02963 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

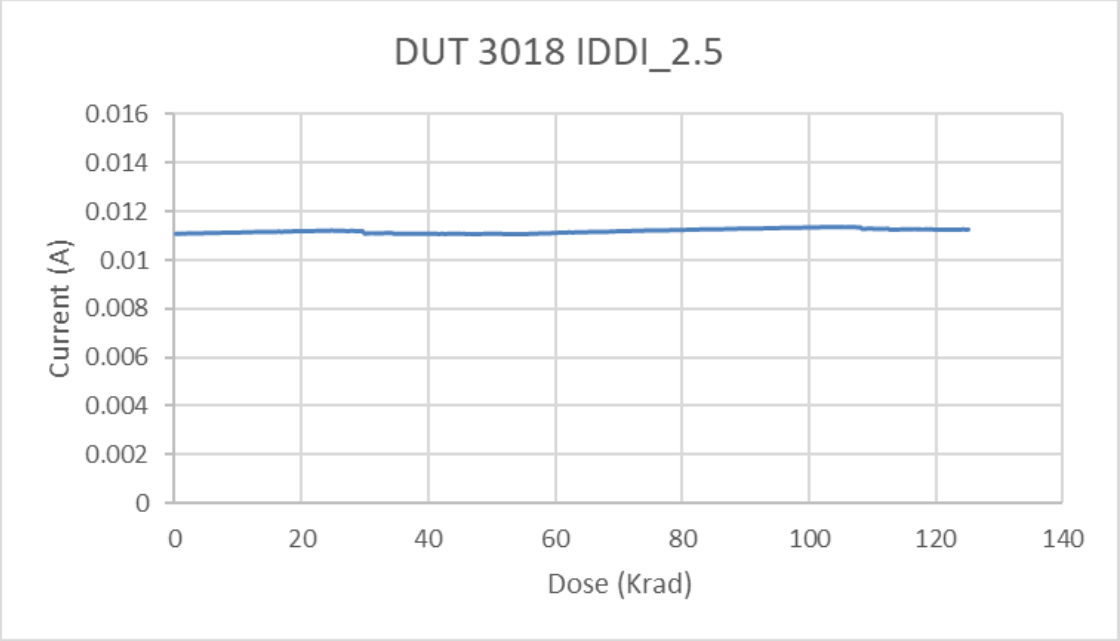

Fig. 10. DUT 03018 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

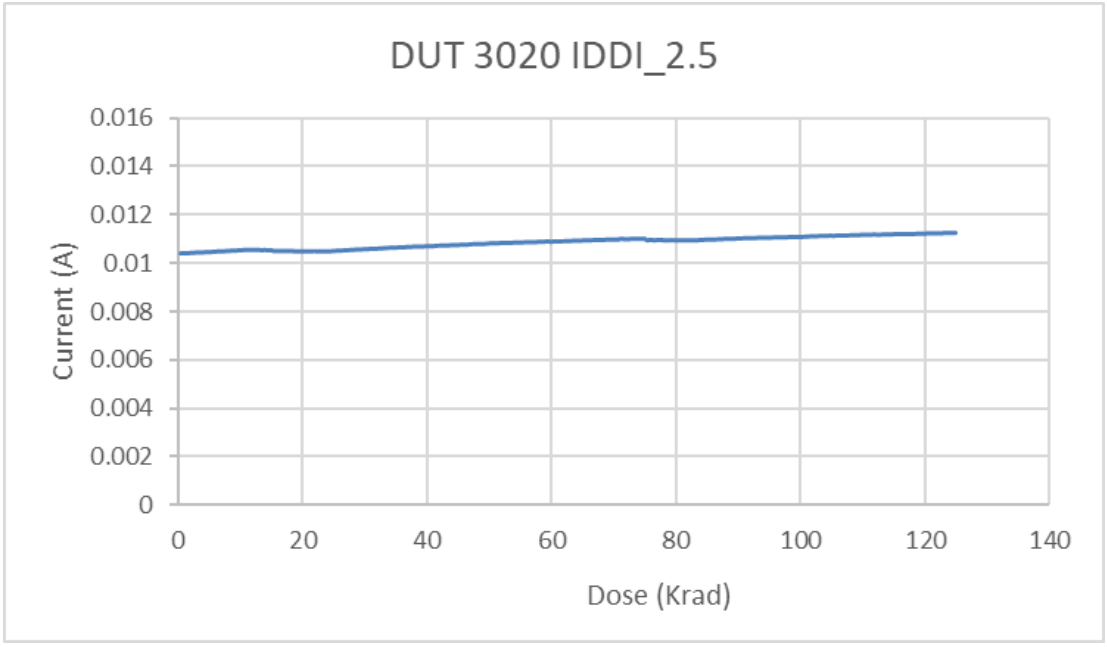

Fig. 11. DUT 03020 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

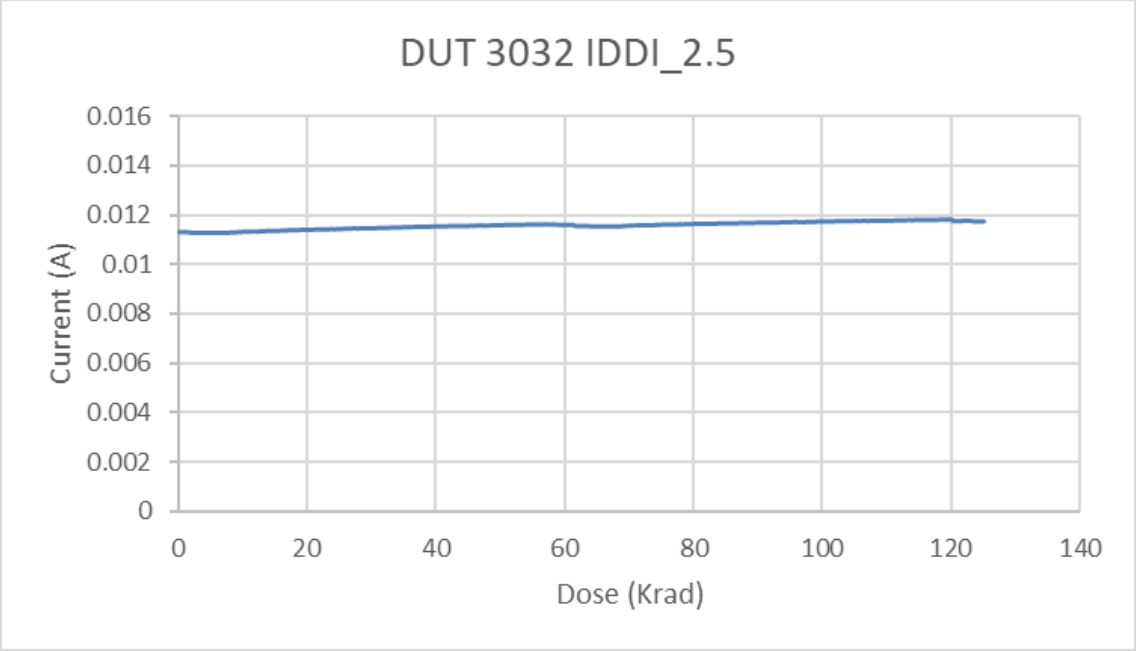

Fig. 12. DUT 03032 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

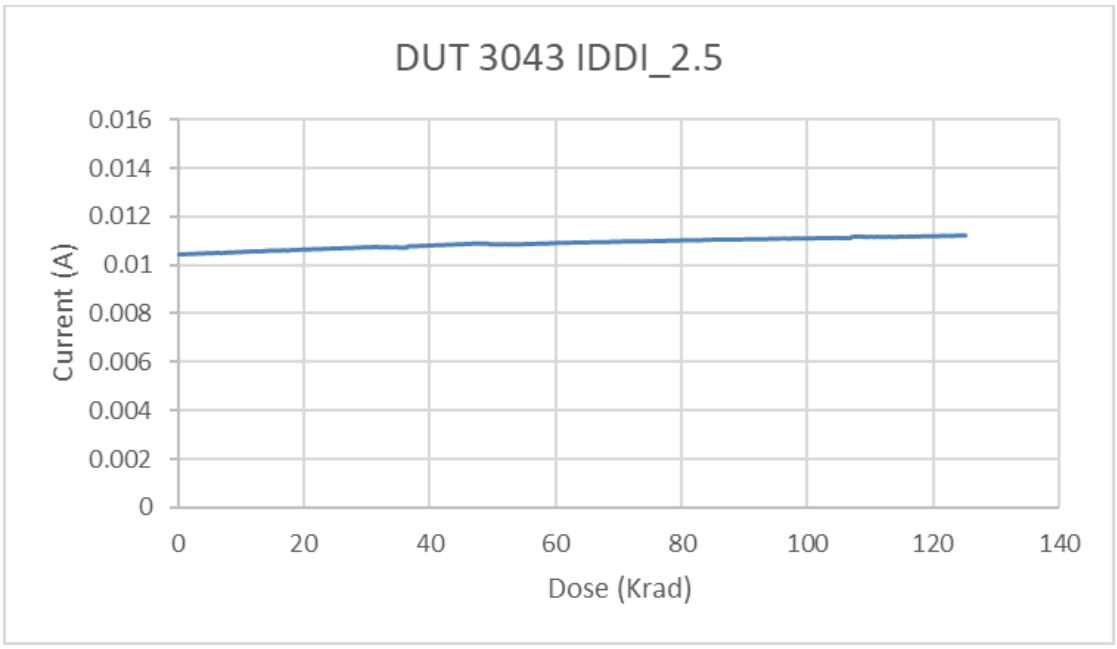

Fig. 13. DUT 03043 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

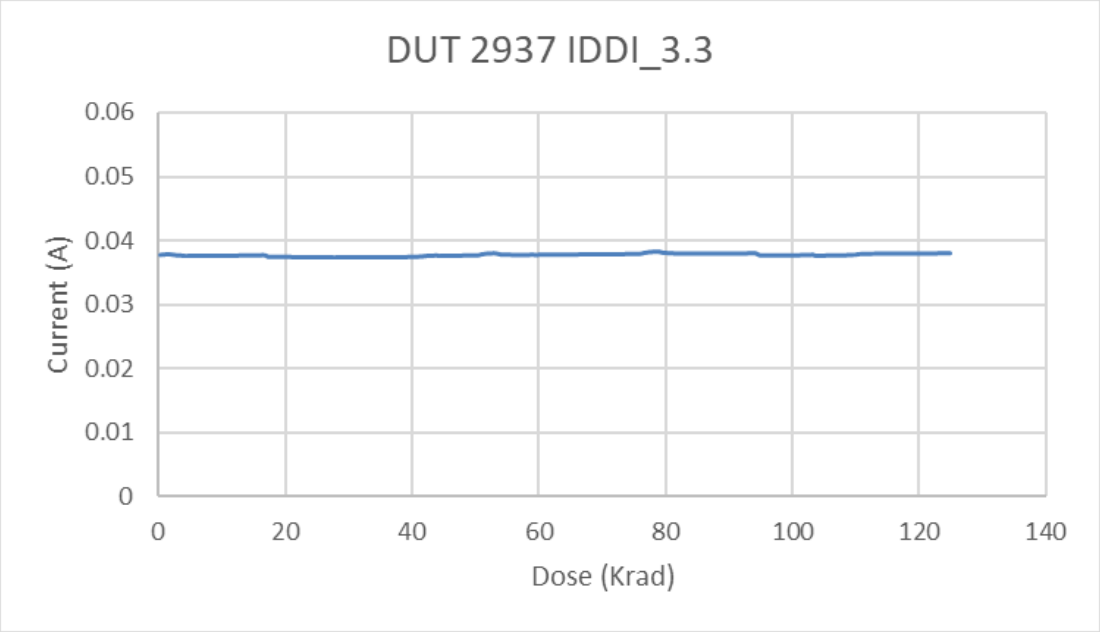

Fig. 14. DUT 02937 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

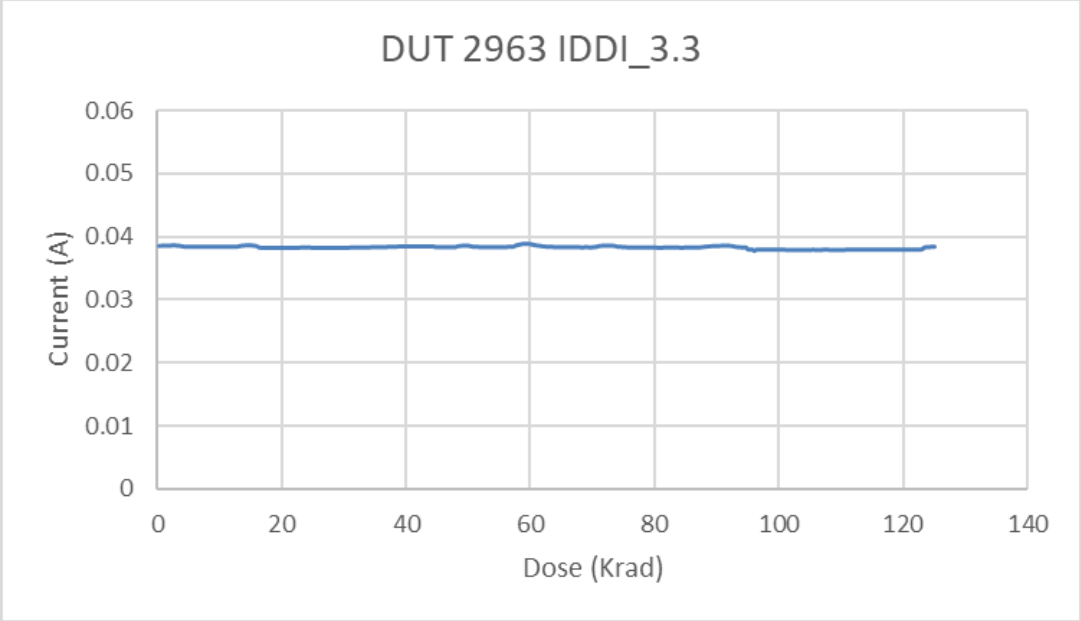

Fig. 15. DUT 02963 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

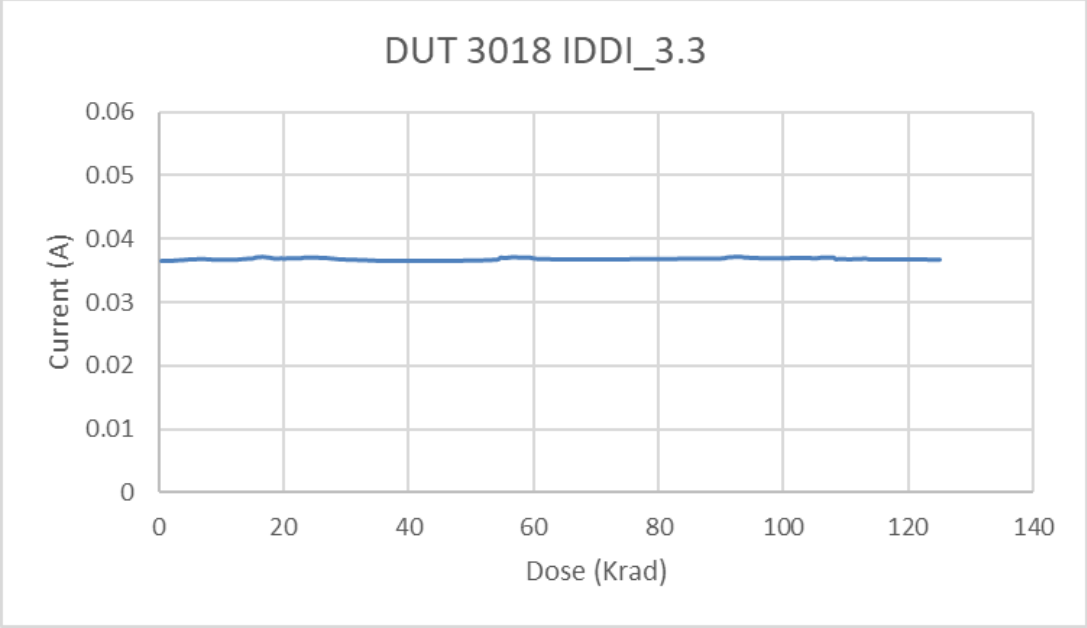

Fig. 16. DUT 03018 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

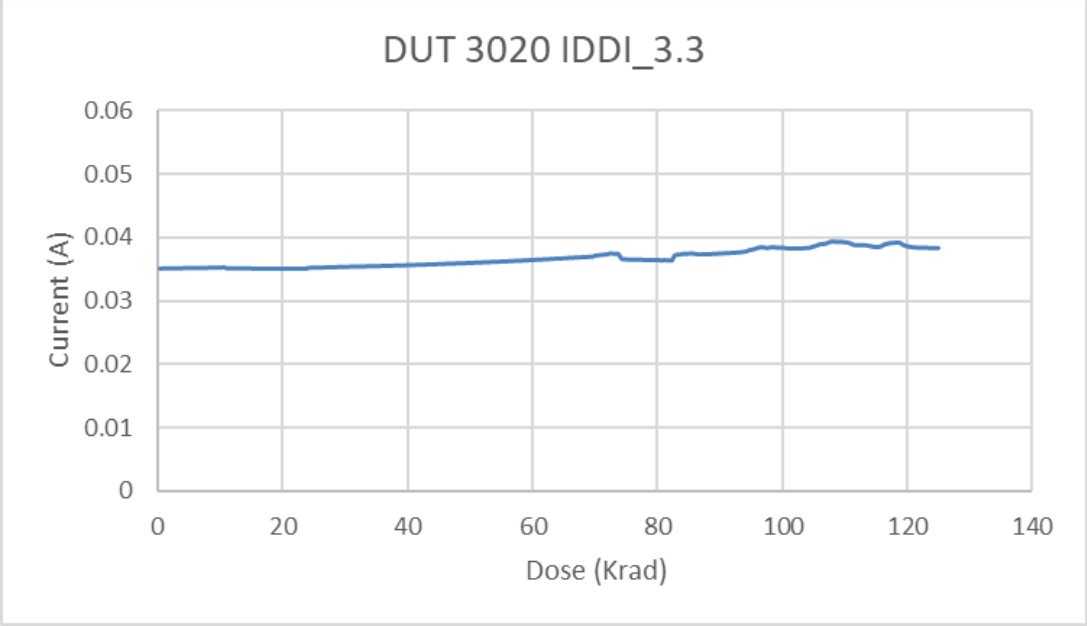

Fig. 17. DUT 03020 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

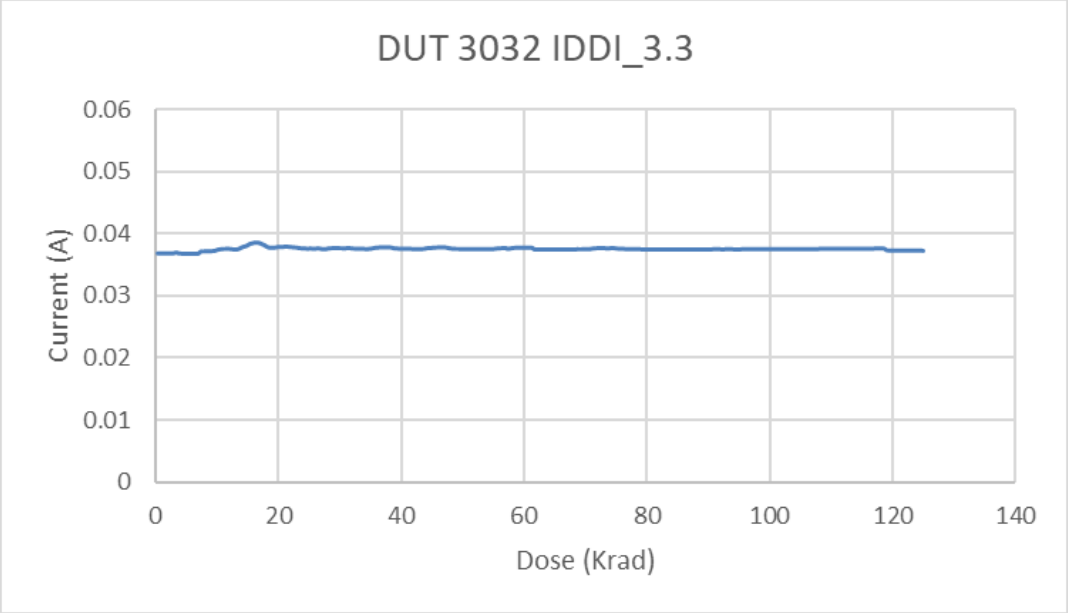

Fig. 18. DUT 03032 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

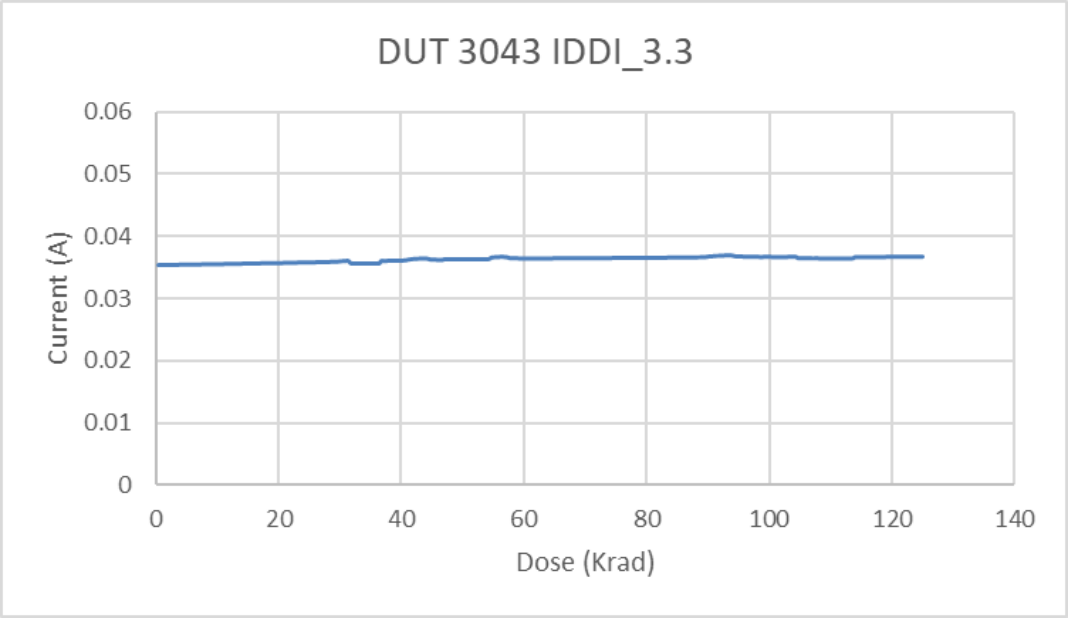

Fig. 19. DUT 03043 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

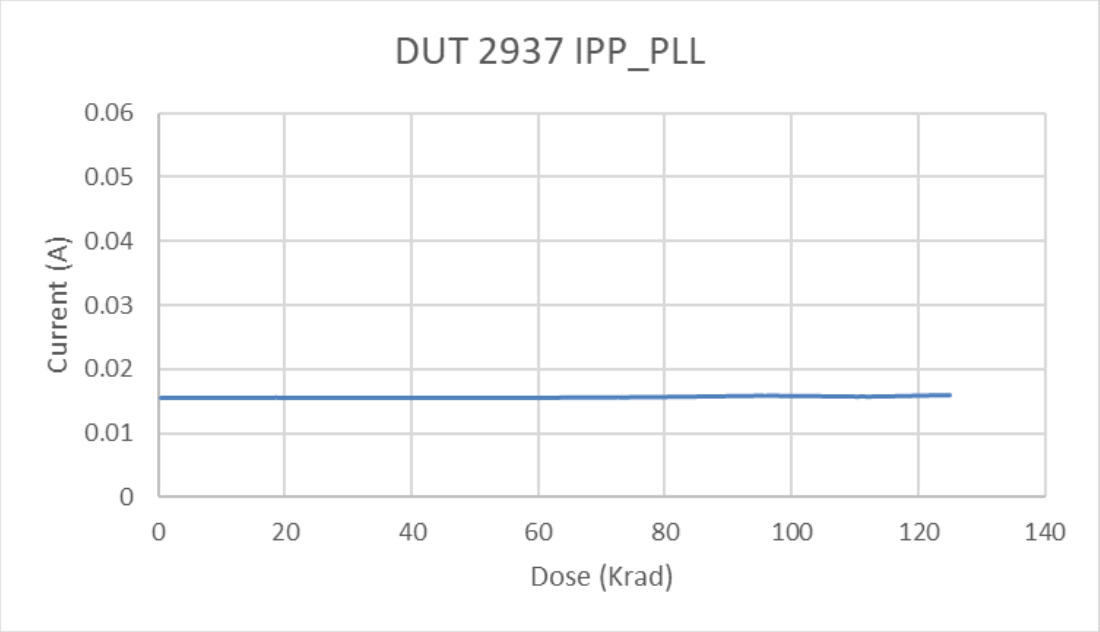

Fig. 20. DUT 02937 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

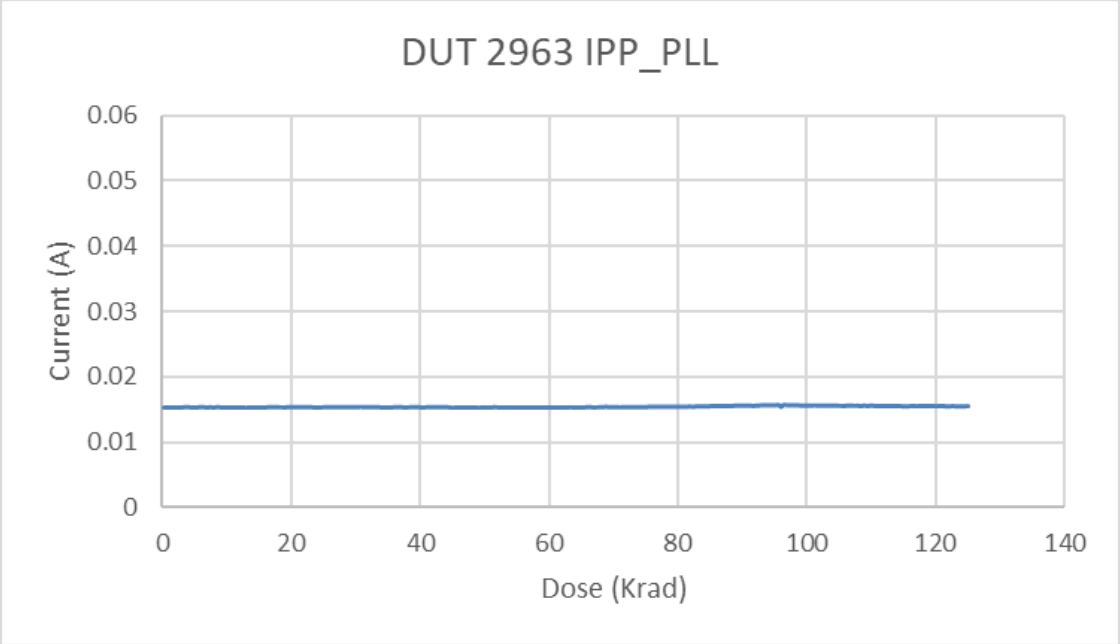

Fig. 21. DUT 02963 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

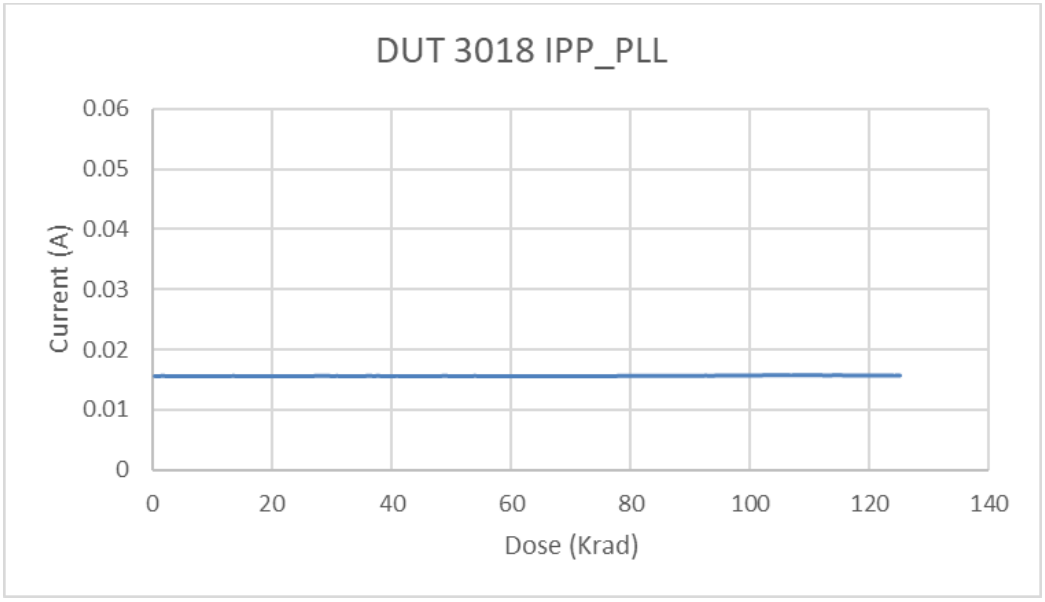

Fig. 22. DUT 03018 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

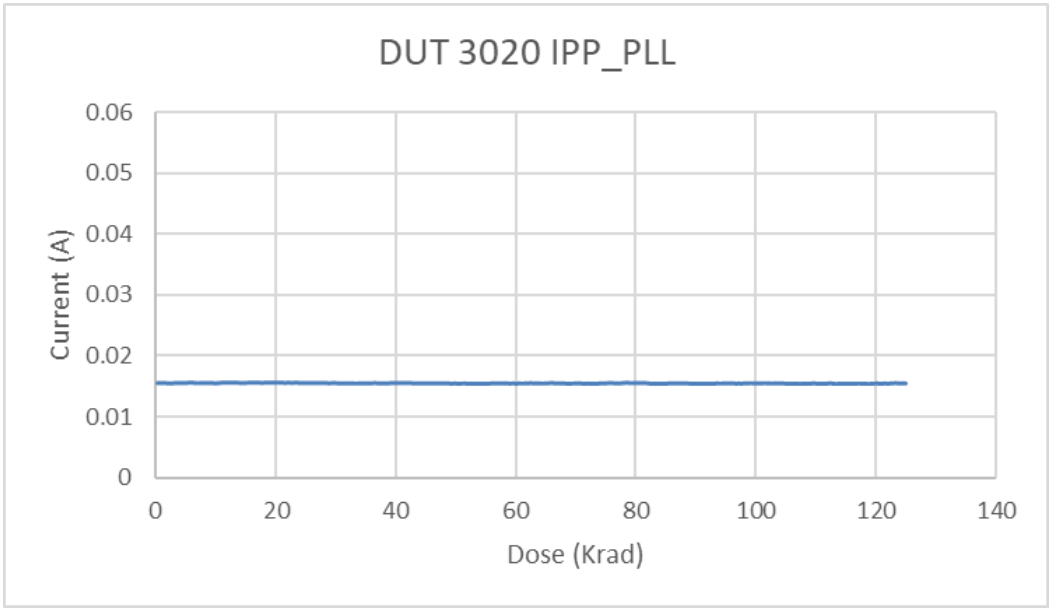

Fig. 23. DUT 03020 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

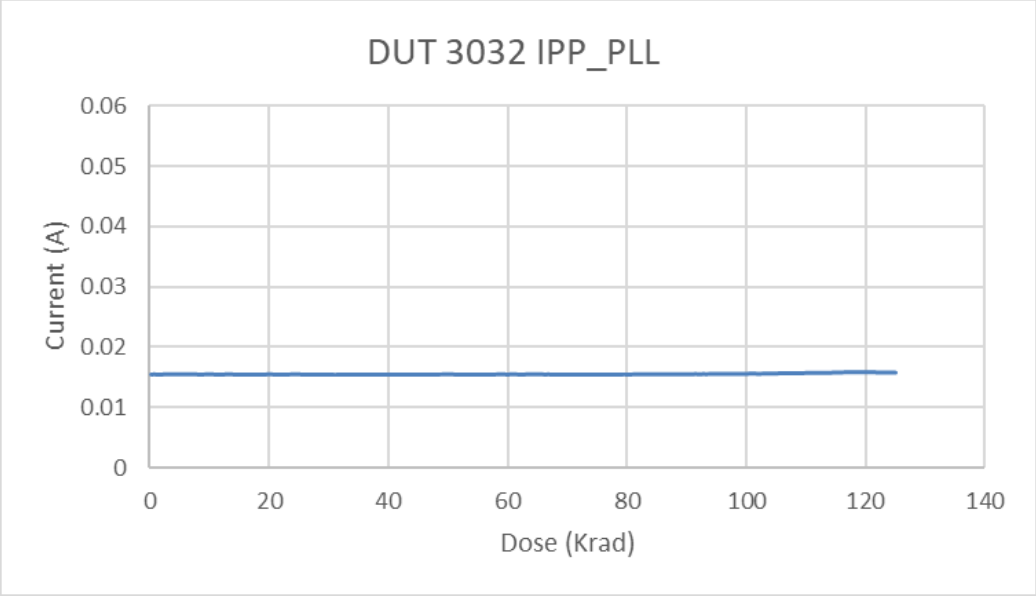

Fig. 24. DUT 03032 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

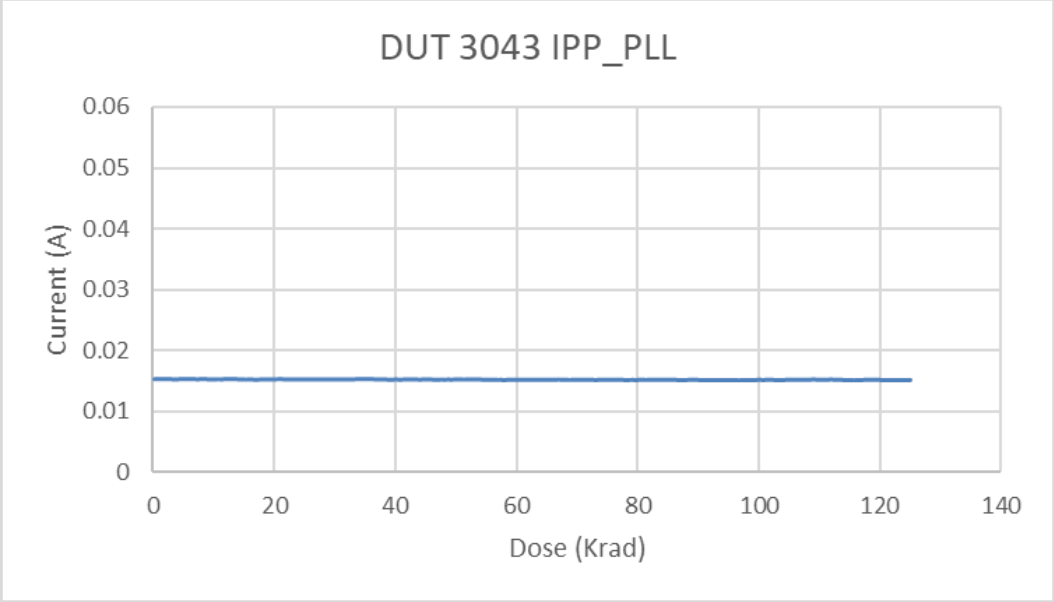

Fig. 25. DUT 03043 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. VIH is the input trip point when the input is going high to low and VIL is the input trip point when the input is going low to high. The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential input and recorded as pass or fail. All I/Os are tested at their respective I/O standards and are compliant to the JEDEC specs. Refer to http://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet for more information.

The 3 DUTs tested passed with respect to the testing specification pre and post-irradiation. This pass/fail is determined as part of the ATE test program used to perform pre and post-irradiation electrical parametric measurements.

Table. 8. VIH Summary

DUT	Pre-irradiation	Post-irradiation
02937	Passed	Passed
02963	Passed	Passed
03018	Passed	Passed
03020	Passed	Passed
03032	Passed	Passed
03043	Passed	Passed

Table. 9. VIL Summary

DUT	Pre-irradiation	Post-irradiation
02937	Passed	Passed
02963	Passed	Passed
03018	Passed	Passed
03020	Passed	Passed
03032	Passed	Passed
03043	Passed	Passed

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are performed on all available IOs. The measurements performed pre and post irradiation are within the specification limits; in each case, the radiation-induced degradation is within 10%. For the purpose of this report, the measurements presented below in tables 10 through 33 are sampled on several pins used in the burn in design.

Table. 10. LVCMOS 25 VOH – DUT 02937

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.128	2.134	2.197	2.203	2.167	2.175	2.145	2.155	2.111	2.124	2.097	2.111
EPCSRST_N_0	B31	2.130	2.135	2.199	2.203	2.170	2.174	2.148	2.154	2.115	2.122	2.100	2.108
EPCSRST_N_1	B32	2.131	2.135	2.200	2.204	2.172	2.176	2.151	2.156	2.120	2.125	2.107	2.112
EPCSRST_N_2	B34	2.130	2.134	2.199	2.203	2.170	2.174	2.148	2.153	2.116	2.121	2.102	2.108
EPCSRST_N_3	B35	2.131	2.135	2.200	2.204	2.172	2.176	2.151	2.156	2.120	2.125	2.107	2.113
EPCSRST_N_4	B36	2.130	2.134	2.198	2.202	2.168	2.172	2.146	2.151	2.112	2.118	2.098	2.103
EPCSRST_N_5	B37	2.130	2.134	2.199	2.203	2.170	2.174	2.149	2.154	2.116	2.122	2.103	2.108
MONITOR	K23	2.132	2.132	2.203	2.203	2.175	2.175	2.155	2.156	2.125	2.126	2.112	2.113
PLL_MON	L20	2.133	2.134	2.205	2.205	2.179	2.179	2.159	2.160	2.131	2.132	2.120	2.120
TOGGLE_MON	L22	2.133	2.133	2.204	2.204	2.176	2.177	2.156	2.157	2.127	2.128	2.116	2.117

Table. 11. LVCMOS 25 VOH – DUT 02963

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.132	2.132	2.200	2.200	2.172	2.171	2.150	2.150	2.118	2.118	2.104	2.104
EPCSRST_N_0	B31	2.133	2.132	2.200	2.200	2.171	2.171	2.150	2.149	2.116	2.116	2.102	2.102
EPCSRST_N_1	B32	2.134	2.133	2.202	2.201	2.174	2.173	2.153	2.152	2.122	2.121	2.109	2.108
EPCSRST_N_2	B34	2.133	2.133	2.201	2.201	2.172	2.172	2.150	2.151	2.118	2.118	2.104	2.105
EPCSRST_N_3	B35	2.134	2.133	2.202	2.202	2.174	2.175	2.154	2.154	2.123	2.123	2.110	2.110
EPCSRST_N_4	B36	2.132	2.132	2.199	2.199	2.170	2.170	2.148	2.148	2.114	2.114	2.100	2.100
EPCSRST_N_5	B37	2.132	2.132	2.201	2.200	2.172	2.172	2.150	2.150	2.118	2.118	2.104	2.104
MONITOR	K23	2.135	2.134	2.204	2.204	2.177	2.176	2.157	2.156	2.127	2.125	2.114	2.113
PLL_MON	L20	2.135	2.134	2.206	2.205	2.179	2.179	2.160	2.159	2.132	2.131	2.121	2.119
TOGGLE_MON	L22	2.134	2.134	2.204	2.204	2.177	2.177	2.158	2.157	2.128	2.128	2.116	2.116

Table. 12. LVCMOS 25 VOH – DUT 03018

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.129	2.129	2.198	2.198	2.169	2.169	2.147	2.147	2.114	2.115	2.100	2.101
EPCSRST_N_0	B31	2.130	2.129	2.198	2.198	2.169	2.168	2.147	2.146	2.114	2.112	2.099	2.098
EPCSRST_N_1	B32	2.130	2.130	2.200	2.200	2.171	2.171	2.150	2.150	2.118	2.118	2.105	2.105
EPCSRST_N_2	B34	2.129	2.129	2.198	2.198	2.169	2.169	2.147	2.147	2.114	2.115	2.100	2.101
EPCSRST_N_3	B35	2.130	2.130	2.200	2.200	2.171	2.171	2.150	2.150	2.119	2.119	2.106	2.106
EPCSRST_N_4	B36	2.129	2.128	2.197	2.197	2.168	2.168	2.145	2.146	2.112	2.112	2.098	2.098
EPCSRST_N_5	B37	2.129	2.129	2.199	2.199	2.170	2.170	2.148	2.148	2.116	2.116	2.103	2.103
MONITOR	K23	2.132	2.131	2.203	2.202	2.175	2.174	2.155	2.154	2.125	2.124	2.112	2.112
PLL_MON	L20	2.133	2.133	2.205	2.205	2.178	2.178	2.159	2.158	2.131	2.130	2.119	2.119
TOGGLE_MON	L22	2.132	2.132	2.204	2.204	2.176	2.176	2.156	2.156	2.127	2.127	2.115	2.115

Table. 13. LVCMOS 25 VOH – DUT 03020

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.131	2.131	2.200	2.200	2.171	2.171	2.149	2.150	2.117	2.118	2.103	2.104
EPCSRST_N_0	B31	2.131	2.131	2.200	2.198	2.171	2.168	2.149	2.145	2.116	2.111	2.102	2.096
EPCSRST_N_1	B32	2.133	2.133	2.202	2.201	2.173	2.173	2.152	2.153	2.122	2.121	2.108	2.108
EPCSRST_N_2	B34	2.132	2.132	2.200	2.201	2.171	2.172	2.150	2.150	2.117	2.118	2.104	2.105
EPCSRST_N_3	B35	2.132	2.132	2.202	2.202	2.174	2.174	2.153	2.153	2.122	2.123	2.109	2.110
EPCSRST_N_4	B36	2.131	2.131	2.198	2.199	2.169	2.169	2.147	2.147	2.113	2.114	2.099	2.099
EPCSRST_N_5	B37	2.131	2.132	2.200	2.200	2.171	2.172	2.150	2.150	2.117	2.118	2.104	2.104
MONITOR	K23	2.134	2.134	2.204	2.204	2.176	2.176	2.157	2.156	2.127	2.126	2.114	2.114
PLL_MON	L20	2.135	2.135	2.206	2.205	2.179	2.179	2.160	2.159	2.132	2.131	2.121	2.119
TOGGLE_MON	L22	2.134	2.135	2.204	2.204	2.177	2.177	2.157	2.157	2.128	2.128	2.116	2.116

Table. 14. LVCMOS 25 VOH – DUT 03032

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.130	2.131	2.199	2.200	2.170	2.170	2.148	2.149	2.115	2.117	2.102	2.103
EPCSRST_N_0	B31	2.130	2.132	2.199	2.200	2.169	2.170	2.147	2.148	2.114	2.115	2.100	2.101
EPCSRST_N_1	B32	2.131	2.132	2.200	2.201	2.172	2.173	2.151	2.152	2.119	2.120	2.106	2.107
EPCSRST_N_2	B34	2.129	2.130	2.198	2.199	2.169	2.170	2.147	2.148	2.115	2.116	2.101	2.102
EPCSRST_N_3	B35	2.130	2.131	2.200	2.201	2.172	2.173	2.150	2.152	2.119	2.121	2.107	2.108
EPCSRST_N_4	B36	2.129	2.130	2.197	2.199	2.168	2.169	2.145	2.147	2.111	2.113	2.097	2.099
EPCSRST_N_5	B37	2.130	2.131	2.199	2.200	2.170	2.171	2.148	2.150	2.116	2.118	2.102	2.104
MONITOR	K23	2.132	2.133	2.203	2.203	2.175	2.176	2.155	2.156	2.126	2.126	2.113	2.113
PLL_MON	L20	2.134	2.135	2.205	2.205	2.178	2.179	2.159	2.159	2.131	2.132	2.120	2.120
TOGGLE_MON	L22	2.133	2.134	2.204	2.204	2.177	2.177	2.156	2.158	2.128	2.129	2.115	2.117

Table. 15. LVCMOS 25 VOH – DUT 03043

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.129	2.129	2.198	2.199	2.169	2.170	2.147	2.148	2.115	2.116	2.101	2.102
EPCSRST_N_0	B31	2.129	2.130	2.198	2.198	2.169	2.168	2.147	2.146	2.113	2.112	2.099	2.097
EPCSRST_N_1	B32	2.130	2.131	2.200	2.200	2.172	2.172	2.151	2.151	2.119	2.119	2.106	2.106
EPCSRST_N_2	B34	2.129	2.130	2.198	2.199	2.169	2.170	2.148	2.149	2.115	2.116	2.102	2.103
EPCSRST_N_3	B35	2.130	2.131	2.200	2.201	2.172	2.172	2.151	2.151	2.120	2.121	2.107	2.108
EPCSRST_N_4	B36	2.129	2.130	2.197	2.198	2.168	2.168	2.145	2.146	2.112	2.113	2.097	2.099
EPCSRST_N_5	B37	2.130	2.130	2.199	2.199	2.170	2.171	2.148	2.149	2.116	2.117	2.103	2.103
MONITOR	K23	2.131	2.132	2.202	2.203	2.175	2.175	2.154	2.155	2.124	2.124	2.112	2.112
PLL_MON	L20	2.133	2.133	2.205	2.205	2.178	2.178	2.158	2.158	2.130	2.131	2.119	2.119
TOGGLE_MON	L22	2.132	2.133	2.203	2.204	2.176	2.176	2.156	2.156	2.127	2.127	2.115	2.115

Table. 16. LVCMOS 25 VOL – DUT 02937

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	238.5	235.1	171.0	166.8	200.0	194.3	221.0	215.8	254.3	245.8	268.8	258.7
EPCSRST_N_0	B31	236.7	234.4	169.5	167.5	198.2	195.6	218.9	217.7	251.2	248.8	265.5	262.2
EPCSRST_N_1	B32	235.5	233.4	167.2	165.7	194.8	193.1	214.4	213.7	245.2	243.7	258.1	256.5
EPCSRST_N_2	B34	237.1	235.0	169.2	167.7	197.6	195.7	218.0	216.8	249.8	247.8	263.4	261.1
EPCSRST_N_3	B35	236.6	234.4	167.8	166.3	195.4	193.7	215.0	214.2	245.5	244.0	258.3	256.6
EPCSRST_N_4	B36	237.6	235.6	170.4	168.9	199.4	197.6	220.4	219.3	253.2	251.6	267.3	265.4
EPCSRST_N_5	B37	237.3	235.2	169.1	167.3	197.2	195.4	217.6	216.5	249.2	247.3	262.6	260.5
MONITOR	K23	236.0	233.9	166.8	165.5	193.9	192.3	213.5	212.0	242.5	241.3	254.9	253.6
PLL_MON	L20	234.6	232.6	164.5	163.3	190.5	189.3	208.2	207.7	235.6	235.0	247.0	246.2
TOGGLE_MON	L22	235.0	232.8	165.7	164.2	192.4	190.8	211.3	209.6	239.8	238.1	251.8	250.0

Table. 17. LVCMOS 25 VOL – DUT 02963

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	235.4	234.9	167.9	167.6	195.9	195.4	216.1	215.6	247.8	247.1	261.6	260.8
EPCSRST_N_0	B31	234.2	233.6	168.1	167.8	196.4	196.3	217.1	217.0	249.6	249.5	263.8	263.8
EPCSRST_N_1	B32	232.9	232.5	165.6	165.6	193.1	193.1	212.5	212.9	243.3	243.8	256.1	257.0
EPCSRST_N_2	B34	234.3	233.6	167.3	166.7	195.4	194.7	215.4	214.7	247.3	246.5	260.9	259.9
EPCSRST_N_3	B35	233.3	232.7	165.8	165.3	193.2	192.7	212.6	212.1	242.8	242.1	255.8	255.0
EPCSRST_N_4	B36	235.0	234.5	168.9	168.3	197.7	197.1	218.4	217.9	251.8	251.0	266.0	265.2
EPCSRST_N_5	B37	235.2	234.6	167.6	167.2	195.7	195.1	215.8	215.3	247.4	246.8	260.8	260.5
MONITOR	K23	233.6	233.1	165.3	165.3	192.3	192.5	211.9	212.1	241.0	241.7	253.4	254.2
PLL_MON	L20	233.6	233.4	163.9	163.8	189.9	190.0	207.8	207.9	235.1	235.6	246.6	247.2
TOGGLE_MON	L22	233.6	233.0	165.1	164.8	191.6	191.2	210.2	209.9	239.0	238.7	251.1	250.7

Table. 18. LVCMOS 25 VOL – DUT 03018

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	238.3	237.3	170.1	169.4	198.5	197.7	219.0	218.2	251.2	250.0	265.2	263.9
EPCSRST_N_0	B31	237.2	236.4	170.0	169.8	198.7	198.7	219.5	219.7	252.1	252.7	266.5	267.2
EPCSRST_N_1	B32	236.0	235.2	167.8	167.3	195.5	195.0	215.4	214.6	246.3	245.5	259.4	258.9
EPCSRST_N_2	B34	238.3	237.1	170.0	169.3	198.5	197.5	218.8	217.7	251.1	249.6	264.7	263.1
EPCSRST_N_3	B35	237.7	236.7	168.5	167.8	196.2	195.4	215.9	215.0	246.6	245.4	259.5	258.3
EPCSRST_N_4	B36	238.7	237.6	170.9	170.3	199.9	199.0	220.6	219.7	253.7	252.6	267.8	266.6
EPCSRST_N_5	B37	238.2	237.3	169.7	169.0	197.9	197.1	218.0	217.1	249.6	248.6	263.0	261.9
MONITOR	K23	236.4	235.6	166.9	166.5	193.9	193.6	213.6	213.3	242.5	242.5	255.0	255.0
PLL_MON	L20	235.2	234.4	164.8	164.4	190.8	190.4	208.5	208.2	235.9	235.6	247.2	247.1
TOGGLE_MON	L22	235.4	234.4	165.8	165.3	192.5	191.9	211.4	210.6	240.1	239.4	252.2	251.3

Table. 19. LVCMOS 25 VOL – DUT 03020

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	235.3	234.1	167.9	167.1	195.9	194.9	215.8	215.1	247.5	246.6	261.3	260.2
EPCSRST_N_0	B31	234.6	234.3	168.0	169.0	196.5	198.3	217.0	219.6	249.4	253.6	263.6	268.5
EPCSRST_N_1	B32	232.8	231.6	165.7	165.0	193.2	192.3	212.8	211.7	243.3	242.2	256.2	255.3
EPCSRST_N_2	B34	234.1	232.9	167.3	166.4	195.2	194.3	215.4	214.1	246.8	245.4	260.4	258.8
EPCSRST_N_3	B35	234.2	232.9	166.0	165.2	193.4	192.4	212.8	211.6	243.1	241.9	255.9	254.6
EPCSRST_N_4	B36	235.5	234.3	169.2	168.3	197.9	197.1	218.8	217.6	251.8	250.5	266.0	264.7
EPCSRST_N_5	B37	235.0	233.7	167.6	166.8	195.8	194.8	215.9	214.7	247.7	246.3	261.2	259.7
MONITOR	K23	233.1	232.2	164.9	164.4	191.8	191.3	211.3	210.8	240.4	240.0	252.6	252.4
PLL_MON	L20	232.4	231.6	163.1	162.9	189.0	189.1	206.7	207.0	234.0	234.7	245.4	246.3
TOGGLE_MON	L22	232.6	231.6	164.6	163.8	191.1	190.3	209.9	208.7	238.7	237.6	250.7	249.7

Table. 20. LVCMOS 25 VOL – DUT 03032

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	237.1	234.7	169.2	167.6	197.5	195.7	218.0	216.0	249.8	247.8	263.8	261.4
EPCSRST_N_0	B31	236.4	234.2	169.3	168.0	198.0	196.3	218.7	216.9	251.2	249.4	265.3	263.4
EPCSRST_N_1	B32	235.1	233.0	167.1	165.6	194.8	193.1	214.5	212.7	245.5	243.3	258.4	256.4
EPCSRST_N_2	B34	237.0	234.8	169.4	167.9	197.7	196.1	218.1	216.2	250.3	248.1	264.0	261.6
EPCSRST_N_3	B35	236.6	234.3	167.8	166.1	195.6	193.7	215.4	213.1	245.9	243.3	258.8	256.1
EPCSRST_N_4	B36	237.8	235.4	170.7	168.7	199.7	197.6	220.6	218.1	253.9	251.0	268.1	265.0
EPCSRST_N_5	B37	237.0	234.8	168.9	167.2	197.3	195.3	217.6	215.3	249.3	246.7	262.8	260.1
MONITOR	K23	235.0	233.0	166.2	165.0	193.2	191.8	212.7	211.3	241.7	240.4	254.0	252.8
PLL_MON	L20	233.9	231.6	164.2	162.9	190.2	188.8	208.0	206.4	235.2	233.7	246.6	245.1
TOGGLE_MON	L22	234.7	232.4	165.4	163.8	192.0	190.2	210.5	208.6	239.4	236.9	251.2	249.0

Table. 21. LVCMOS 25 VOL – DUT 03043

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	237.1	235.4	169.4	168.0	197.6	196.0	218.0	216.3	249.8	247.8	263.6	261.5
EPCSRST_N_0	B31	236.4	235.3	169.5	169.2	198.1	198.1	218.8	219.0	251.3	252.3	265.6	266.9
EPCSRST_N_1	B32	235.2	233.7	166.9	166.2	194.6	193.8	214.4	213.4	244.9	244.2	258.0	257.1
EPCSRST_N_2	B34	236.8	235.2	168.8	167.6	197.1	195.5	217.3	215.5	249.1	246.8	262.5	260.3
EPCSRST_N_3	B35	236.0	234.4	167.6	166.3	195.1	193.8	214.7	213.1	245.1	243.2	257.9	256.0
EPCSRST_N_4	B36	237.0	235.4	170.1	168.9	199.1	197.7	220.0	218.2	252.9	250.8	267.0	264.9
EPCSRST_N_5	B37	236.4	234.6	168.5	167.4	196.6	195.4	216.8	215.4	248.6	247.1	262.0	260.4
MONITOR	K23	235.2	233.8	166.4	165.6	193.5	192.6	212.9	212.1	242.0	241.2	254.5	253.5
PLL_MON	L20	234.6	233.0	164.7	163.7	190.7	189.7	208.5	207.3	236.0	234.7	247.5	246.0
TOGGLE_MON	L22	234.8	233.3	165.5	164.5	192.2	191.1	210.9	209.7	239.5	238.2	251.5	250.2

Table. 22. LVTTL VOH – DUT 02937

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.915	2.920	2.905	2.911	2.884	2.894	2.864	2.876	2.843	2.859
EPCSRST_N_0	B31	2.917	2.921	2.906	2.911	2.887	2.892	2.867	2.873	2.847	2.855
EPCSRST_N_1	B32	2.917	2.921	2.908	2.913	2.891	2.895	2.873	2.877	2.855	2.860
EPCSRST_N_2	B34	2.916	2.920	2.907	2.910	2.888	2.892	2.869	2.873	2.849	2.855
EPCSRST_N_3	B35	2.917	2.921	2.908	2.912	2.891	2.895	2.873	2.878	2.856	2.861
EPCSRST_N_4	B36	2.916	2.920	2.906	2.909	2.885	2.890	2.865	2.870	2.845	2.850
EPCSRST_N_5	B37	2.916	2.920	2.907	2.911	2.888	2.892	2.870	2.874	2.850	2.856
MONITOR	K23	2.919	2.919	2.911	2.911	2.894	2.895	2.878	2.878	2.862	2.862
PLL_MON	L20	2.921	2.921	2.913	2.914	2.899	2.899	2.885	2.885	2.870	2.870
TOGGLE_MON	L22	2.920	2.920	2.912	2.913	2.896	2.897	2.881	2.882	2.865	2.866

Table. 23. LVTTL VOH – DUT 02963

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.919	2.918	2.909	2.909	2.890	2.890	2.872	2.872	2.852	2.852
EPCSRST_N_0	B31	2.919	2.919	2.909	2.909	2.889	2.889	2.870	2.869	2.850	2.849
EPCSRST_N_1	B32	2.920	2.920	2.911	2.910	2.893	2.892	2.876	2.874	2.857	2.856
EPCSRST_N_2	B34	2.919	2.919	2.910	2.910	2.891	2.891	2.872	2.872	2.852	2.853
EPCSRST_N_3	B35	2.921	2.921	2.911	2.911	2.894	2.894	2.877	2.877	2.859	2.859
EPCSRST_N_4	B36	2.919	2.918	2.908	2.909	2.888	2.888	2.868	2.868	2.847	2.847
EPCSRST_N_5	B37	2.918	2.918	2.909	2.909	2.891	2.890	2.872	2.872	2.853	2.852
MONITOR	K23	2.922	2.921	2.913	2.913	2.897	2.896	2.880	2.879	2.864	2.862
PLL_MON	L20	2.922	2.921	2.915	2.914	2.900	2.899	2.886	2.885	2.871	2.869
TOGGLE_MON	L22	2.921	2.921	2.914	2.913	2.898	2.897	2.882	2.882	2.866	2.866

Table. 24. LVTTL VOH – DUT 03018

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.916	2.916	2.906	2.906	2.887	2.887	2.867	2.868	2.848	2.848
EPCSRST_N_0	B31	2.916	2.916	2.906	2.906	2.886	2.885	2.866	2.865	2.846	2.845
EPCSRST_N_1	B32	2.917	2.917	2.908	2.908	2.890	2.890	2.872	2.872	2.853	2.853
EPCSRST_N_2	B34	2.916	2.916	2.906	2.906	2.887	2.887	2.867	2.868	2.848	2.849
EPCSRST_N_3	B35	2.916	2.916	2.907	2.908	2.890	2.890	2.872	2.873	2.854	2.855
EPCSRST_N_4	B36	2.915	2.915	2.905	2.905	2.885	2.885	2.865	2.865	2.845	2.845
EPCSRST_N_5	B37	2.916	2.916	2.906	2.906	2.888	2.888	2.869	2.869	2.850	2.850
MONITOR	K23	2.919	2.918	2.911	2.911	2.894	2.894	2.878	2.877	2.862	2.861
PLL_MON	L20	2.920	2.920	2.913	2.913	2.899	2.898	2.885	2.884	2.870	2.869
TOGGLE_MON	L22	2.920	2.920	2.912	2.912	2.896	2.896	2.881	2.881	2.865	2.865

Table. 25. LVTTL VOH – DUT 03020

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.918	2.918	2.908	2.909	2.889	2.890	2.870	2.871	2.851	2.852
EPCSRST_N_0	B31	2.918	2.917	2.908	2.907	2.889	2.885	2.869	2.864	2.849	2.843
EPCSRST_N_1	B32	2.919	2.920	2.910	2.910	2.893	2.893	2.875	2.875	2.857	2.857
EPCSRST_N_2	B34	2.919	2.919	2.909	2.909	2.890	2.890	2.871	2.872	2.852	2.853
EPCSRST_N_3	B35	2.919	2.919	2.910	2.910	2.893	2.893	2.876	2.876	2.858	2.858
EPCSRST_N_4	B36	2.918	2.918	2.907	2.908	2.887	2.887	2.867	2.867	2.846	2.846
EPCSRST_N_5	B37	2.918	2.918	2.909	2.909	2.889	2.890	2.871	2.872	2.851	2.852
MONITOR	K23	2.921	2.921	2.913	2.913	2.897	2.896	2.880	2.880	2.864	2.863
PLL_MON	L20	2.922	2.922	2.915	2.914	2.900	2.900	2.886	2.884	2.872	2.869
TOGGLE_MON	L22	2.922	2.922	2.913	2.914	2.898	2.898	2.882	2.882	2.866	2.866

Table. 26. LVTTL VOH – DUT 03032

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.916	2.917	2.907	2.908	2.888	2.889	2.868	2.869	2.849	2.850
EPCSRST_N_0	B31	2.917	2.918	2.907	2.908	2.887	2.888	2.867	2.868	2.847	2.848
EPCSRST_N_1	B32	2.917	2.918	2.908	2.909	2.891	2.891	2.873	2.874	2.854	2.855
EPCSRST_N_2	B34	2.916	2.917	2.906	2.907	2.887	2.888	2.868	2.869	2.848	2.849
EPCSRST_N_3	B35	2.917	2.917	2.908	2.909	2.890	2.892	2.873	2.874	2.855	2.856
EPCSRST_N_4	B36	2.916	2.916	2.905	2.906	2.885	2.886	2.865	2.866	2.844	2.846
EPCSRST_N_5	B37	2.916	2.917	2.907	2.908	2.888	2.889	2.869	2.871	2.850	2.852
MONITOR	K23	2.920	2.920	2.911	2.912	2.895	2.895	2.878	2.879	2.862	2.862
PLL_MON	L20	2.921	2.921	2.913	2.914	2.899	2.900	2.885	2.885	2.870	2.870
TOGGLE_MON	L22	2.920	2.921	2.912	2.913	2.897	2.897	2.881	2.882	2.865	2.867

Table. 27. LVTTL VOH – DUT 03043

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.916	2.916	2.906	2.906	2.887	2.888	2.868	2.869	2.848	2.850
EPCSRST_N_0	B31	2.916	2.916	2.906	2.905	2.886	2.885	2.866	2.865	2.846	2.844
EPCSRST_N_1	B32	2.917	2.917	2.908	2.909	2.890	2.890	2.873	2.873	2.854	2.854
EPCSRST_N_2	B34	2.916	2.916	2.906	2.907	2.887	2.889	2.869	2.870	2.849	2.850
EPCSRST_N_3	B35	2.917	2.917	2.908	2.909	2.890	2.891	2.873	2.874	2.855	2.856
EPCSRST_N_4	B36	2.916	2.916	2.905	2.906	2.885	2.886	2.865	2.866	2.844	2.846
EPCSRST_N_5	B37	2.916	2.917	2.907	2.907	2.888	2.889	2.869	2.870	2.850	2.851
MONITOR	K23	2.919	2.919	2.910	2.910	2.894	2.894	2.877	2.877	2.861	2.861
PLL_MON	L20	2.920	2.920	2.913	2.913	2.898	2.898	2.884	2.884	2.869	2.869
TOGGLE_MON	L22	2.919	2.920	2.912	2.912	2.896	2.896	2.880	2.881	2.865	2.865

Table. 28. LVTTL VOL – DUT 02937

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	218.3	215.7	227.4	226.7	247.8	241.0	268.1	258.5	288.5	277.1
EPCSRST_N_0	B31	216.7	215.5	225.8	226.9	245.5	243.0	264.8	261.6	284.5	281.3
EPCSRST_N_1	B32	215.4	214.4	223.0	223.3	241.2	239.5	258.5	256.6	276.5	274.8
EPCSRST_N_2	B34	217.0	215.6	224.8	225.4	244.8	242.8	263.3	261.0	282.3	280.0
EPCSRST_N_3	B35	216.2	215.1	223.4	224.1	241.6	239.9	258.9	257.0	276.4	275.0
EPCSRST_N_4	B36	217.7	216.1	226.2	226.6	246.9	245.2	266.8	264.8	286.9	285.2
EPCSRST_N_5	B37	217.1	216.0	224.4	225.2	244.2	242.3	262.7	260.5	281.4	279.4
MONITOR	K23	215.9	214.0	223.7	222.6	239.7	237.9	255.6	254.2	272.7	271.3
PLL_MON	L20	214.8	213.0	219.8	219.7	235.7	234.2	249.9	248.4	263.7	263.1
TOGGLE_MON	L22	215.0	213.3	221.9	220.5	237.9	236.1	253.4	251.7	269.1	267.4

Table. 29. LVTTL VOL – DUT 02963

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	215.1	214.6	223.3	222.4	242.2	241.7	260.8	260.3	279.9	279.1
EPCSRST_N_0	B31	214.0	213.6	223.0	222.5	242.9	242.8	262.6	262.3	282.5	282.5
EPCSRST_N_1	B32	212.8	212.7	219.9	219.7	238.7	238.9	256.1	256.7	274.1	274.9
EPCSRST_N_2	B34	213.9	213.3	221.5	221.0	241.5	240.7	260.1	259.3	279.3	278.4
EPCSRST_N_3	B35	212.9	212.5	220.1	219.7	238.6	238.0	255.7	254.9	273.3	272.7
EPCSRST_N_4	B36	214.6	214.2	223.1	222.6	244.5	243.7	264.5	264.0	285.1	284.3
EPCSRST_N_5	B37	215.0	214.5	222.1	222.0	241.9	241.3	260.4	259.8	279.3	278.9
MONITOR	K23	213.3	213.2	221.5	221.2	237.6	237.9	253.8	254.7	270.7	271.8
PLL_MON	L20	214.0	213.4	218.9	218.9	234.5	234.8	248.8	249.6	263.0	263.7
TOGGLE_MON	L22	213.6	213.0	220.6	220.1	236.6	236.2	252.3	252.1	268.1	267.8

Table. 30. LVTTL VOL – DUT 03018

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	217.6	216.8	226.3	225.4	245.7	244.6	264.5	263.4	283.9	282.6
EPCSRST_N_0	B31	216.7	216.6	225.6	225.5	245.8	246.0	265.5	266.2	285.5	286.4
EPCSRST_N_1	B32	215.7	214.8	223.1	222.2	241.8	241.3	259.4	258.9	277.7	277.1
EPCSRST_N_2	B34	217.4	216.7	225.6	224.5	245.4	244.3	264.4	263.0	283.5	281.8
EPCSRST_N_3	B35	217.1	216.2	224.1	223.4	242.4	241.5	259.6	258.8	277.5	276.4
EPCSRST_N_4	B36	218.2	217.1	226.4	225.5	247.3	246.5	266.8	265.9	287.0	285.8
EPCSRST_N_5	B37	217.8	216.9	225.2	224.1	244.7	243.8	262.8	262.0	281.6	280.4
MONITOR	K23	216.1	215.5	223.4	223.1	239.6	239.1	255.6	255.7	272.6	272.6
PLL_MON	L20	215.2	214.5	219.9	219.6	235.5	235.3	249.8	249.7	263.7	263.9
TOGGLE_MON	L22	214.9	214.3	222.1	221.0	237.9	237.3	253.6	253.0	269.3	268.6

Table. 31. LVTTL VOL – DUT 03020

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	215.2	214.5	223.0	222.2	242.4	241.5	260.8	259.9	279.9	278.8
EPCSRST_N_0	B31	214.8	214.7	223.1	224.3	243.2	245.8	262.6	266.9	282.3	288.3
EPCSRST_N_1	B32	212.8	212.1	220.3	219.5	239.1	238.2	256.4	255.5	274.3	273.3
EPCSRST_N_2	B34	213.9	213.0	221.8	220.7	241.6	240.7	260.0	258.8	279.0	277.5
EPCSRST_N_3	B35	214.1	213.2	220.7	219.5	239.4	238.2	256.4	254.9	274.0	272.6
EPCSRST_N_4	B36	215.5	214.4	223.9	222.8	245.4	244.2	265.1	264.0	285.5	284.1
EPCSRST_N_5	B37	215.0	214.0	222.5	221.2	242.2	241.2	260.9	259.6	280.0	278.5
MONITOR	K23	213.0	212.4	221.1	220.7	237.1	236.5	253.6	253.0	270.2	270.0
PLL_MON	L20	212.8	212.1	218.0	217.6	233.7	233.9	248.0	248.8	261.8	263.2
TOGGLE_MON	L22	212.8	211.7	220.4	219.0	236.3	235.4	252.1	251.1	268.0	266.9

Table. 32. LVTTL VOL – DUT 03032

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	216.9	215.2	225.2	223.5	244.8	242.6	263.5	261.7	282.7	280.6
EPCSRST_N_0	B31	216.7	214.8	225.3	223.6	245.4	243.7	264.9	263.0	284.7	282.8
EPCSRST_N_1	B32	215.2	213.7	222.6	220.6	241.2	239.4	258.9	257.2	277.0	275.1
EPCSRST_N_2	B34	217.2	215.3	225.0	223.0	244.9	243.0	264.0	261.8	283.2	280.9
EPCSRST_N_3	B35	216.8	214.8	223.5	221.5	242.1	239.8	259.7	257.1	277.3	274.6
EPCSRST_N_4	B36	218.1	216.0	226.3	224.2	247.4	245.1	267.7	264.8	287.9	284.7
EPCSRST_N_5	B37	217.2	215.1	224.8	222.6	244.1	242.1	263.0	260.6	281.9	279.2
MONITOR	K23	215.1	213.6	223.0	221.7	239.1	237.9	255.1	253.8	272.0	270.9
PLL_MON	L20	214.3	212.9	219.7	218.1	235.5	234.1	249.4	248.3	263.4	262.1
TOGGLE_MON	L22	214.7	213.1	221.6	219.8	237.6	235.8	252.9	250.9	268.8	266.5

Table. 33. LVTTL VOL – DUT 03043

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	217.1	215.8	225.7	224.2	244.8	243.0	263.5	261.5	282.7	280.4
EPCSRST_N_0	B31	216.3	215.8	225.2	224.9	245.5	245.8	265.2	265.9	285.0	286.3
EPCSRST_N_1	B32	215.5	214.2	222.5	221.1	240.9	240.0	258.5	257.6	276.4	275.8
EPCSRST_N_2	B34	216.6	215.4	224.4	222.8	244.0	242.4	262.7	260.6	281.7	279.3
EPCSRST_N_3	B35	215.8	214.7	223.1	221.5	241.4	239.7	258.6	256.7	276.3	274.3
EPCSRST_N_4	B36	217.1	215.6	225.4	223.9	246.8	245.1	266.4	264.5	286.7	284.6
EPCSRST_N_5	B37	216.4	215.0	224.0	222.5	243.4	242.1	262.1	260.9	281.0	279.4
MONITOR	K23	215.4	214.3	223.2	222.3	239.0	238.5	255.5	254.8	272.2	271.7
PLL_MON	L20	215.0	213.7	220.2	218.7	236.0	234.9	250.2	249.2	264.3	263.0
TOGGLE_MON	L22	215.0	213.8	221.7	220.2	237.9	236.7	253.3	252.2	268.9	267.7

E. Propagation Delay

Table 34 lists the pre-irradiation and post-irradiation propagation delay measurements. It shows that the change due to radiation on each DUT is not significant and every DUT passes the 10% degradation criterion.

Table. 34. Pre-irradiation and Post-irradiation Propagation Delay Change

DUT	Total Dose	Pre-irradiation (µs)	Post-irradiation (µs)	Change Degradation (%)
02937	125 krad	0.459	0.463	0.87
02963	125 krad	0.463	0.466	0.65
03018	125 krad	0.482	0.484	0.41
03020	125 krad	0.468	0.47	0.43
03032	125 krad	0.475	0.478	0.63
03043	125 krad	0.469	0.469	0.00

F. Transition Time

The figures below show the pre-irradiation and post-irradiation transitions edges. In each case the radiation induced transition degradation is not observable.

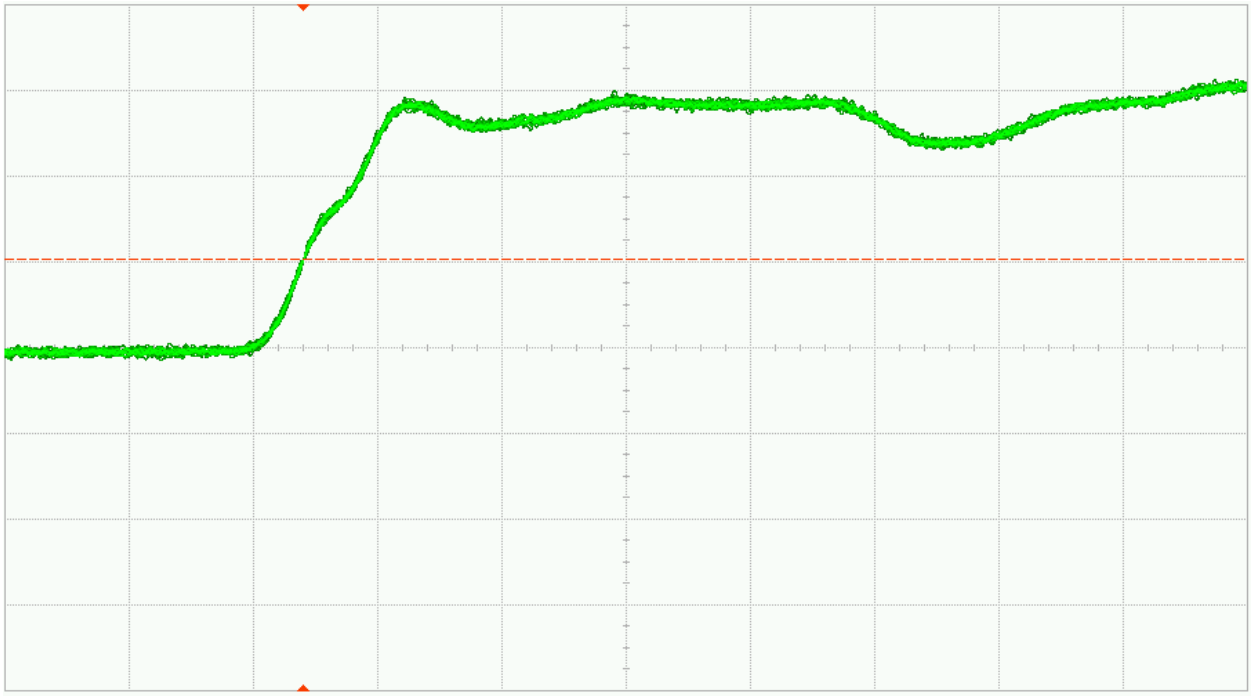

Fig. 26 (a). DUT 02937 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

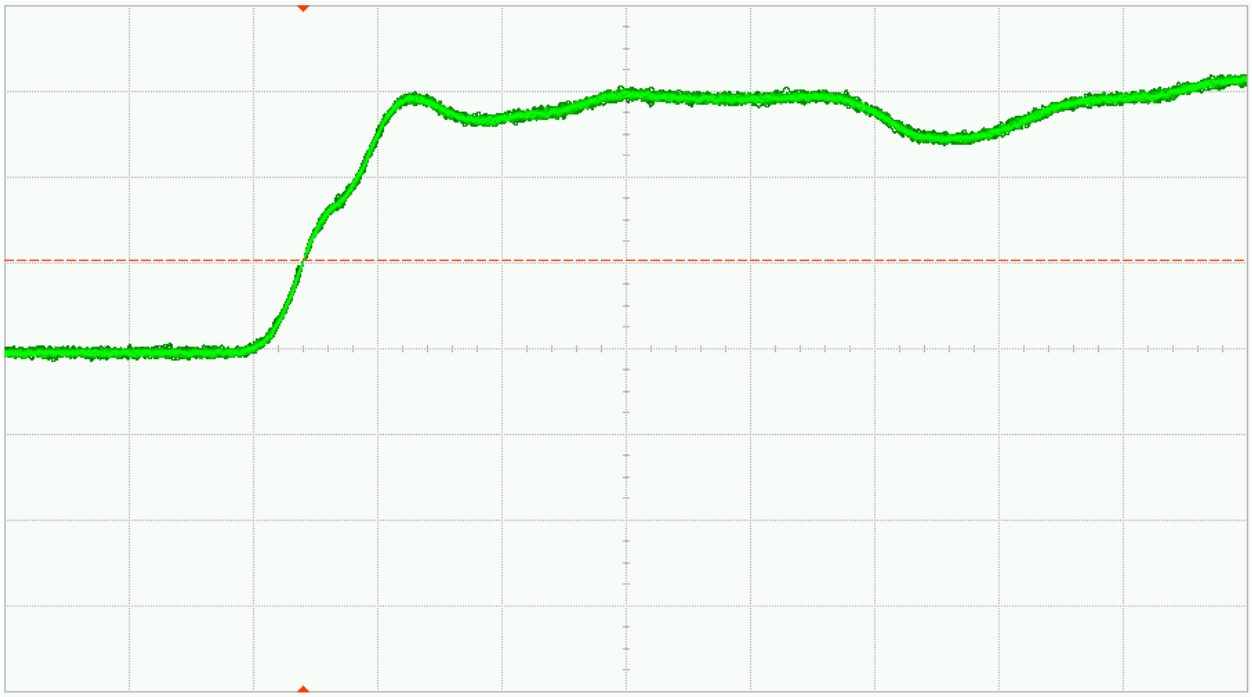

Fig. 26 (b). DUT 02937 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

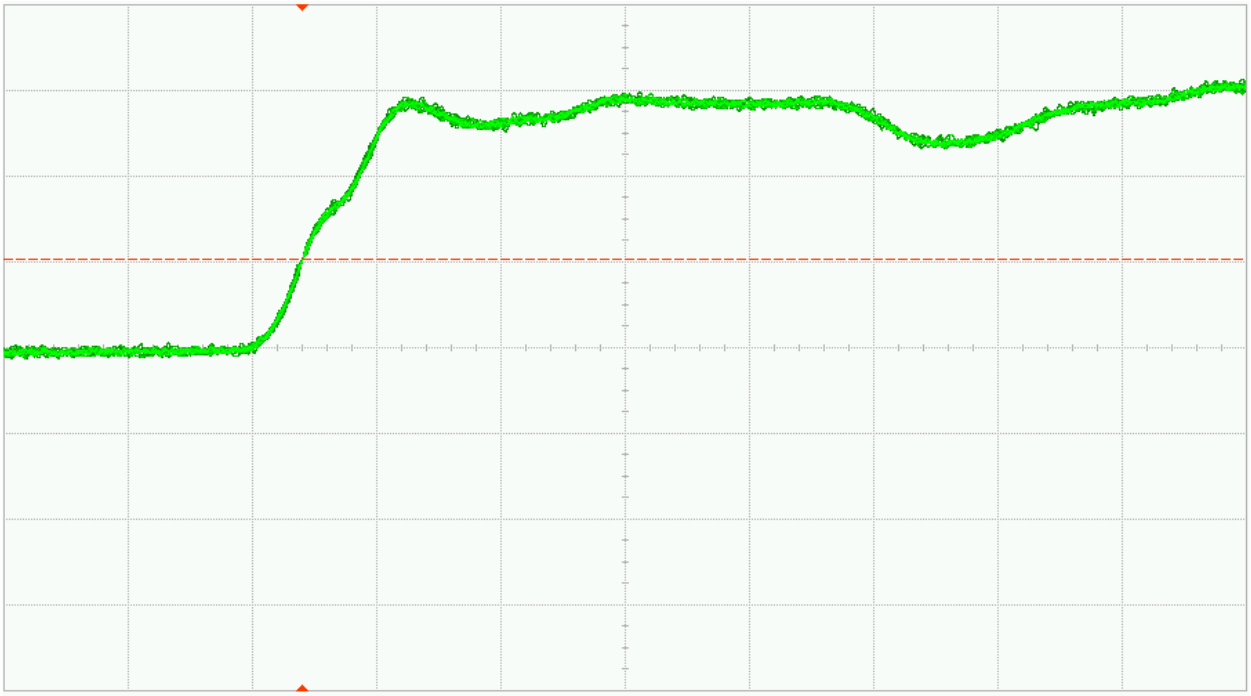

Fig. 27 (a). DUT 02963 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

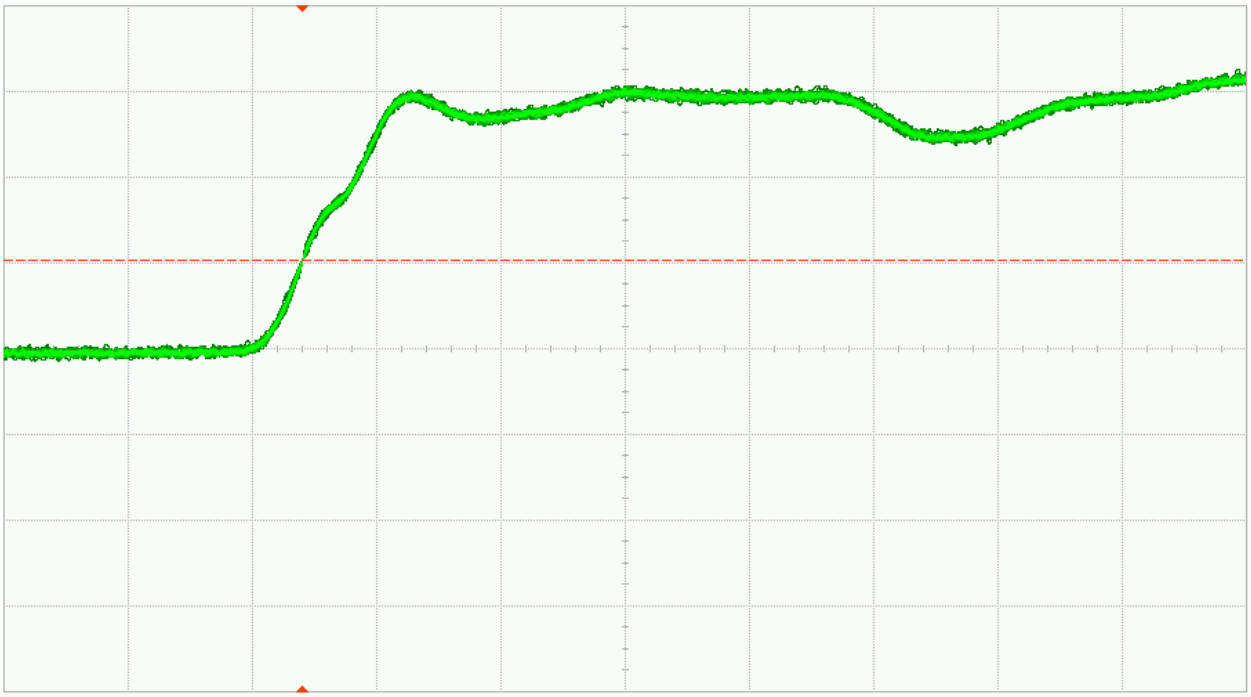

Fig. 27 (b). DUT 02963 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

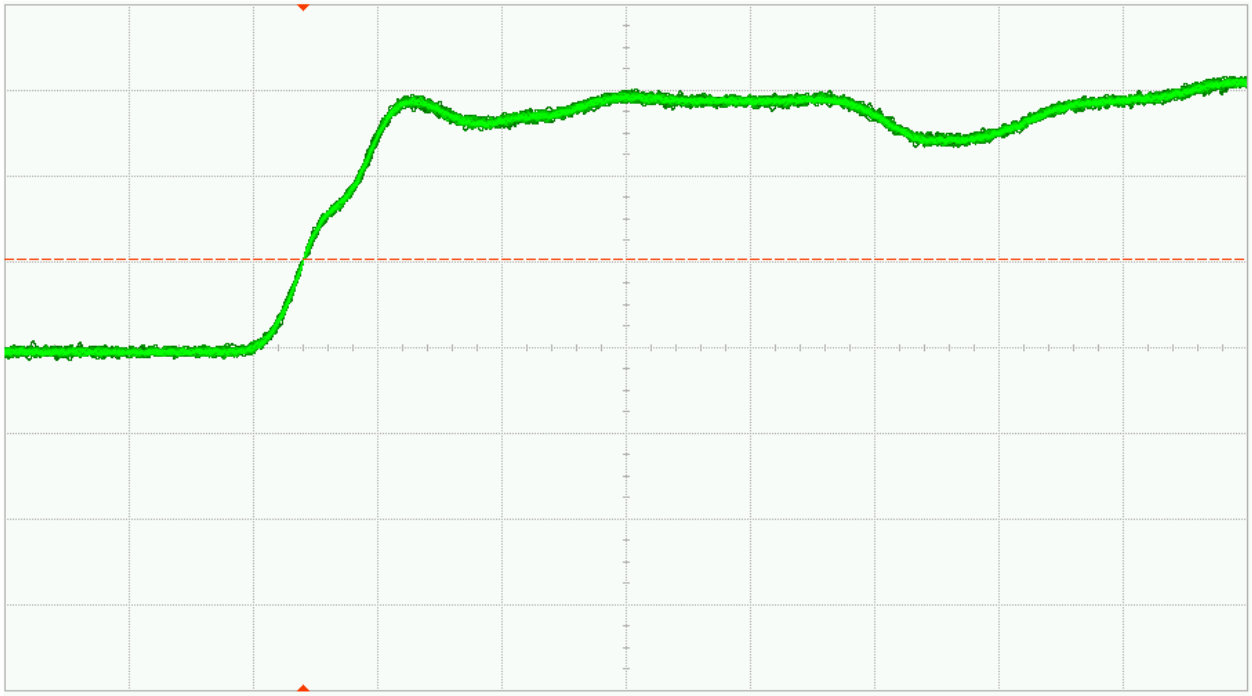

Fig. 28 (a). DUT 03018 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

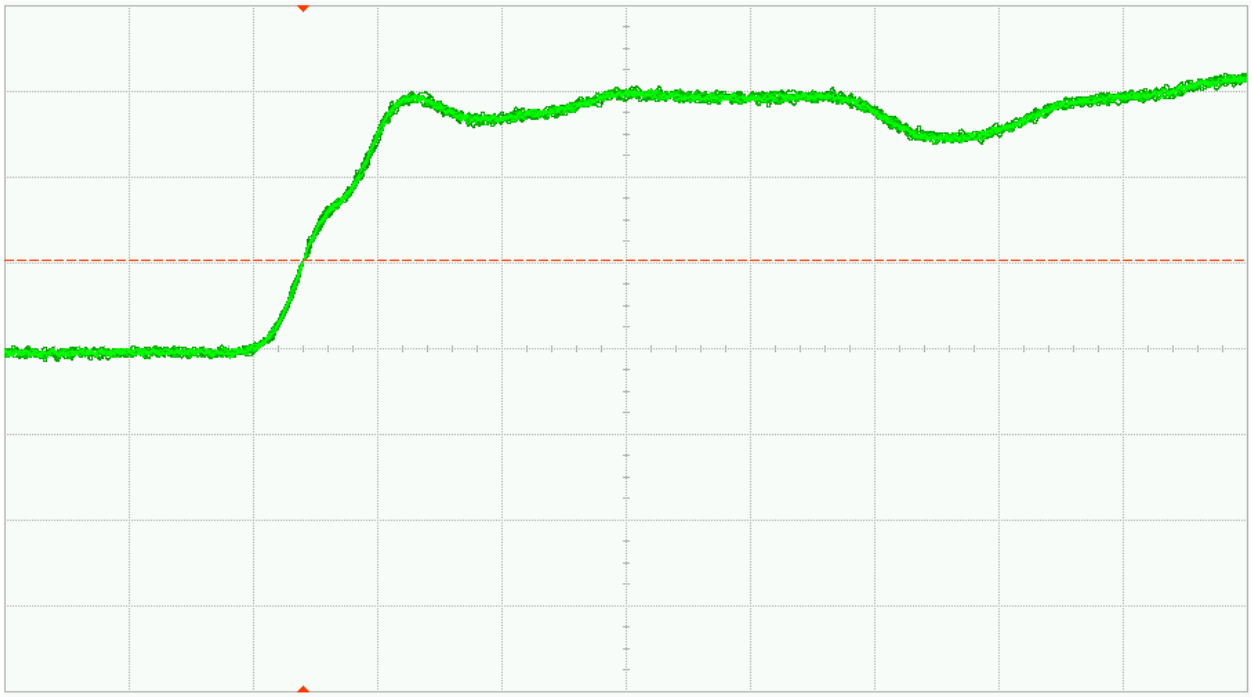

Fig. 28 (b). DUT 03018 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

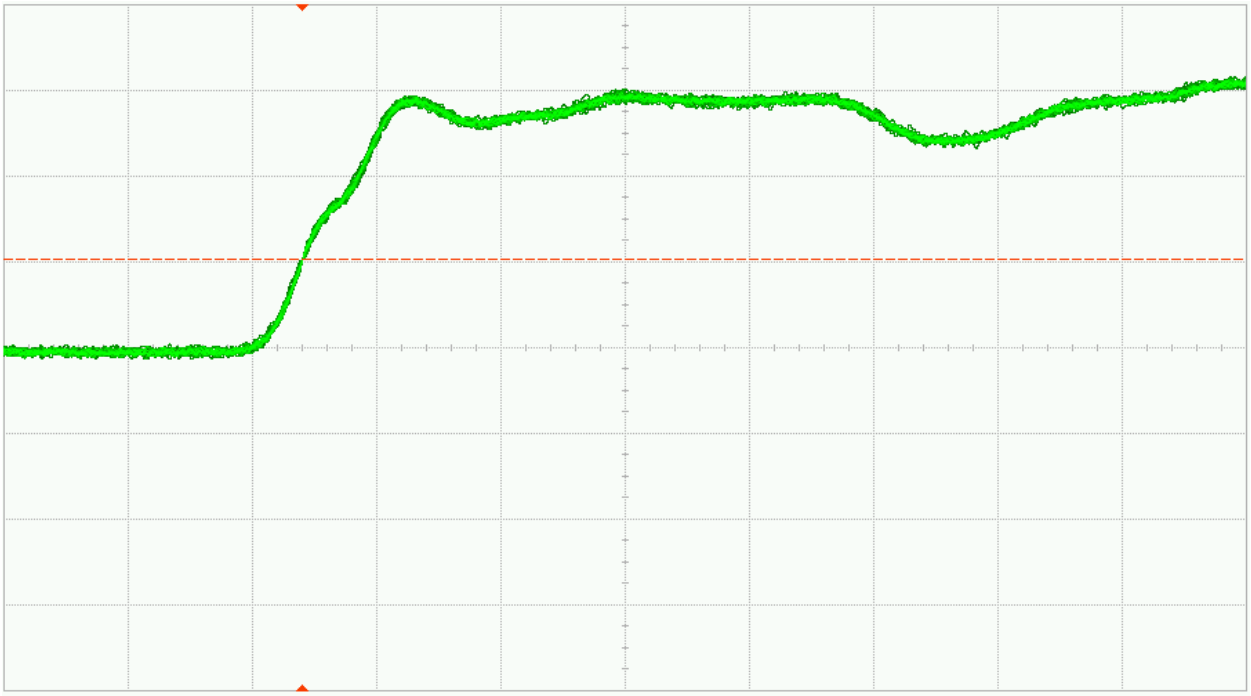

Fig. 29 (a). DUT 03020 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

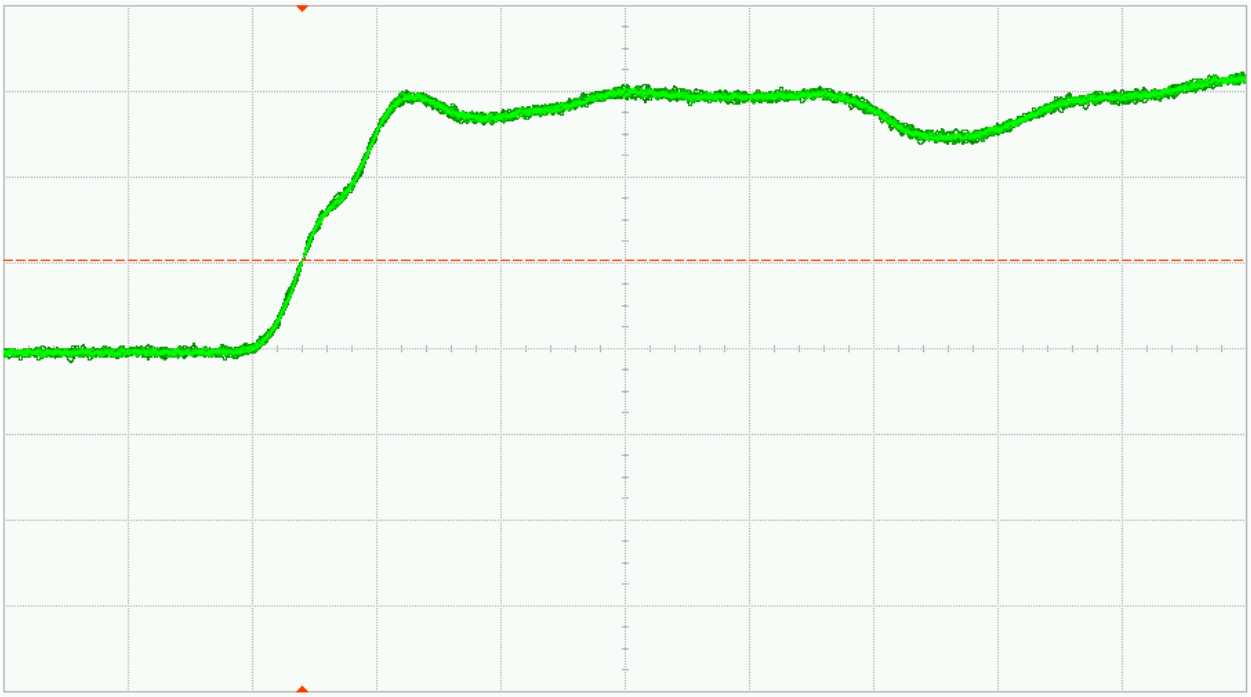

Fig. 29 (b). DUT 03020 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

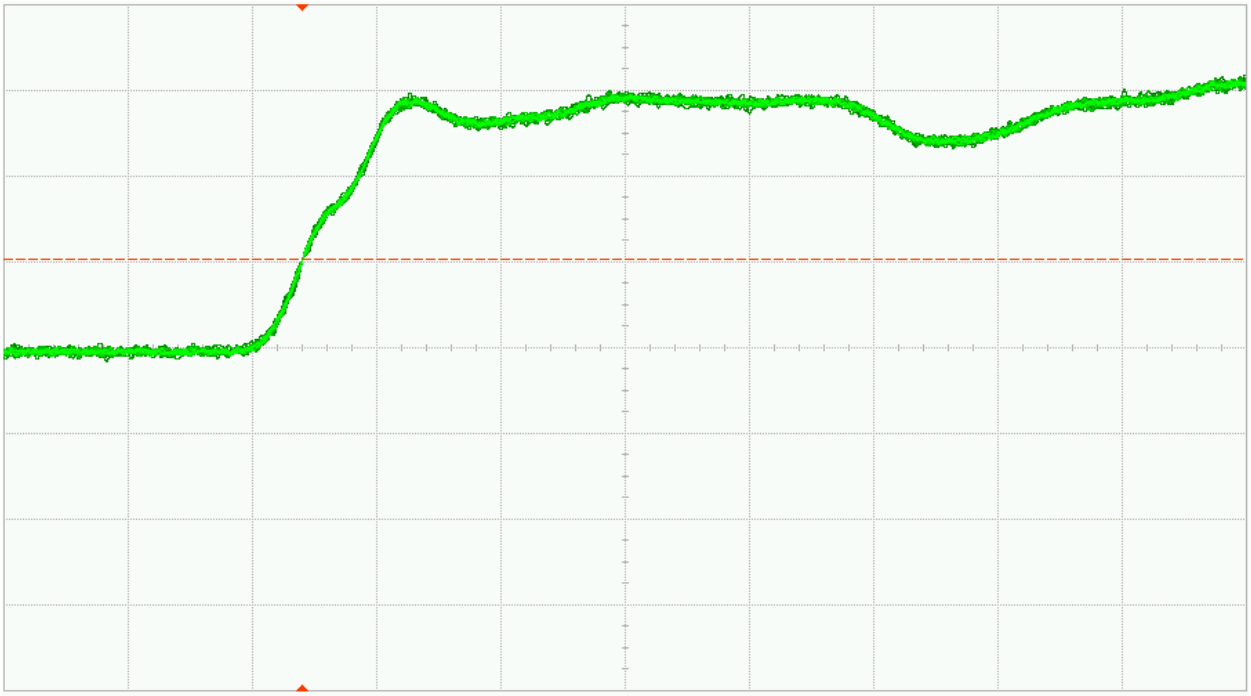

Fig. 30 (a). DUT 03032 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

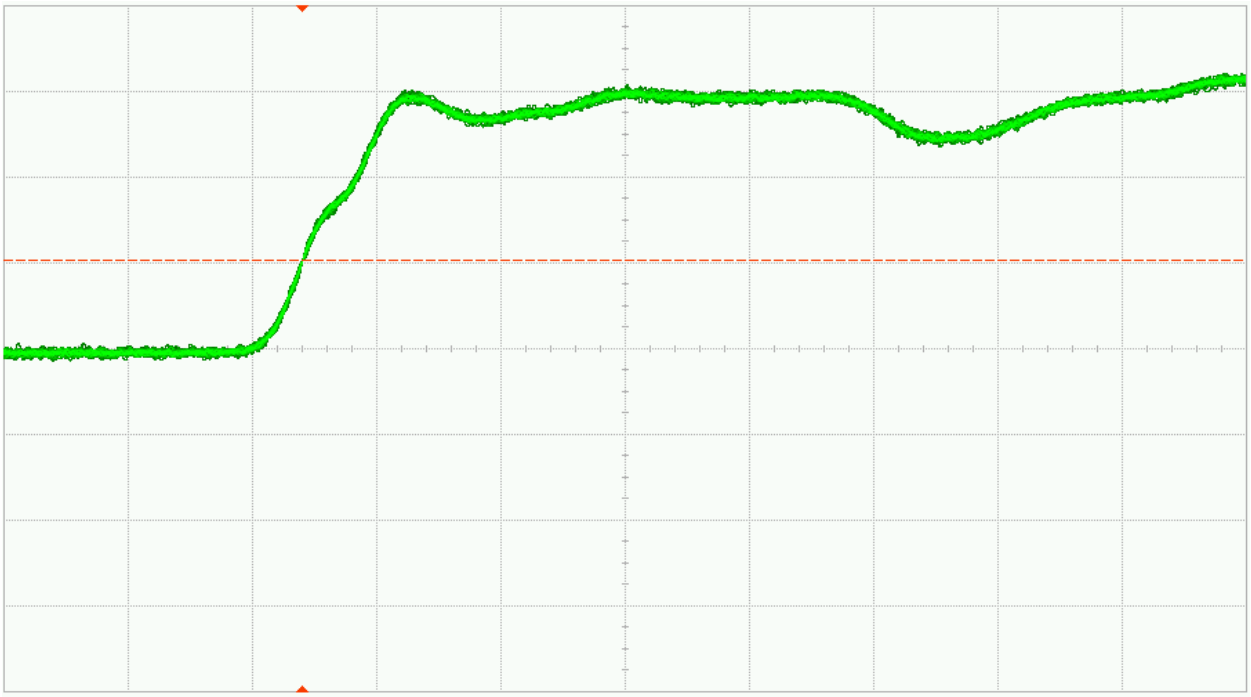

Fig. 30 (b). DUT 03032 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

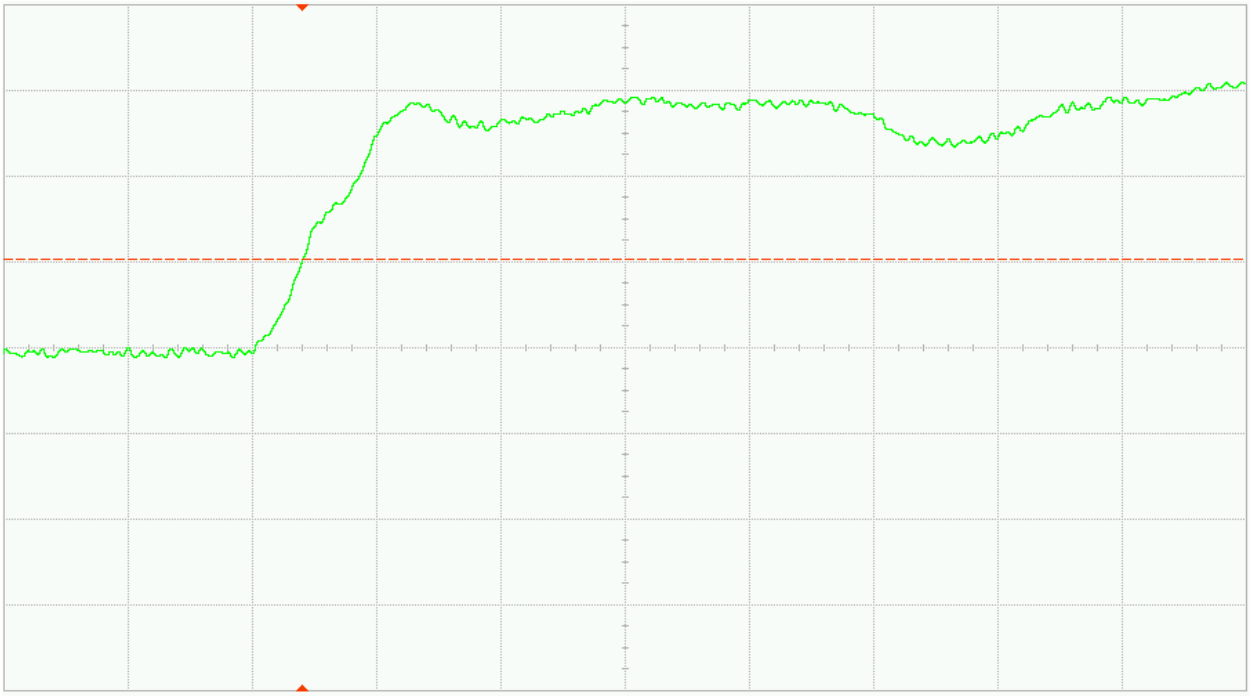

Fig. 31 (a). DUT 03043 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

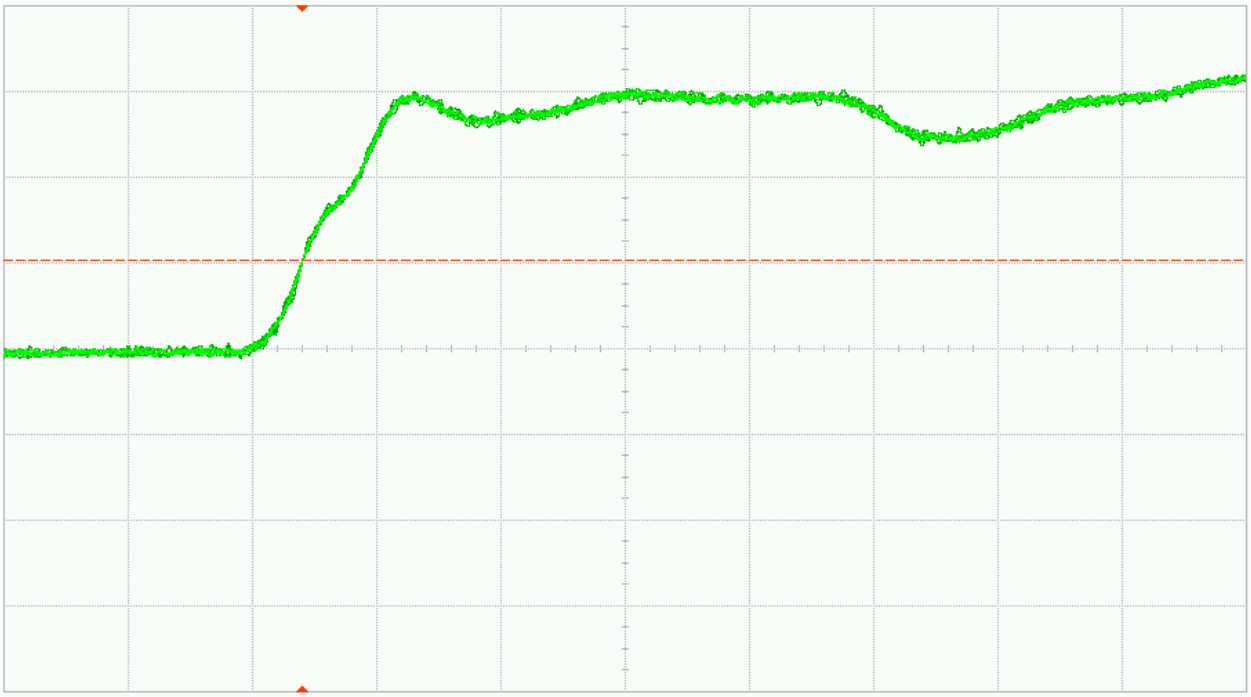

Fig. 31 (b). DUT 03043 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

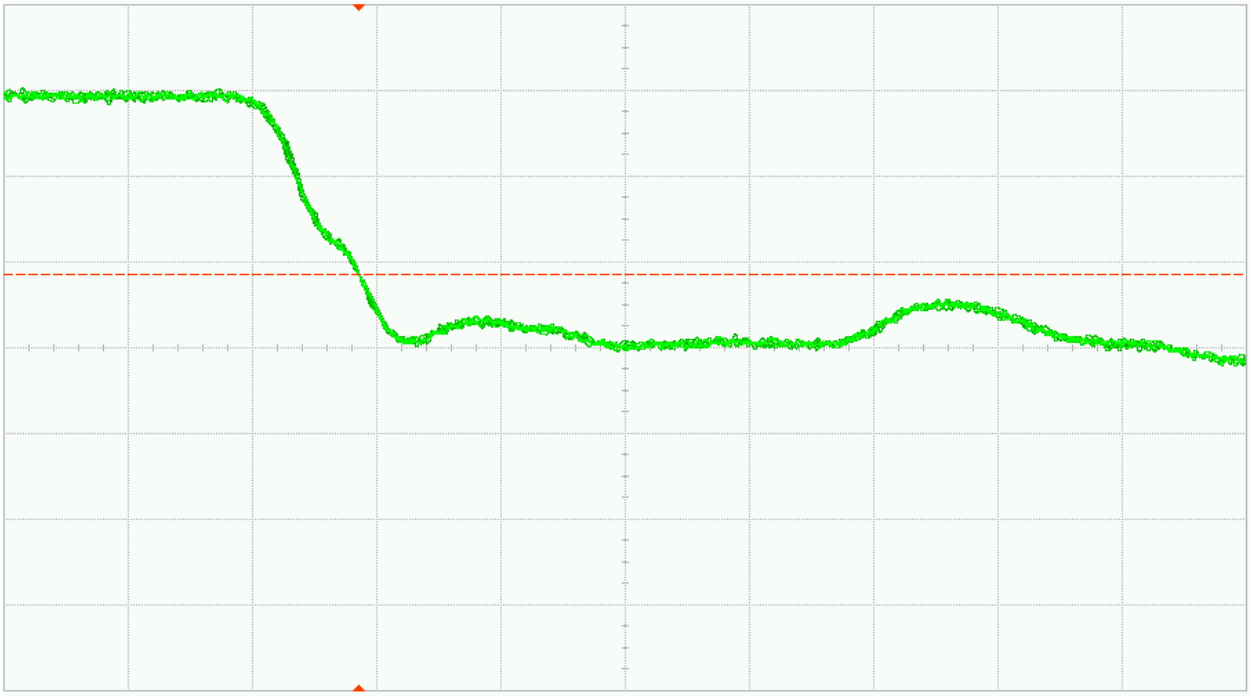

Fig. 32 (a). DUT 02937 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

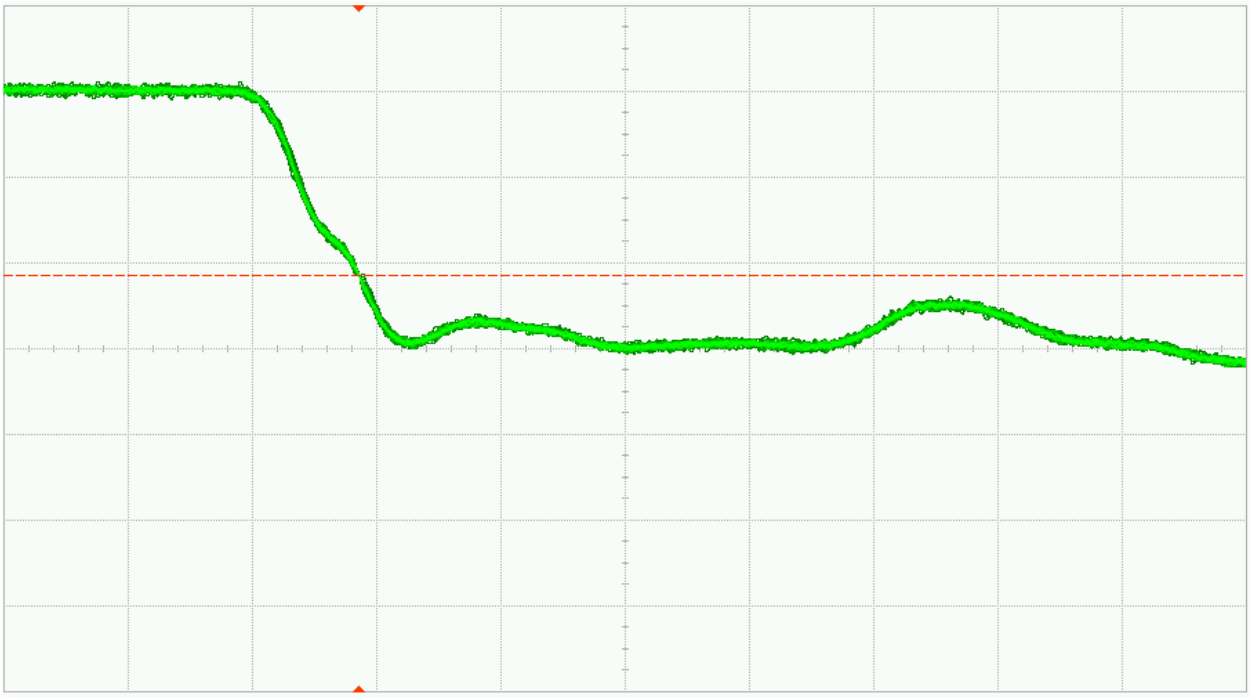

Fig. 32 (b). DUT 02937 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

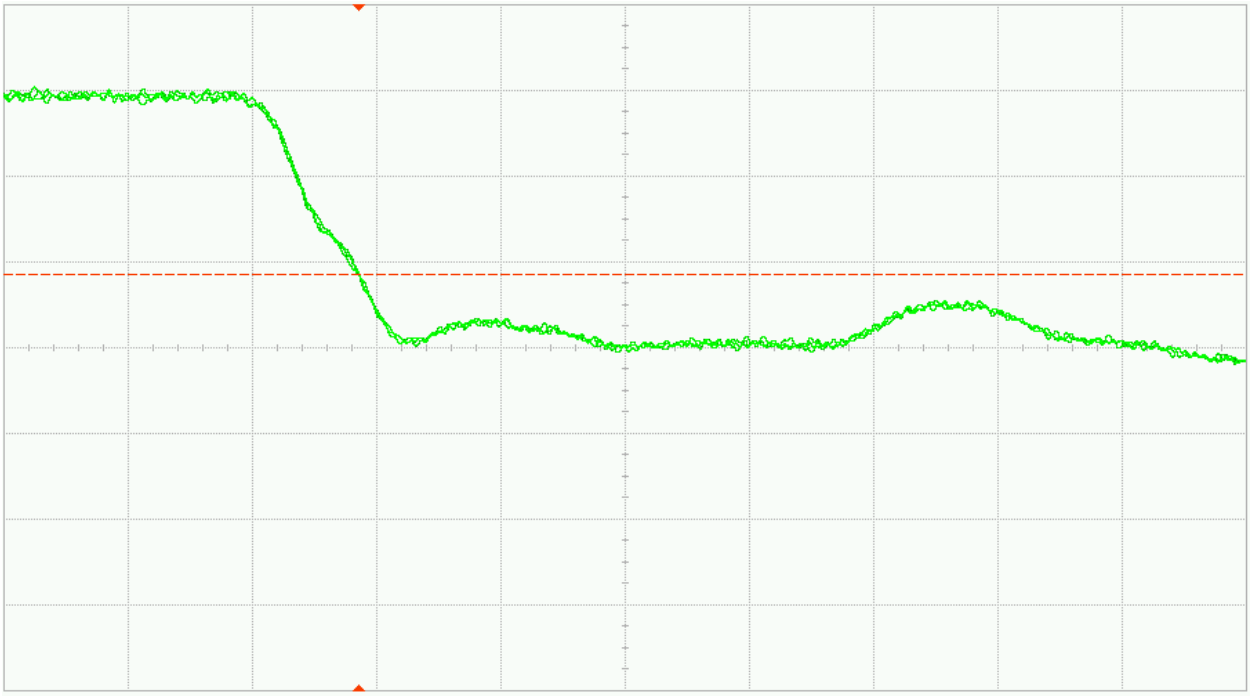

Fig. 33 (a). DUT 02963 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

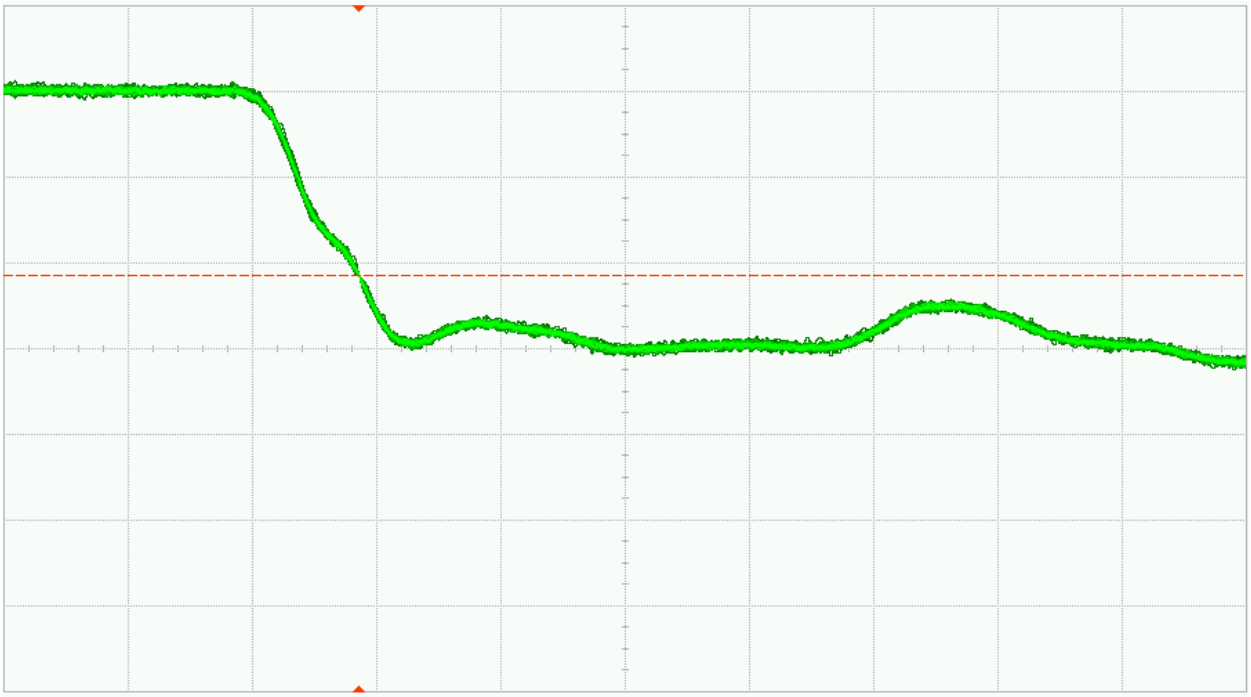

Fig. 33 (b). DUT 02963 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

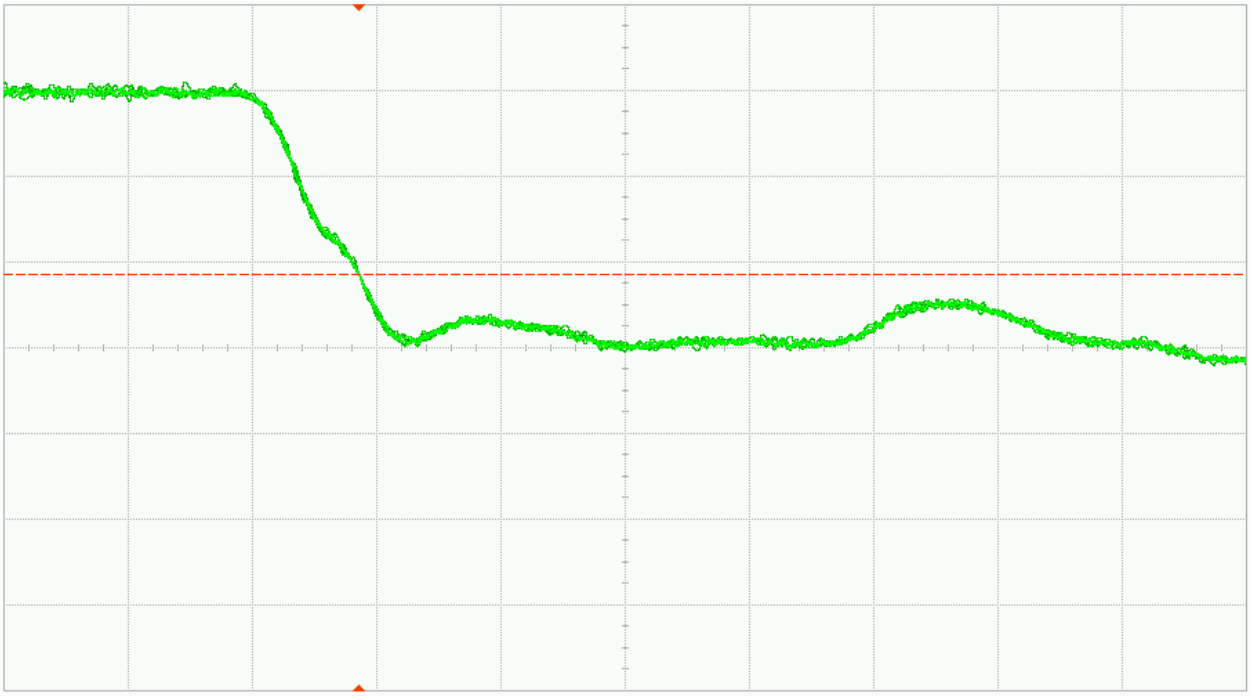

Fig. 34 (a). DUT 03018 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

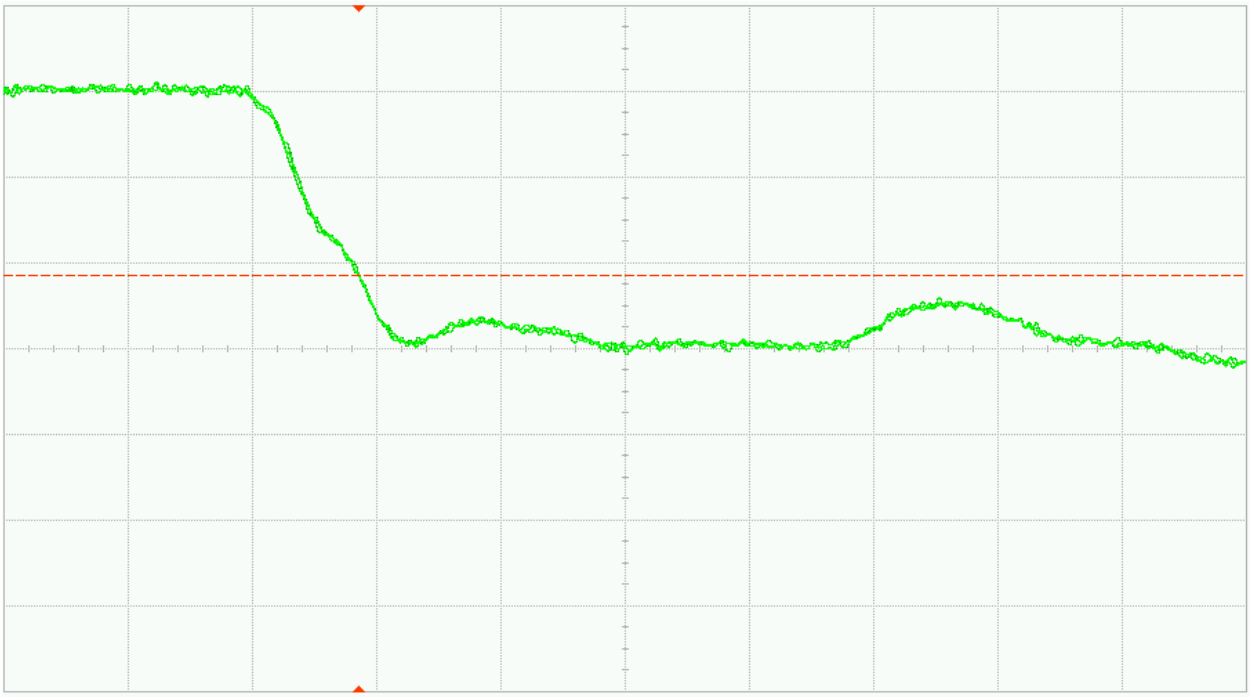

Fig. 34 (b). DUT 03018 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

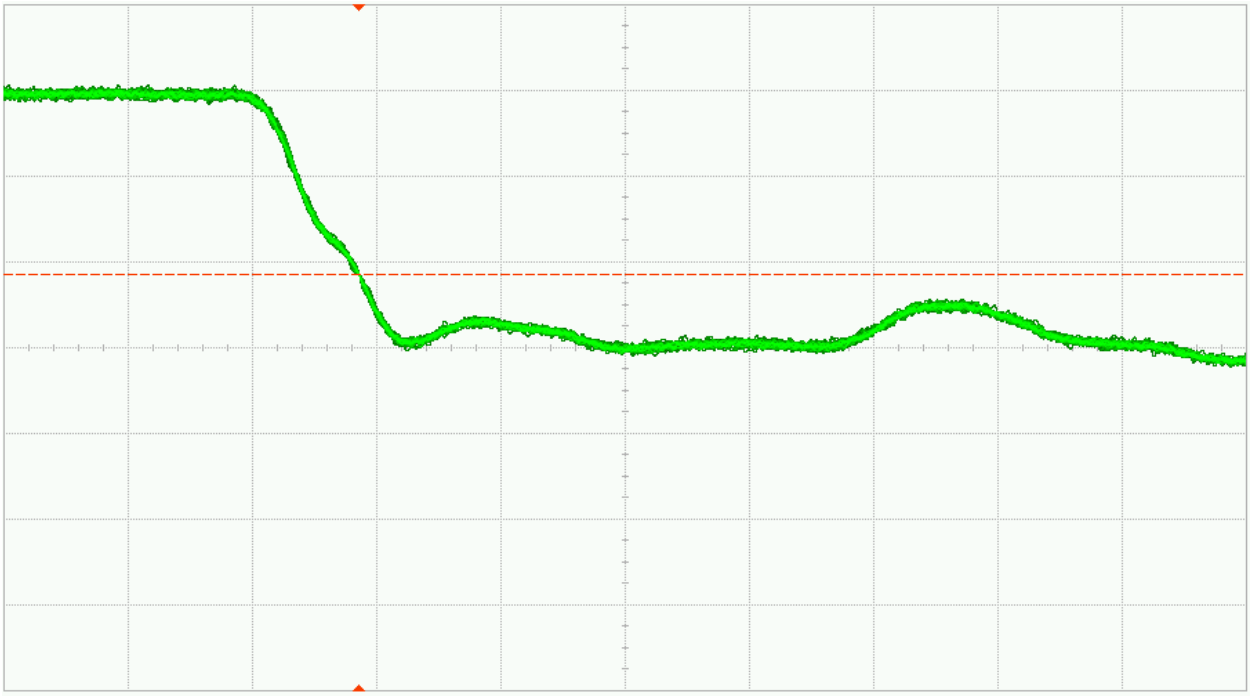

Fig. 35 (a). DUT 03020 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

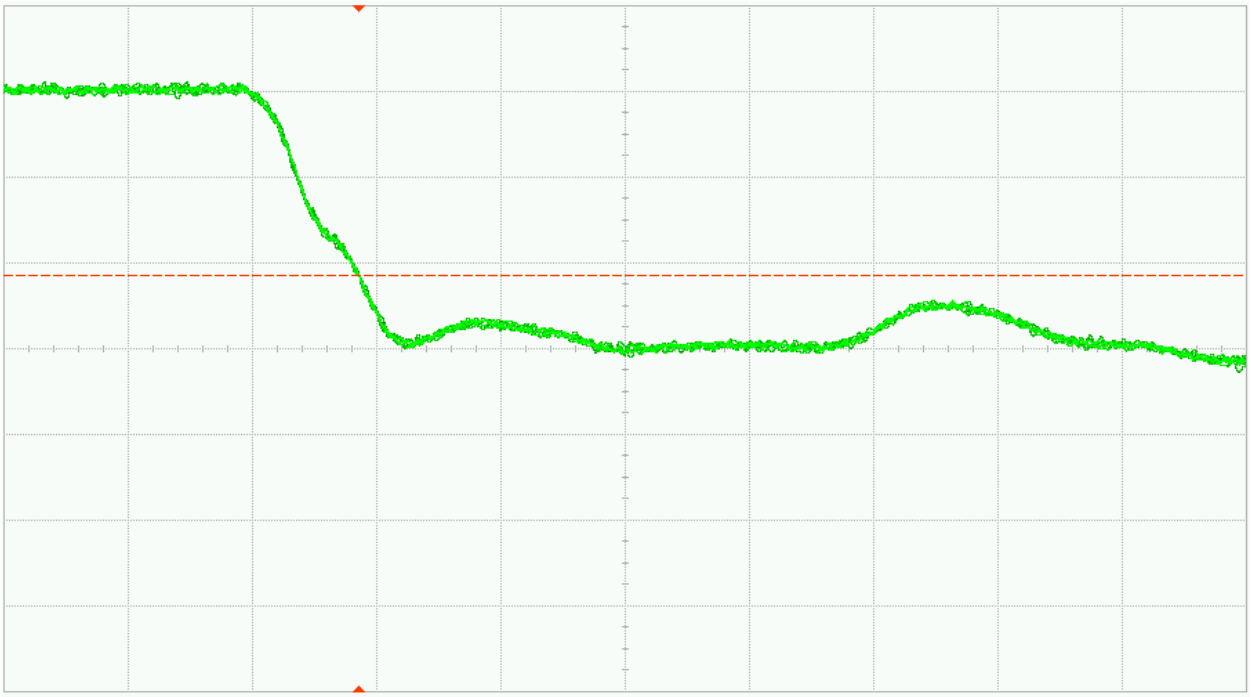

Fig. 35 (b). DUT 03020 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

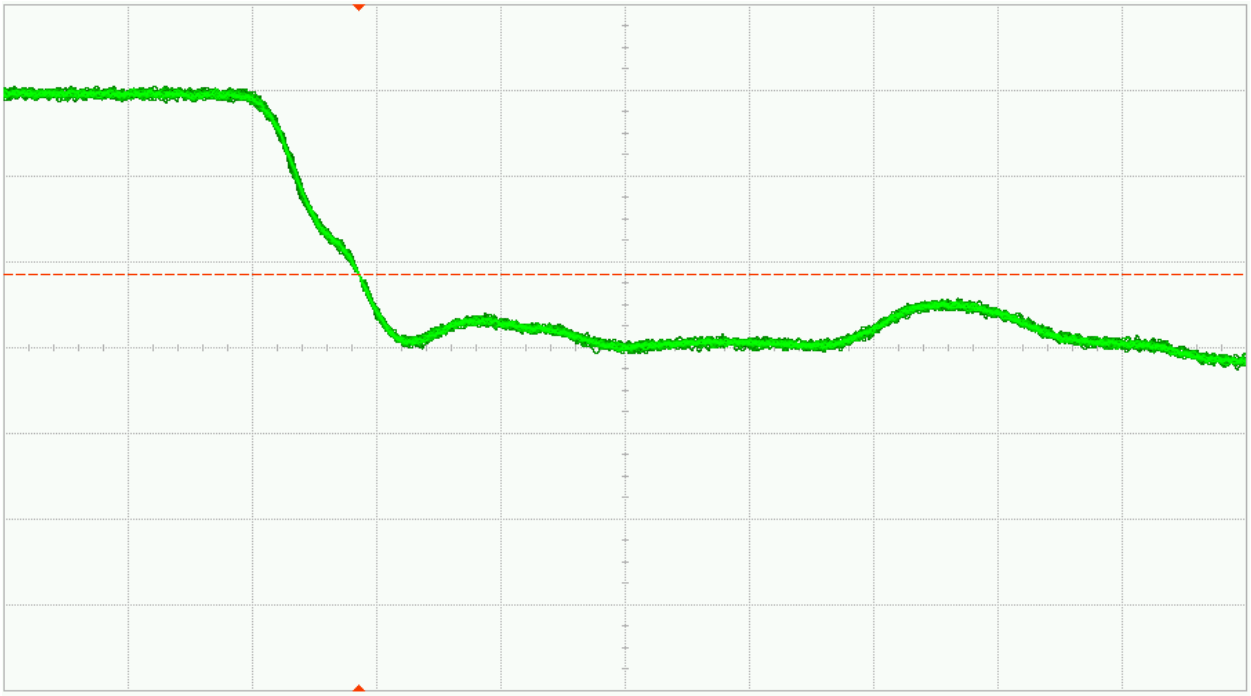

Fig. 36 (a). DUT 03032 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

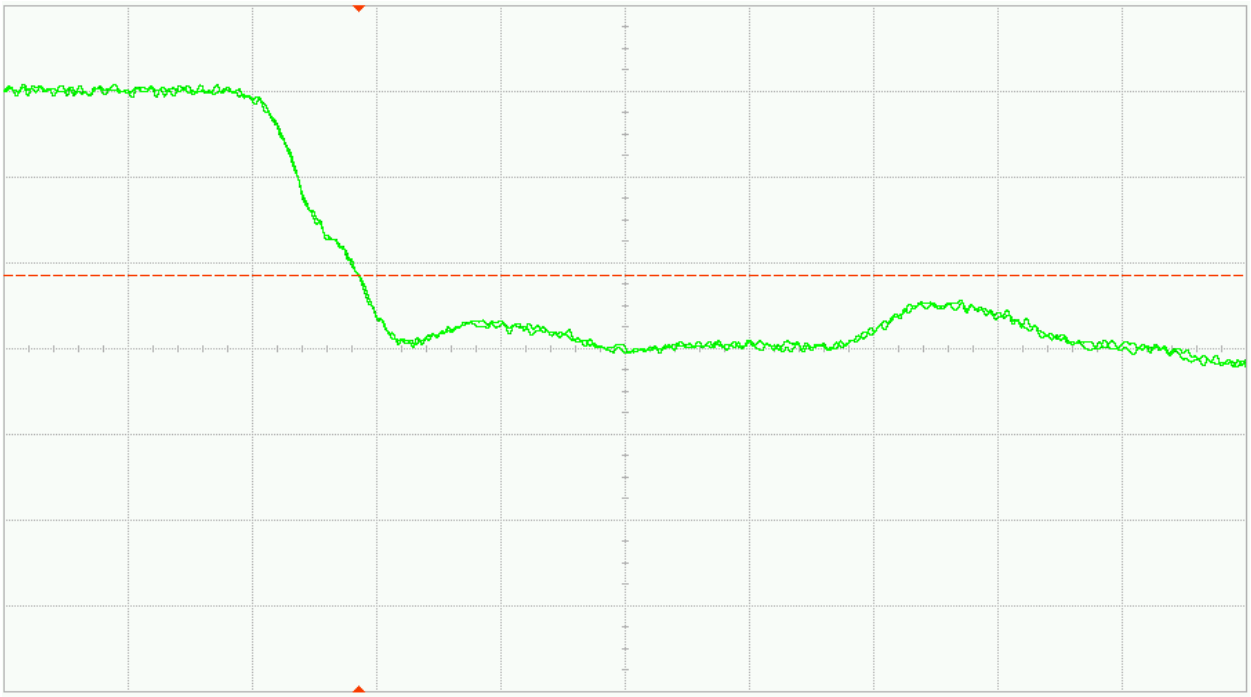

Fig. 36 (b). DUT 03032 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

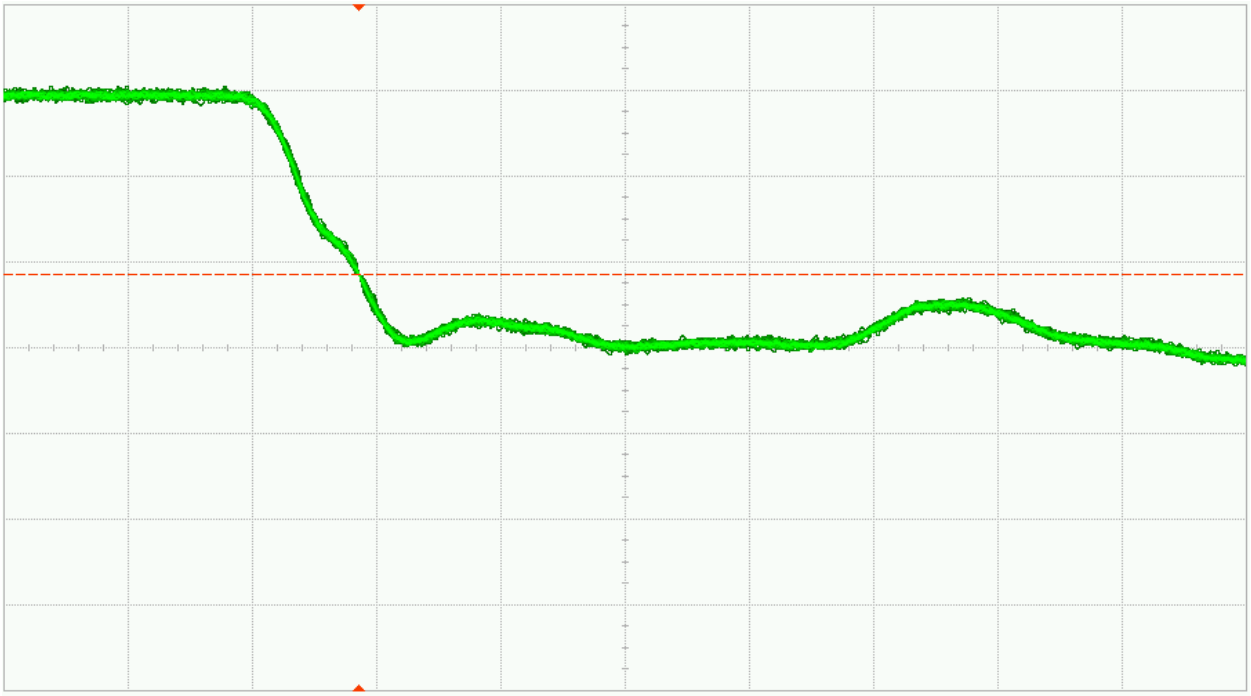

Fig. 37 (a). DUT 03043 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

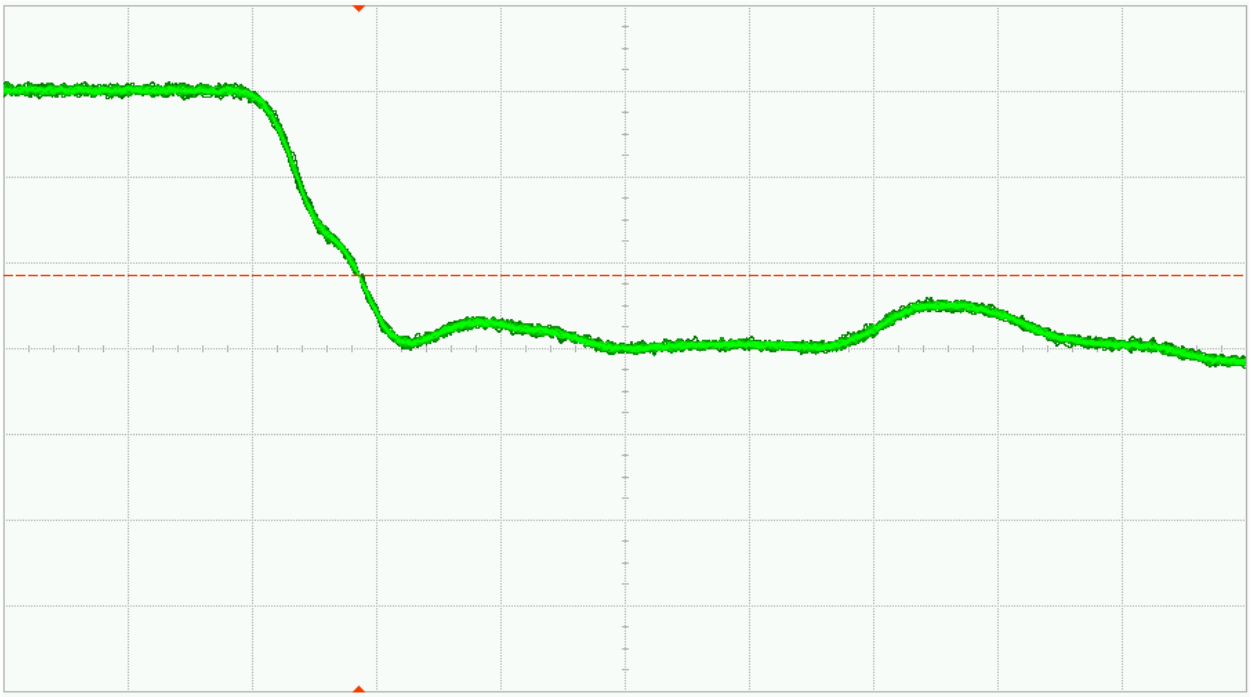

Fig. 37 (b). DUT 03043 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Appendix A

Table. 35. High level block diagrams of blocks used to perform fabric functional coverage pre and post-irradiation

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
IO Block	IO utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

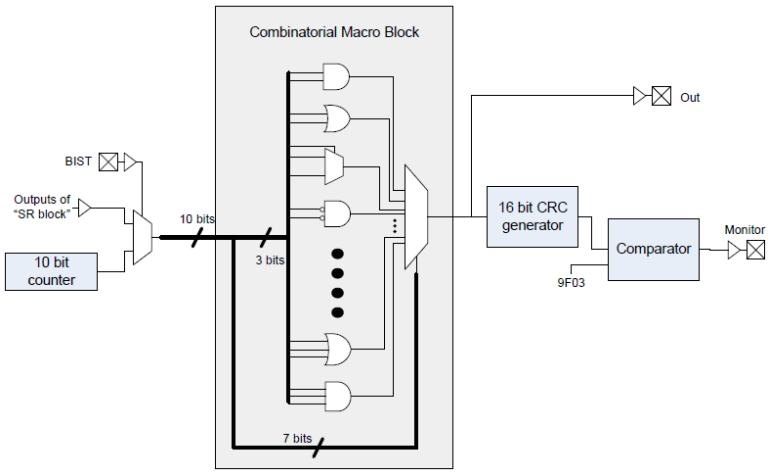

Fig. 38. Combo Block

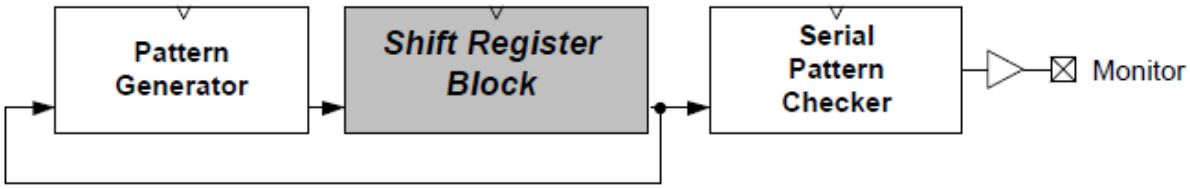

Fig. 39. Shift Register Block

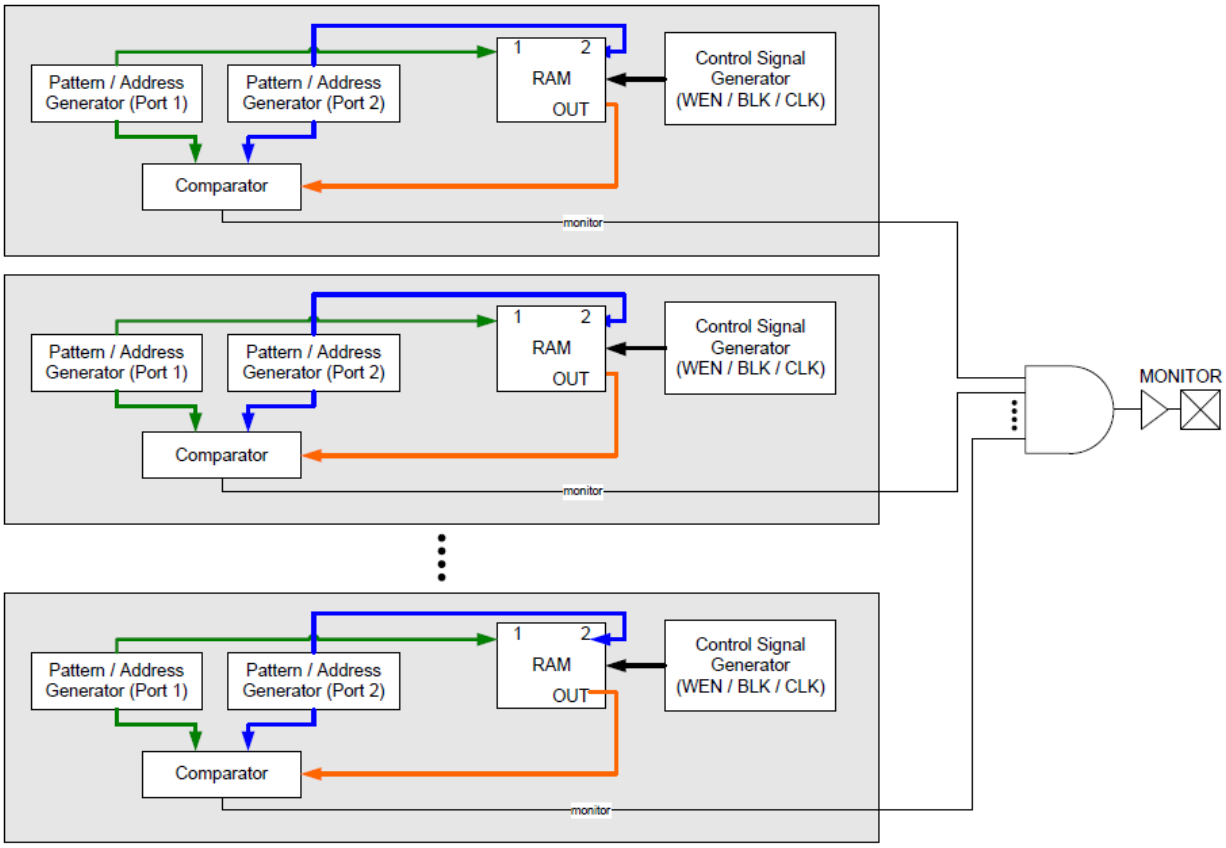

Fig. 40. Embedded Ram Blocks

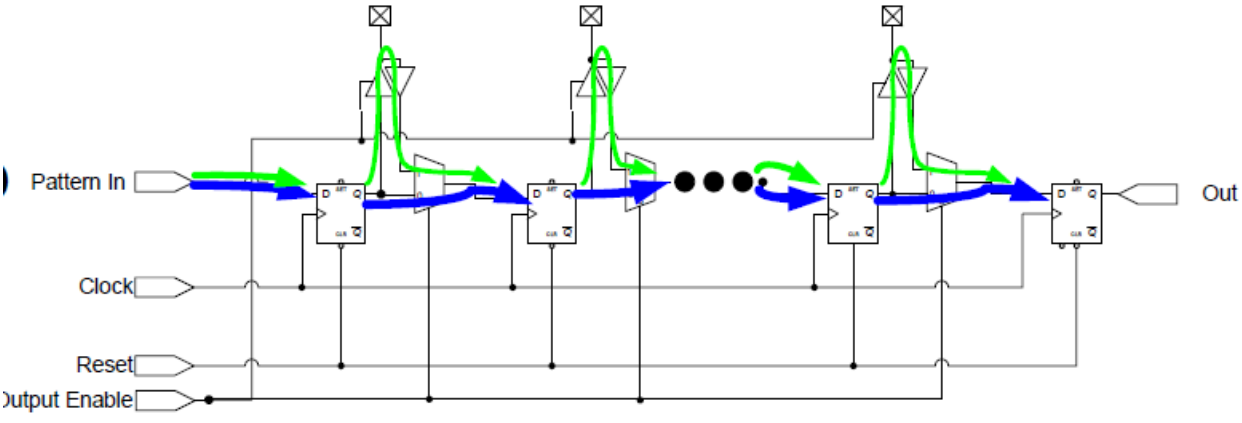

Fig. 41. IO Block

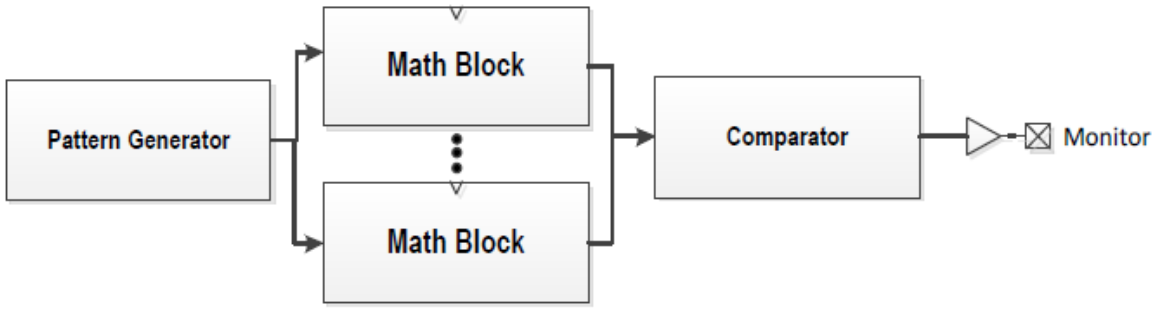

Fig. 42. Math Block

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