Release Notes
Libero IDE v9.2 SP4

Introduction (Ask a Question)

Thank you for your interest in Microchip's Libero Integrated Design Environment (IDE) v9.2 SP4.

System Requirements (Ask a Question)

See the System Requirements on the web for more information regarding operating system support and minimum system requirements.

Libero IDE v9.2 and its service packs require runtime components of Microsoft Visual C++ libraries. If a Libero IDE application fails to start, download and install one of the following packages:

- For 32-bit architecture install Microsoft Visual C++ 2008 SP1 Redistributable Package (x86)
- For 64-bit architecture install Microsoft Visual C++ 2008 SP1 Redistributable Package (x86)

Setup instructions for Red Hat Enterprise Linux OS can be found on the Libero IDE Documents webpage.

Note: All tools within the Libero IDE software suite only support installation, execution, and project manipulation on disk partitions that are 2 TB or smaller. If either the Libero install, the HOME directory or the Libero project folder is located on a partition that is larger than 2 TB, file access errors or tool crashes might occur.

Download Libero IDE v9.2 SP4 (Ask a Question)

Important: Libero IDE v9.2 SP4 is a full installer that includes Libero IDE v9.2 , Libero IDE v9.2 SP1, Libero IDE v9.2 SP2, Libero IDE v9.2 SP3 installers. You do not need to install Libero IDE v9.2 and its service packs separately if you install Libero IDE v9.2 SP4 software.

Download Libero IDE v9.2 SP4 from the Libero IDE downloads page.

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1. What's New (Ask a Question)

1.1 Libero IDE v9.2 SP4 (Ask a Question)

Libero IDE v9.2 SP4 includes:

- Linux RHEL 7 support
- CentOS7 support
- New versions of Synplify Pro AE P-2019.03A-SP1 (Windows and Linux) and Identify AE P-2019.03A-SP1 (Windows only)

1.2 Libero IDE v9.2 SP3 (Ask a Question)

Libero IDE v9.2 SP3 includes:

- The Global Set Fuse option is removed from the Generate Programming Files UI in this service pack, which eliminates the option to use internal Power-on Reset circuits to establish flip-flop states at power-up. To correctly establish the power-up states of flip-flops, Microchip recommends the use of an external Power-on Reset circuit.
- Fixes for the SDF back annotated simulation.

1.3 Libero IDE v9.2 SP2 (Ask a Question)

Libero IDE v9.2 SP2 includes:

- Use of the ProASIC®3 A3PE1500 for RT prototyping with the Free Gold license
- New MX packages for customers migrating from ACT1 and ACT2 devices

1.4 Libero IDE v9.2 SP1 (Ask a Question)

Libero IDE v9.2 SP1 includes:

- Use of the ProASIC®3 A3PE3000 for RT prototyping with the Free Gold license
- Fixes a Designer runtime error introduced in v9.2
- Allows A3PE high-effort layout for RT prototyping

1.5 Libero IDE v9.2 (Ask a Question)

Libero IDE v9.2 includes timing enhancements for RTAX™-S/SL/DSP and Axcelerator® FPGA families. This version also updates the routing of long delay lines in RTAX4000S/SL/DSP FPGAs and adds a new design rule check to RTAX-S/SL/DSP pipeline SRAM

1.5.1 ACT-to-MX Migration Table (Ask a Question)

A Tcl script is available to facilitate your design migration. To download the Tcl script, see Application Note AC399 and Application Note AC405.

Table 1-1. ACT1/40MX

ACT1		40MX	
A1010B	84 CPGA	A40MX02	84 CPGA
A1020B	84 CPGA	A40MX04	84 CPGA
A1020B	84 CQFP	A40MX04	84 CQFP

Table 1-2. ACT2/42MX

ACT2		42MX	
A1240A	144 PQFP	A42MX09	144 PQFP
A1240A	132 CPGA	A42MX09	132 CPGA
A1280A	172 CQFP	A42MX16	172 CQFP

.....continued			
ACT2		**42MX**	
A1280A	176 CPGA	A42MX16	176 CPGA

1.5.2 New Implementation of Min-Max Timing Analysis for RTAX™-S/SL/DSP FPGAs (Ask a Question)

Libero IDE v9.2 includes timing enhancements for Hold Check under Worst Case and Setup Check under Best Case timing analysis for RTAX™-S/SL/DSP and Axcelerator FPGAs. Please read Application Note AC395: RTAX-S/SL/DSP Timing Analysis Using Libero IDE v9.2 for details. This document describes a detailed max-min analysis of the external setup and hold time and clock-to-output time for a synchronous design implemented in Microsemi RTAX™- S/SL/DSP FPGAs. We recommend four-corner timing analysis on RTAX-S/SL/DSP and AX designs. See Customer Notification CN1410.

1.5.3 Routing Change for RTAX4000S and RTAX4000 (Ask a Question)

Libero IDE 9.2 implements a routing constraint on RTAX4000S and RTAX4000D designs. The router will not create connections using more than four unbuffered long lines. This change to routing behavior is intended to avoid long propagation delays in RTAX4000S and RTAX4000D designs. For more information, see Customer Notification CN1412.

1.5.4 AX/RTAX-S/RTAX-D Pipeline SRAM Issue (Ask a Question)

Libero IDE v9.2 provides a new SRAM design rule check (DRC) put in place for RTAX and AX designs. This check will prevent the usage of a pipeline SRAM configuration which can result in a race condition in the SRAM. For more information, see Customer Notification CN1411.

1.5.5 Designer is No Longer Available from the Programs > Microsemi Libero IDE v9.2 List (Ask a Question)

Select **Libero IDE v9.2**.

Alternatively, you can double-click `<installation_path>\Microsemi\Libero_v9.2\Designer\bin\designer.exe`.

2. Software Fixes and Enhancements (Ask a Question)

2.1 Libero IDE v9.2 SP4 (Ask a Question)

The following table lists the software fixes and enhancements in Libero IDE v9.2 SP4.

Table 2-1. Software Fixes and Enhancements in Libero IDE v9.2 SP4

Family	Description
All	RHEL 7 support for Libero IDE: C-set was rejected.
AX	`IOPAD_BI` bibuf timing shows zero delay on D-to-Y and E-to-Y.
RTAXS	Add design-specific export of IBIS model for RTAX250S.
RTAX	Make 4-corner analysis requirement easier and more obvious after layout is complete.
AX RTAXS	When layout is complete, generate a timing violation report that covers all 4-corners.

2.2 Libero IDE v9.2 SP3 (Ask a Question)

The following table lists the software fixes and enhancements in Libero IDE v9.2 SP3.

Table 2-2. Software Fixes and Enhancements in Libero IDE v9.2 SP3

Customer Case	Description
493642-1764988552	Presynthesis simulation of Two Port RAM is not as expected.
493642-1800456531, 493642-1858459527	Designer Generate 0.00 as min time for RTSX-SU.
493642-1869957150	RTSX72SU simulation issue.
493642-1874661784	No ref clk available when create a generated clk.
493642-1911587871	Exporting SmartTime `.sdc` timing constraints after compile step gets appended with additional paths.
493642-1743158292	RTAX/AX: Remove global set fuse selection option from Generate Programming Files UI.
493642-2053959082	ARTSX-SU post-layout SDF shows 0 delay for all macros in best case.

2.3 Libero IDE v9.2 SP2 (Ask a Question)

The following table lists the software fixes and enhancements in Libero IDE v9.2 SP2.

Table 2-3. Software Fixes in Libero IDE v9.2 SP2

Customer Case	Summary
493642-1668140385	SXS SDC: TDPR crashes if length of clock constraint exceeds 100 chars.
	Incorrect SDC conversion.
493642-1676544432,493642-1720933183	9.2SDF does not match Tmin best number.
493642-1657158666	Timing report has incorrect External Setup with EMD.
	SmartPower reports 1/2 power for RTAX LVDS I/Os.
	Add A3PE1500 for RT Prototyping.

2.4 Libero IDE v9.2 SP1 (Ask a Question)

The following table lists software fixes and enhancements in Libero IDE v9.2 SP1.

Table 2-4. Issues Fixed in Libero IDE v9.2 SP1

Case Number	Description
57490	Fixes a v9.2 problem that prevents running high-effort layout for A3PE devices.

.....continued	
Case Number	**Description**
57773	Fixes runtime error when executing Designer in Libero IDE 9.2 using Gold license.
56282	Add A3PE3000 to the free Libero Gold license.

2.5 Libero IDE v9.2 (Ask a Question)

The following table lists the software fixes and enhancements in Libero IDE v9.2. We recommend you to see your Technical Support Hotline Case Number for more information.

Table 2-5. Software Fixes and Enhancements in Libero IDE v9.2

Case Number	Product	Summary
1-40412951	Synopsys	Need attribute to control AX DFM* macro inference.
489394-107140793 489394-178835093 493642-30133523 493642-32925603 493642-559503196	VHDL Library	Inconsistent data in the DP RAM when the data is read back out..
489394-198764592	SmartTime	Running data sheet report in SmartTime corrupts timing data in subsequent analysis.
489394-399717782	Misc	RHEL6-Request for newer MOTIF Library Support in Libero Linux.
493642-1028036568	Timing	RTAX-S/SL/DSP External Setup decreased when temperature increased.
493642-1063001761	Designer	Creating ANTIFUSESTATS report causes different AFM file.
493642-1196381888	Compile	Libero v9.1 SP5 Designer crashes when an ADB created with Libero 9.1.3 is opened.1
493642-1215350914	Designer	Designer crash during layout stage..
493642-1215350914	Designer	Excessively long instance names causes crash during layout.
493642-1219970789	Designer	RTSX-SU Prototyping flow for CQ84 is not implemented.
493642-1231776798	Timing	SXA/SNet delay no change between FF to Latch even place a new location
493642-1296864192	Timing	Re-opening a saved ADB does not keep the min delay analysis.
493642-1355056818	Timing	Tcl command `st_expand_path` does not generate complete report in CSV format.
493642-1412481392	Timing	RH1280 design has large delay on bidirectional bus.
493642-1458982040	Timing	Best case analysis considers nonzero Krad (radiation).
493642-1474493016	CAE	AX Vital lib has wrong if statement.
493642-1494513598	Timing	Timing-driven layout crashes in Libero 9.1 SP5.
493642-1495486649	SmartGen	`RTAX_COUNTER`: Compact counter does not function correctly at 26th bit and onward.
493642-1499505826	Layout	Prototyping file generation is crashing.
493642-1503387344	Timing	RTAX4000D: EMD factors still in default values.
493642-1503387344	Timing	RTAX4000S-1 speed grade factor on nets is not correct.
493642-1503683041	Timing	Max/Min delay constraints enhancements.
493642-1523263801	Timing	SmartTime issue with cross clock domain timing analysis.
493642-1529815451	Timing	Incorrect clock constraint on inter-clock domain analysis.
493642-1539844086	Timing	Timing difference between SmartTime GUI and timing report.
493642-1552954572	VHDL Library	APA Dynamic PLL simulation model issue.
493642-25401413	Synopsys	Netlist Implementation of 40MX and 42MX.
493642-553205603	SmartTime	Constraints coverage report fails to recognize constraints.

.....continued

Case Number	Product	Summary
493642-622346682	SmartTime	Enhance data sheet reporting functionality.
493642-624269471	Synopsys	Using `syn_maxfan` and `syn_noclockbuf`, but signals are still buffered.
493642-744434833	Compile	Optimized netlist is dropping INV from the original netlist.
493642-752234875, 493642-1510861284	Compile	Port missing after publishing the Designer block.
493642-87097473	SmartTime	Constraint Coverage Report.
93642-945599141	SynplifyPro	Post-synthesis simulation failed with Synplify Pro ME 2010.09A-1 and speed_grade=STD.

3. Known Limitations, Issues, and Workarounds (Ask a Question)

3.1 AX-Generated Clocks Issue with SP3 (Ask a Question)

Users may see an issue (crash) with Timing-driven Place and Route or Timing analysis when an AX design has a PLL and the timing constraints file has a generated clock constraint (that is, `create_generated_clock` constraint) on the PLL output clocks. To get around this issue, users can use create clock constraint (that is, `create_clock`) on the PLL output.

3.2 Repeated Clock-to-Out Entries in SmartTime (RTAXS) (Ask a Question)

SmartTime clock-to-output incorrectly displays multiple repeated entries (i.e., fills to the "number of paths" limit with repeats). As a result, no other signals can be accessed from the summary level.

Workaround: The repetition is due to the generated clock on the output port. It is possible to see other paths in the same set by temporarily removing the generated clock or by explicitly looking for paths to a specific output.

3.3 Synplify Pro will Not Run in Batch Mode with a Node-Locked License (Ask a Question)

If you want to run Synplify Pro ME in batch mode you need a floating license. Floating licenses for Libero Gold are free. If you are purchasing Libero Platinum, request a floating license product. If have a Libero Platinum node- locked license and want to exchange it for floating, please contact customer support.

3.4 Unresponsive Buttons on Linux (Ask a Question)

Buttons (**Close**, **Browse**, **OK**, **Cancel**, **Next**, **Back**, etc.) in the configurators and dialog boxes may be unresponsive to mouse clicks when the window is first opened.

Workaround: Move the entire dialog box slightly. The buttons will then respond.

Also, some of the buttons (such as **Execute Script** dialog buttons) must be double-clicked, which is not typical button behavior.

3.5 Drag and Drop of Catalog Components to SmartDesign Canvas May Stop Working when Using VNC on Linux (Ask a Question)

Use one of the following workarounds to solve the issue:

- Right-click the selected core in the Catalog and choose **Instantiate in SmartDesign**.
- Exit Libero. Create a new VNC session and log back in to the machine. Start Libero. The drag-and-drop feature will be enabled.

3.6 JTAG Reset Option Description in the Online Help is Incorrect (Ask a Question)

RTAX-S enables you to program an internal pull-up resistor for the JTAG TRST pin. This option is available in the Programming dialog box. The help topic for this dialog box is INCORRECT. It says:

Use the JTAG reset pull-up resistor - Forces the JTAG circuitry to constantly be in RESET. Microsemi recommends that you use this option. The correct statement is:

Use the JTAG reset pull-up resistor – Programs the pull-up and forces TRST to HIGH so that it will not reset the Tap controller.

3.7 FlashPro Issues Previously Reported in Libero IDE v9.0 SP3 Release Notes (Ask a Question)

Table 3-1. FlashPro Issues Previously Reported in Libero IDE v9.0 SP3 Release Notes

Issue	Description
23423- Error when using Inspect Device if JTAG chain is constructed by performing Auto-Chain Construction.	If the JTAG chain is constructed automatically by selecting **Construct Chain Automatically** in the **Configuration** menu, and you click the **Inspect Device** button, you will see the following error: Error: Cannot initialize debug engine: Cannot initialize the programmer: No available Actel products found on USB port. **Workaround:** Option 1: Construct the device chain by manually specifying the list of devices in the chain using the **Add Actel Device** or **Add non-Actel Device** options, and save the FlashPro project. Option 2: Manually resolve the device by selecting the Actel device that is in the chain, and save the FlashPro Project. Option 3: Load the programming file for the devices in the chain; execute `read_idcode` action in the programming files, and save the FlashPro Project.
6871- Cannot load the same PDB for multiple devices or copy and paste.	**Workaround**: Use STAPL files. Generate STAPL files from Libero IDE or FlashPro.
6859- When using FlashPro programmer with Windows Vista operating system, the Refresh/Rescan may remove the programmer from the programmer list.	**Workaround**: Restart the FlashPro software. This action will refresh the list of programmers.

4. Additional Third-Party Tools and Documentation (Ask a Question)

The following versions of third-party tools are included with Libero IDE v9.2 SP4. Future releases of Synopsys ME tools will be released stand-alone as they become available.

- Synplify AE P-2019.03A-SP1
- Identify AE P-2019.03A-SP1
- Synphony Model Compiler ME I-2013.09M-1
- ModelSim10.2c ME
  Note: If you are using Libero IDE v9.2 SP3 on the Windows 10 platform, you must install ModelSim ME v10.5c standalone software to simulate your design.

Important: To run Synphony Model Compiler ME, you must have MATLAB/Simulink by MathWorks installed with a current license. You cannot run Synphony Model Compiler ME without MATLAB/Simulink. MATLAB/Simulink licenses must be obtained from MathWorks.

Additional References

For more information, refer to the following documentation.

- ModelSim® ME
- Synopsys Synplify Pro ME Release Notes
- Identify ME
- Synphony Model Compiler ME

5. Revision History (Ask a Question)

Revision	Date	Description
B	09/2023	Updated the 2. Download Libero IDE v9.2 SP4 section.
A	04/2021	Initial Revision

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