RN0222
Release Notes
CoreRxIODBitAlign v2.2

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Updated for CoreRxIODBitAlign v2.2.

1.2 Revision 2.0

Updated the release notes with additional information for the sections: Functional Description and Timing Diagrams. Updated for CoreRxIODBitAlign v2.1.

1.3 Revision 1.0

This was the first publication of the document. Created for CoreRxIODBitAlign_v2.0.

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2 CoreRxIODBitAlign

2.1 Overview

This release notes accompany the production release of CoreRxIODBitAlign v2.2. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

CoreRxIODBitAlign supports the following features:

- Supports Bit Alignment with different eye widths 1-7
- Supports different Fabric DDR modes 2/4/3p5/5
- Supports Restart / Hold mechanism
- Supports MIPI training through LP signaling start of frame
- Supports 256 Tap delays for bit alignment

2.3 Delivery Types

No license required. Un-obfuscated Verilog RTL source files provided.

2.4 Supported Families

- PolarFire® SoC
- PolarFire®

2.5 Supported Tool Flows

CoreRxIODBitAlign v2.2 requires Libero® System-on-Chip (SoC) v12.0 or higher.

2.6 Installation Instructions

The CoreRxIODBitAlign CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the Add Core catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based* article. To know how to create SmartDesign project using the IP cores, refer to the *SmartDesign User guide*.

2.7 Documentation

This release contains a copy of the *CoreRxIODBitAlign Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also suggests implementation changes. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

Verilog user testbench.

2.9 Resolved Issues in the v2.2 Release

Table 1 lists the Software Action Requests (SARs) that were resolved in the CoreRxIODBitAlign v2.2 release.

Table 1 • **Resolved Issues in the v2.2 Release**

SAR Number	Changes
115013	Added Left and Right EYE Tap delays information in the top module.

2.10 Discontinued Features and Devices

There are no discontinued features and devices in CoreRxIODBitAlign v2.2.

2.11 Known Limitations and Workarounds

There are no known limitations and workarounds in CoreRxIODBitAlign v2.2.