RN0241
Release Notes
CoreQSPI v2.0

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at www.microsemi.com.

51300241. 1.0 11/20

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

This is the first publication of this document. Created for CoreQSPI v2.0

Contents

Tables

2 CoreQSPI

This release notes accompany the production release of the CoreQSPI IP core version 2.0. This document provides details about the features and enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.1 Features

CoreQSPI supports the following features:

- Master SPI Data Rate
  - Programmable SPI clock HCLK/2, HCLK/4, or HCLK/6
  - Maximum data rate is HCLK/2
- FIFOs
  - Transmit and Receive FIFO
  - 16 byte transmit FIFO depth
  - 32 byte receive FIFO depth
- SPI Protocol
  - Master operation
  - Motorola SPI supported
  - Slave select operation in idle cycles configurable
  - Supports Extended SPI operation (1, 2, and 4-bit)
  - Supports QSPI operation (4-bit operation)
  - Supports BSPI operation (2-bit operation)
  - Support XIP (execute in place)
  - Supports three or four-byte SPI address.
- Frame Size
  - Supports 8- bit frames directly
  - Back to back frame operation supports >8-bit frames
  - Supports up to 4 GB Transfer (2**32 bytes)
- Direct Mode
  - Allows a CPU to directly control SPI interface pins.

2.2 Delivery Types

CoreQSPI is available with Obfuscated version (license locked) at the time of packaging.

2.2.1 Obfuscated

The core can be instantiated with SmartDesign for Simulation, Synthesis, and Layout can be performed with Libero® System-on-Chip (SoC) or Integrated Design Environment (IDE).

2.3 Supported Families

CoreQSPI supports the following families:

- PolarFire® SoC
- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

2.4 Supported Tool Flows

CoreQSPI requires Libero® System-on-Chip (SoC) v11.9 or higher.

2.5 Installation Instructions

The CoreQSPI CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.6 Documentation

This release contains a copy of the *CoreQSPI Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to *Libero SoC documents page* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.7 Supported Test Environments

Verilog user testbench.

2.8 Resolved History

Table 1 describes the release history for CoreQSPI.

Table 1 • **Release History**

Version	Date	Changes
2.0	November 2020	Initial release.

2.9 Known Limitations and Workarounds

There are no known limitations and workarounds in CoreQSPI v2.0.