Welcome to Edition 28 of Microchip's Space Brief newsletter. Written for design engineers and design managers, system engineers and system architects, component engineers, radiation effects scientists and program managers in the space industry, Space Brief is a quarterly newsletter in which we aim to bring you the latest news about Microchip's radiation-tolerant and radiation-hardened products. Space Brief provides information about new products, updates on qualification and radiation testing, links to formal customer notifications, and news about workshops and conferences at which Microchip will be presenting or exhibiting.

Please forward Space Brief to your colleagues, and let them know they can register to receive this newsletter directly to their email inbox every three months by clicking here.

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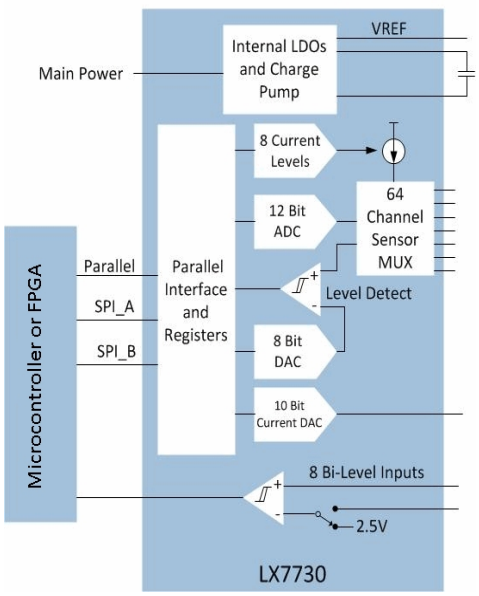
PRODUCT NEWS
New Datasheet Now Available for LX7730 Telemetry Controller

To simplify your design needs, we have made a major update to the datasheet for our LX7730 rad-hard by design telemetry controller. You'll see a new format with this version that now includes all application notes within the document. These cover subjects such as grounding architecture, power savings, and AMUX application items. We have also added useful tables that contain calculated values for external components.

The new LX7730 datasheet can be found here.

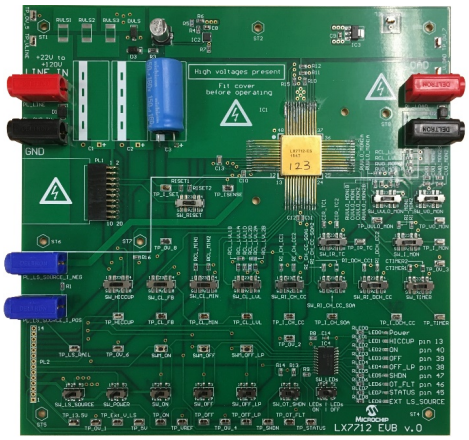


Key features of the LX7730 include:

- 64-channel analog input multiplexer
- 13 ksps 12-bit ADC and 10-bit DAC
- 3% precision adjustable current source
- 8 bi-level analog inputs and logic outputs
- Parallel interface or dual SPI interfaces
- Replaces 19–24 discrete ICs
- 132-pin CQFP and 208 plastic QFP
- Radiation tolerance: TID 100 krad, ELDRS 50 krad, SEL immune to 87 MeV.cm^2/mg
- QML SMD 5962-1721901 (Q and V flows)

LX7712 Programmable Current-Limiting Power Switch Evaluation Boards Now Available

As mentioned in the last newsletter, we are now sampling the LX7712 rad-hard by design programmable current limiting power switch. In addition to IC samples, we presently offer an evaluation board to assist you with your evaluation.



The LX7712 is designed for spacecraft applications and can be configured as a latch-able current limiter or a fold-back current limiter. It provides a means to turn on or off a DC load with current up to 5A and includes a solid-state P channel MOSFET switch and catch diode. The integration allows the temperature of the switch to trigger an optional thermal shutdown. The LX7712 can be programmed with just a few external components, and multiple devices can be paralleled in a master/slave arrangement to increase the current rating. It is packaged is a 48-pin hermetic HTF package.

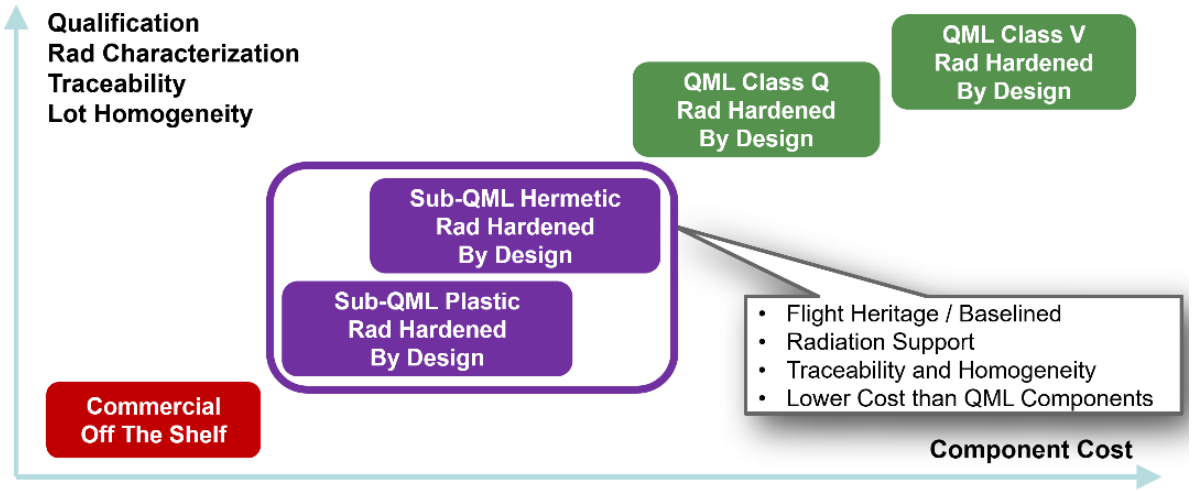
The LX7712 datasheet and radiation test results can be found here.

Please contact Dorian.Johnson@microchip.com for more information.

Sub-QML FPGA Information is Now Live

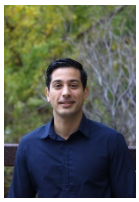
Please visit our new Sub-QML web page, where you will find important documentation for Sub-QML FPGAs. In the documents tab we have uploaded the RTG4™ FPGA Plastic product brief and RTG4 FPGA Plastic package mechanical drawings. We have also uploaded Sub-QML screening flows that apply to all our RT FPGAs. Stay tuned for the RTG4 FPGA Plastic data sheet and pin assignment document.

Our Sub-QML FPGAs bridge the gap between QML and Commercial Off-the-Shelf (COTS) components. Until now, the two main component options have been COTS products, which usually come with no radiation and limited reliability data, or QML-Q/V components, which are radiation-hardened but more expensive and have longer lead times. Our Sub-QML FPGAs are ideal components for New Space applications where commercial satellite constellations require lower unit cost and faster service entry.



Please reach out to your local Microchip sales team if you require Sub-QML FPGAs or radiation-tolerant FPGAs in higher volume and at a lower cost than traditional space applications, or contact Microchip's space marketing team:

Ken O'Neill,
Director of Marketing,
Space and Aviation:
Ken.ONeill@microchip.com



Julian Di Matteo,
Senior Engineer,
Product Marketing,
Space and Aviation:
Julian.DiMatteo@microchip.com

Documentation Update: RT ProASIC3, RTAX Datasheets, and RT FPGA Brochure

Since our last edition of Space Brief, we worked on several documentation updates that are now live on our website. The RT ProASIC3 data sheet has been updated to revision 6. We have updated the 'Radiation Performance' section on the first page of the data sheet to reflect the latest guidance on TID performance. A customer notification CN20007 was issued to inform our customers of this important change.

We have updated the RTAX-S/SL and RTAX-DSP Radiation-Tolerant FPGA data sheet to revision 18. In this revision, we have made several modifications that are listed in the revision history of the datasheet.

Microchip's RT FPGA Brochure has been updated to reflect the latest information on our products.

For questions please contact:

Julian Di Matteo,
Senior Engineer,
Product Marketing,
Space and Aviation:
Julian.DiMatteo@microchip.com

Integrating MathWorks FIL Workflow with Microchip RTG4 FPGA Development Kit

The integrated Field Programmable Gate Array (FPGA)-in-the-loop (FIL) workflow with MathWorks' HDL Coder and HDL Verifier enables you to automatically generate test benches for hardware description language (HDL) verification, including VHSIC Hardware Description Language (VHDL) and Verilog, providing rapid prototyping and verification of designs.

The workflow is now available in MATLAB®'s R2020A release with Microchip Libero® SoC Design Suite v12.0 and subsequent releases. This now enables you to integrate MathWorks' MATLAB, a multi-paradigm numerical computing environment, and MathWorks' Simulink®, a graphical programming environment, with Microchip's RTG4 FPGA Development Kit for FIL verification.

To execute this workflow, you will require the following software tools:

- **Microchip Libero SoC (v12.0 or subsequent release)**
  - Libero SoC Design Suite v12.x
- **Hardware Support Package for RTG4 FPGAs**
  - Hardware support package from MathWorks **OR**
  - From within MATLAB Add On > "Get Hardware Support Package" option
- **MathWorks Tools**
  - MATLAB
  - Simulink
  - HDL Coder
  - HDL Verifier
  - Fixed-Point Designer

Along with these software tools, you will require the following hardware:

- Microchip's RTG4 FPGA Development Kit
- Ethernet cable
- USB JTAG cable for programming the RTG4 FPGA kit

The hardware support package automatically integrates our PolarFire® FPGA and SmartFusion® 2 System-on-Chip (SoC) FPGA development board along with the RTG4 FPGA Development Kit.

Once the tools are installed, you need to set up the Libero SoC Design Suite tool path in MATLAB by invoking the “hdlsetuptoolpath” command from MATLAB prompt and set the path to the Libero software installer.

This enables the call to the Libero software once the “FPGA-In-Loop Option” is selected from “HDL Workflow Advisor” from the system block diagram within Simulink design for integrating the RTG4 FPGA development kit in the Libero software, as shown in Figure 1.

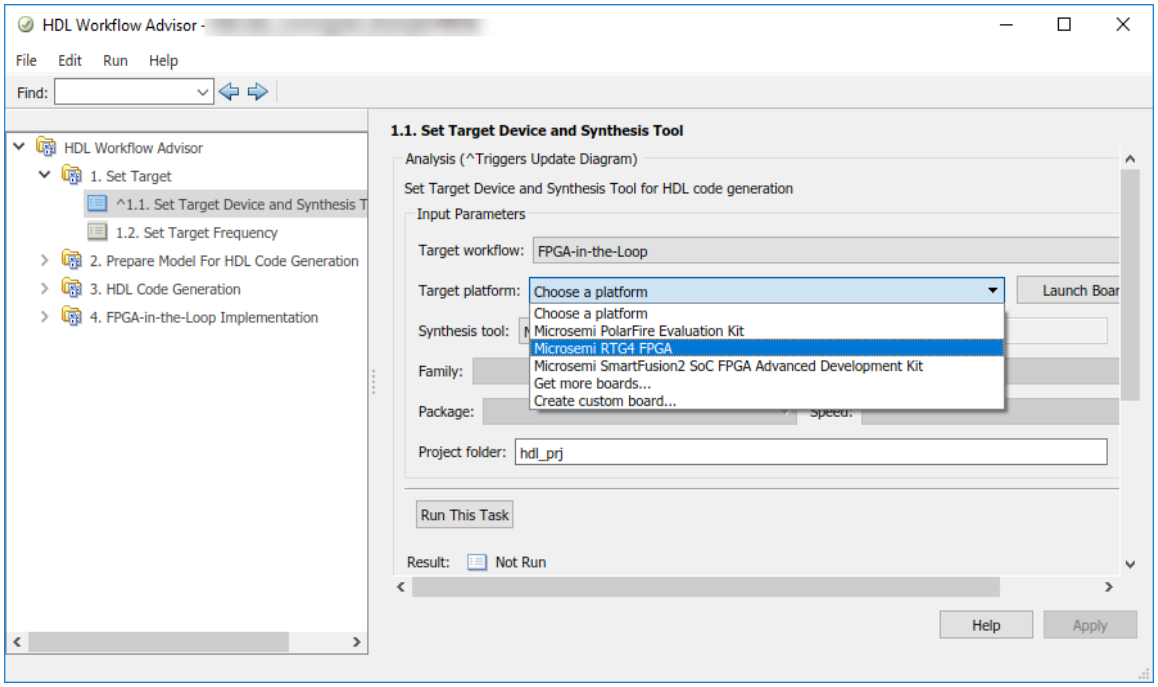


Figure 1

MathWorks ”HDL Workflow Advisor” is a guided tool which helps you generate the HDL Code with “HDL Coder” and deploy the bit stream directly on the RTG4 FPGA development kit, and connect these boards directly with MATLAB and Simulink System Level Testbenches using “HDL Verifier”. This FIL simulation helps you validate mission-critical systems for space and other applications directly on the RTG4 FPGA in one unified environment.

Microchip’s integrated FIL workflow with MathWorks enables a unified workflow to verify designs comprehensively. It integrates Libero SoC Design Suite—a comprehensive, easy-to-learn, easy-to-adopt development toolset for designing with Microchip's FPGAs—with MATLAB and Simulink for design verification and provides FIL verification with Microchip FPGA boards. This allows you to catch bugs early in the design cycle, helping reduce time to market and enabling early verification.

You can also watch the webinar “Targeting Algorithms to Microsemi FPGAs using MATLAB and Simulink” to see how MATLAB and Simulink are used to model, simulate and verify algorithms targeted to Microchip FPGA boards.

For further information, please contact Puneet.Kumar@microchip.com

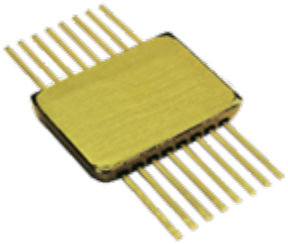
Vectron’s DOC203679, Rev F, and OS-68338, Rev P Offer Miniaturized Space Qualified Clocks to the Industry

Since 2000, our general specifications for high-reliability, radiation-tolerant, space-qualified clocks have been used in place of customer-generated SCDs and have quickly become the industry standard for many of today's leading satellite OEMs. DOC203679, Revision F (LVDS) features a 50% footprint reduction for single complementary output platforms through the use of a 10 x 13 mm flatpack enclosure and also includes a lead forming option. OS-68338, Rev P (ACMOD) features the addition of three 7x9 mm platforms to bridge the gap between our legacy 5 x 7 mm and 9 x 14 mm offerings. Both revisions were released in February 2020 and include ordering codes that reflect full compliance with MIL-PRF-55310, Rev F Screening, and Group C Inspection for Product Level S devices. Vectron (now Microchip) Hi-Rel Standards can be found at https://www.vectron.com/products/space/space.htm and will certainly minimize design time and program costs.

DOC203679, Revision F (LVDS)

New Features:

- Addition of 10 ×13 mm platforms that offer a 50% footprint reduction over the legacy enclosure:
  - Model 1203 (straight leads)
  - Model 1219 (lead-formed)
- Single complementary output pairs available to 200 MHz
- Utilizes ruggedized 4-point crystal mount
- Tolerant to 100 krad(Si) TID; buffer rated to 135 MeV.cm^2/mg (SEL) and 67 MeV.cm^2/mg (SET/SEU)
- Optional pre-crystal mount AND post-crystal mount pre-cap inspections
- Optional 20 MP high-resolution digital pre-cap photos



Download

DOC203679, Rev F

Hi-Rel Radiation-Tolerant LVDS Clock Specification

Same Benefits:

- No OEM SCD required
- No additional qualification required
- Quicker delivery
- Lower overall cost
- Multiple screening options
- Multiple enclosure options

OS-68338, Revision P (ACMOS)

New Features:

- Addition of leaded 7 × 9 mm platforms to bridge the gap between our 5 × 7 mm and 9 × 14 mm offerings:
  - Model 1179 (straight leads)
  - Model 1189 (gull-wing leads in)
  - Model 1199 (gull-wing leads out)
- Nominal frequencies up to 70 MHz
- Utilizes ruggedized 4-point crystal mount
- Tolerant to 100 krad (Si) TID; microcircuit tested to 120 MeV.cm^2/mg (SEL) and 40 MeV.cm^2/mg (SET)
- Optional pre-crystal mount AND post-crystal mount pre-cap inspections
- Optional 20 MP high-resolution digital pre-cap photos

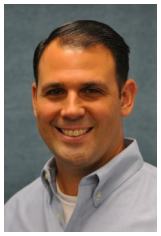
Download

OS-68338, Rev P

Hi-Rel Radiation Tolerant ACMOS Clock Specification

Same Benefits:

- No OEM SCD required
- No additional qualification required
- Quicker delivery
- Lower overall cost
- Multiple screening options
- Multiple enclosure options



For more information, contact Scott.Murphy@microchip.com

Microchip Announces DLA SMD Numbers for ATMX150RHA ASIC Technology

ATMX150RHA ASICs are now available in several quality assurance grades, including Mil-Prf 38535 QML-Q and QML-V, and ESCC 9000 under respective numbers ESCC DS : 9202/083 and SMD : 5962-20B01.

ATMX150RHA is a mixed-signal ASIC technology providing high-performance and high-density solutions for space applications with a set of qualified analog IPs, such as DACs, ADCs, PLL and regulators. ATMX150RHA simplifies the design of mixed-signal ASICs.

ATMX150RHA ASICs also cover the digital domain, extending up to 22 million gates.

The availability of a 5V to 1.8V regulator and the 5V tolerant I/O permits easy retargeting of obsolete or end-of-life ASICs with 5V core supply.

In addition, the availability of the Physical Design Kit (PDK) gives you the ability to develop your own analog blocks and use Microchip SMPW foundry services.

This technology provides also high-voltage capabilities (LDMOS transistors up to 25V characterized) that can be interesting in some power management applications.

The ATMX150RHA ASIC technology is manufactured on a 150 nm, five-metal-layers + thick metal layer SOI CMOS process intended for use with a supply voltage of 1.8V for core and 2.5/3.3/5V for the periphery. This ASIC platform is supported by a combination of state-of-the-art third-party and proprietary design tools from Synopsys, Mentor and Cadence. The tools from these suppliers collectively form the reference tool flows for both the front and back end.

The technology parameters and some extra features include:

- Comprehensive library of standard logic and I/O cells
- Up to 22M usable gates (NAND2-equivalent)
- Operating voltage 1.8 ± 0.15V for the core and 5V ± 0.5V, 3.3 ± 0.3V, 2.5 ± 0.2V for the periphery
- High-speed LVDS buffers 655 Mbps according to the TIA/EIA-644-A standard
- PCI buffers
- No single-event latch-up below a LET threshold of 78 MeV.cm^2/mg at 125°C
- SEU hardened flip-flops
- TID test up to 150 krads (Si) for 1.8V and 3.3V devices and 90 krads (Si) for 5V according to Mil-Std 883 TM1019
- CCGA, CLGA and CQFP qualified packages
- Analog IPs with dedicated qualification packages available: voltage regulator, voltage reference and monitoring, clock synthesizer, signal conditioning

Microchip is proud to continue supplying the space Industry with high-quality solutions and a higher level of services through the release of the SMD number of the ATMX150RHA ASIC technology for the digital domain. We are now planning to extend the qualified domain by adding our analog IPs within the ESCC data sheet.

For more information, contact Pascale Charpentier, Product Marketing, ADG Group.
Pascale.Charpentier@microchip.com

RT PolarFire® FPGAs Support in Libero SoC Design Suite v12.4 Release

Microchip has released version 12.4 of the Libero SoC Design Suite, which includes support for RT PolarFire radiation-tolerant FPGAs. Advance timing for standard speed grade RTPF500T FPGAs over the military temperature range is included. SynplifyPro can infer Soft triple module redundancy (TMR) for inferred FFs. You can use TMR to mitigate SEUs in any part of the design. Place-and-route separates the TMR flip-flops physically to mitigate clock transients and upsets. Libero SoC Design Suite v12.4 supports pin assignment for the new CG1509 ceramic column grid array package. However, programming and BSDL export of this device are not yet enabled.

Libero SoC Design Suite v12.4 can be downloaded here. More information about the Libero SoC Design Suite can be obtained here.

For the latest information on RT PolarFire FPGAs including radiation test data, contact Ken.O'Neill@microchip.com.

High-Performance, Multi-Axis Motor Control for Space and Aviation Applications

Microchip's FPGA-based multi-axis, deterministic, high-precision and low-power motor control solution features an IP suite, flexible design options and extensive resources. The solution has been optimized for RTG4 FPGAs and SmartFusion 2 SoC FPGAs and caters to industrial, medical, space and aviation segments. We also offer a space-grade motor driver (LX7720 Rad Tolerant Spacecraft Motor Controller) to enable holistic solution development. The solution builds on the underlying advantages of our radiation-tolerant and configuration-SEU-immune FPGAs to be an ideal choice for space and aviation applications requiring long operating life, high reliability and security under high-vacuum, radiation and wide-operating-temperature environments.

Watch our latest video on **High-Performance, Multi-axis Motor Control for Space and Aviation Applications** to learn more.

For more information, visit Microchip's FPGA-Based Multi-Axis Motor Control Solution page or contact Apurva.Peri@microchip.com.

Radiation-Tolerant Microcontrollers - System Error Management In-Flight System Recovery With SAM-BA Interface

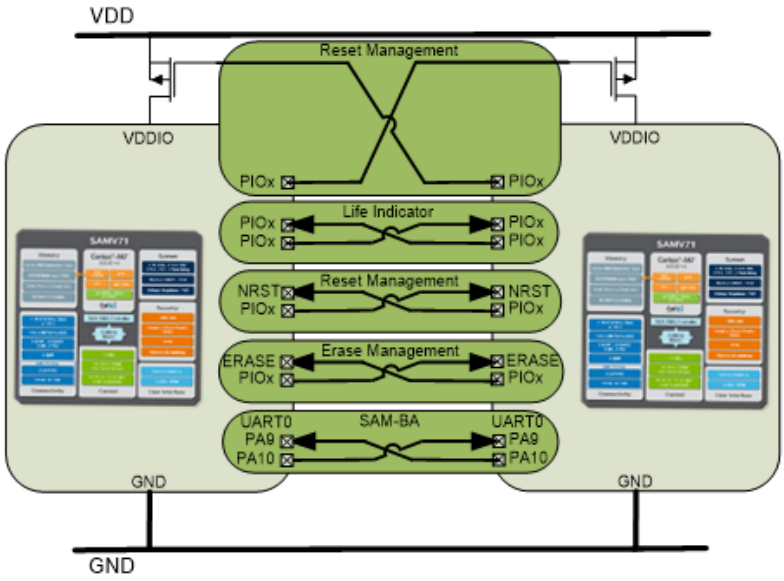
In space flight applications, critical events caused by radiation effects may require that a system be partially or fully reconfigured to recover. The SAMV71SAMV71Q21RT is a high-performance, radiation-tolerant Flash microcontroller (MCU) based on the 32-bit Arm® Cortex®-M7 RISC processor with floating point unit (FPU). This device operates at a maximum speed of 300 MHz, offers 2048 Kbytes of Flash, 16 Kbytes of dual cache memory and 384 Kbytes of SRAM and is available in 144-pin packages. The SAM3X8ERT is a high-performance, radiation-tolerant Flash MCU based on the 32-bit Arm Cortex-M3 RISC processor with floating point unit (FPU). This device operates at a maximum speed of 100 MHz, offers 2048 Kbytes of Flash, 16 Kbytes of dual cache memory and 384 Kbytes of SRAM and is available in 144-pin packages.

These two radiation-tolerant MCUs offer high radiation performance, featuring Single Event Latch-up (SEL) immunity up to 60 MeV.cm^2/mg and with a TID capability up to 30 Krad. With regards to the SEU figures, characterization of the different blocks has been completed to assess the performance. While the SAMV71Q21RT and the SAM3X8ERT are not immune to single event functional interrupts, their embedded features enable them to recover from two types of events that require system-level mitigation:

- Flash content integrity corruption
- Single event functional interrupts

As illustrated below, basic system management to mitigate these errors can be implemented using several I/Os and a UART interface. At the system level, the infrastructure to enable recovery should consist of a basic master/slave interface that can support:

- A shared simple life indicator
- Reset management - NRST (reset signal)
- Flash erase management - ERASE (Flash erase signal)
- SAM-BA interface – UART0 port
- Power management – I/O to control the power rail



System Error Recovery Demonstration

We have created a simple MPLAB® X Integrated Development Environment (IDE) project to demonstrate how to use the SAM-BA interface to reprogram the Flash memory of a SAMV71Q21RT MCU. The application note and its software are y available from:

https://www.microchip.com/wwwappnotes/appnotes.aspx?appnote=en1001788
and
http://ww1.microchip.com/downloads/en/Appnotes/AM_V71RT02_firmware.zip

Product Information

- The SAMV71Q21RT family is offered in a hermetic ceramic CQFP144 and plastic LQFP144 packages. The data sheet and safety application note can be found at: https://www.microchip.com/wwwproducts/en/SAMV71Q21RT
- The SAM3X8ERT family is offered in a hermetic ceramic CQFP144 and plastic LQFP144 packages. The data sheet and safety application note can be found at: https://www.microchip.com/wwwproducts/en/SAM3X8ERT

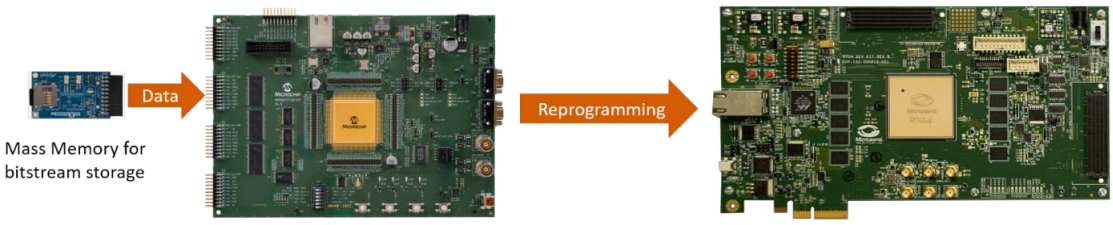
Please contact Yohann.Bricard@microchip.com for more information.

In-Flight Reconfiguration of RT FPGAs with RH Microcontroller

Providing the ability to reconfigure or reprogram a space flight application after integration is becoming a key requirement. It enables essential bug fixes in a system during the final stages of development and after launch of a mission. It also gives you the ability to reprogram or fine tune processing algorithms after mission deployment or to repurposing functional flight hardware after a mission is completed.

With the RTG4 and RT PolarFire FPGA families, Microchip offers an unrivaled space-rated FPGA portfolio that can be reprogrammed during flight. Reprogramming of these FPGAs is done via a simple interface that can be managed by a processor or microcontroller, like the SAMRH71F20 space-rated microcontroller that operates at up to 200 DMIPS. This combination of solutions makes it simple to implement a reconfigurable architecture in your space application. The FPGA and the microcontroller can be interconnected with only a few I/Os to manage the complete reprogramming process and emulate the JTAG interface and the configuration protocol directly in the microcontroller firmware.

The RTG4 and RT PolarFire FPGAs and the SAMRH71F20 now enable in-application reconfiguration for space flight applications. Two demonstrations are available and ready to use, based on standard development kits and of-the-shelf software.



SAMRH71F20 Dev hosts the reconfiguration application, including DirectC library.

RTG4 Dev Kit hosts RTG4 to be reprogrammed by the SAMRH71F20

The main principle of the RT FPGA reconfiguration is that the microcontroller manages the in-flight programming process of the RT FPGA thanks to the DirectC library that emulates both the JTAG interface of the FPGA and the configuration protocol. The microcontroller manages the up-link via the telecommand system to accept a new programming bistream for the FPGA, stores the bitstream in memory, places the FPGA into programming mode, executes the DirectC code to initiate the transfer of programming bistream to FPGA, monitors the FPGA's return to operation and re-initiates programming in case the programming process is interrupted by a radiation upset.

Key features for in-flight reconfiguration include:

- One SAMRH71F20 radiation-hardened microcontroller
- DirectC library that emulates both the JTAG interface of the FPGA and the configuration protocol
- One or more RTG4 or RT PolarFire FPGAs
- A mass memory suitable for bitstream temporary storage

Product Information

- The SAMRH71F20 family is offered in a 256-pin hermetic ceramic quad flatpack and is available now:
- RTG4 FPGAs are offered in a 1657-pin hermetic ceramic column grid array and a 352-pin hermetic ceramic quad flatpack and are available now.
- The RT PolarFire FPGA is currently under development, and will be available in a 1509-pin hermetic ceramic columns grid array.

Development Tools

The In-Flight Reconfiguration for Space Applications demonstration is based upon our standard FPGA and microcontroller development kit available for purchase. It is supported by our standard software and FPGA configuration development platform.

- SAMRH71F20 Evaluation Kit
- Demonstration Expansion Memory Card
- Demonstration Software
- RTG4 FPGA Development Kit
- PolarFire Development Kit (coming soon)

Visit our Github repository to access the software used for these demonstrations and to find details about the interconnect between the FPGA and the microcontroller: https://github.com/MicrochipTech/adg_fpga_reconfiguration

Please contact Yohann.Bricard@microchip.com for more information.

An Engineer's Perspective on Radiation Effects in Semiconductors: Part 2: SEE in BJTs and MOSFETs

This brief article is based on the work that was presented at Microchip's 2019 Space Forum events.

In the last newsletter we discussed Total Ionizing Dose and its impact on BJTs and MOSFETs. In this version we will take a look into Single Event Effects (SEEs) in BJTs, MOSFETs and Schottkies.

Before we look into SEE, we have to discuss Bragg Depth (same as Bragg Distance). This is central to SEE and it's a bit counter intuitive. Lighter ions penetrate further into the DUT; heavier ions have a shorter Bragg distance. A light ion at a constant MeV/ Atomic Mass Unit (AMU) will have fewer collisions and impart much less energy into these collisions than a heavier ion at the same MeV/AMU. This is important for the ion species used in SEE testing due to the geometries and diffusion profiles in the DUT. For example, if the Bragg depth of a heavy ion is 83 MeV/mg/cm^2 at normal incidence, this ion will penetrate about 100 um into the DUT. This may be in the middle of a depletion region in a BJT or the channel of a vertical MOSFETs. Lighter ion species will stop well into the substrate or pass through completely. This impacts the SEE interactions in both discrete devices and ICs.

Energy Level	Ion	Total Energy	Energy at Bragg Peak	Range in Si	Range at Bragg Peak	Range To Bragg Peak	Initial LET (air)
A (MeV)		MeV	MeV	um	um	um	MeV/mg/cm^2
15	^{4}He	60	0.4	1423	2	1421	0.11
15	^{14}N	210	7	428	7	421	1.3
15	^{20}Ne	300	14	316	8	308	2.6
15	^{40}Ar	599	29	229	9	220	8
15	^{63}Cu	944	90	172	16	156	18.7
15	^{84}Kr	1259	152	170	21	149	26.6
15	^{109}Ag	1634	248	156	26	130	40.3
15	^{129}Xe	1934	339	156	31	124	49.3
15	^{141}Pr	2114	441	154	37	117	56
15	^{165}Ho	2474	608	156	44	112	66.7
15	^{181}Ta	2714	702	155	46	109	74.8
15	^{197}Au	2954	902	155	53	102	82.8
25	^{4}He	99	0.4	3449	2	3447	0.07
25	^{14}N	347	7	1009	7	1002	0.9
25	^{22}Ne	545	14	799	8	791	1.8
25	^{40}Ar	991	29	493	9	484	5.5
25	^{84}Kr	2081	152	332	21	311	19.8
25	^{129}Xe	3197	335	286	31	255	38.9
40	^{14}N	560	7	2334	7	2327	0.6
40	^{20}Ne	800	14	1655	8	1647	1.2
40	^{40}Ar	1598	29	1079	9	1070	3.8
40	^{78}Kr	3117	140	622	20	602	14.4
40	Proton	40	0.1	8148	1.2	8147	0.012

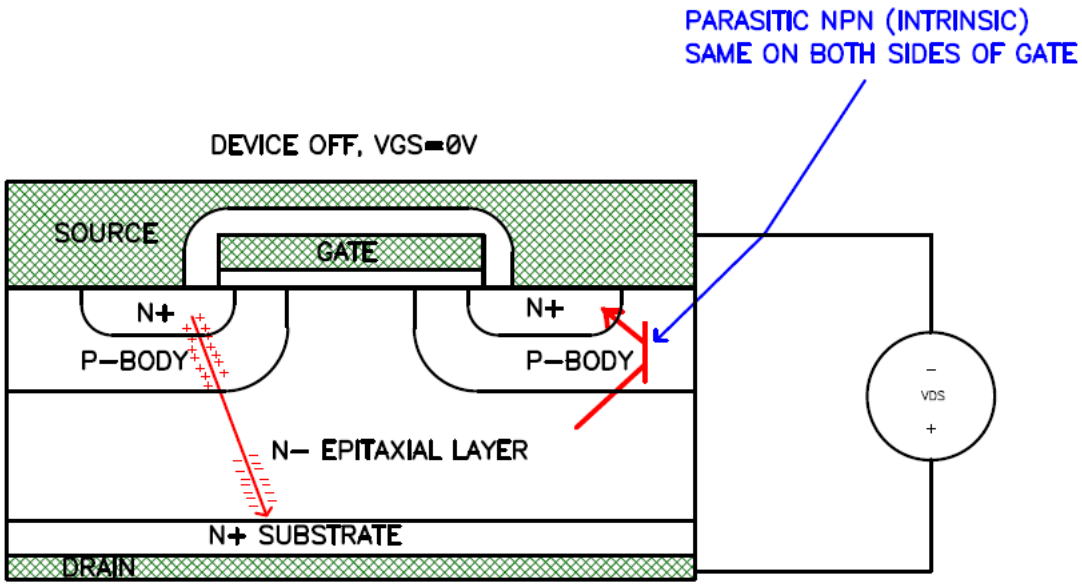
Table 1: Ion Species, Energy Levels and Bragg Distances for SEE Tests

SEE testing is carried out as per JEDEC JESD57A. This test outlines the setup, the flux and the fluence. SEE testing uses heavy ion species, usually at 15 MeV/AMU. Based on this, an He4 ion would then have 60 MeV energy in the beam. But how is this energy transferred to the DUT? The mechanism is known as Linear Energy Transfer (LET), and it varies with the ion species. The heavier the ion, the higher the LET. It is expressed in MeV.cm^2/mg.

SEE is a shorter test in view of TID. The fluence is usually around 1E7 ion/cm^2, the flux is usually around 1E3 to 1E5 ion/cm^2/second.

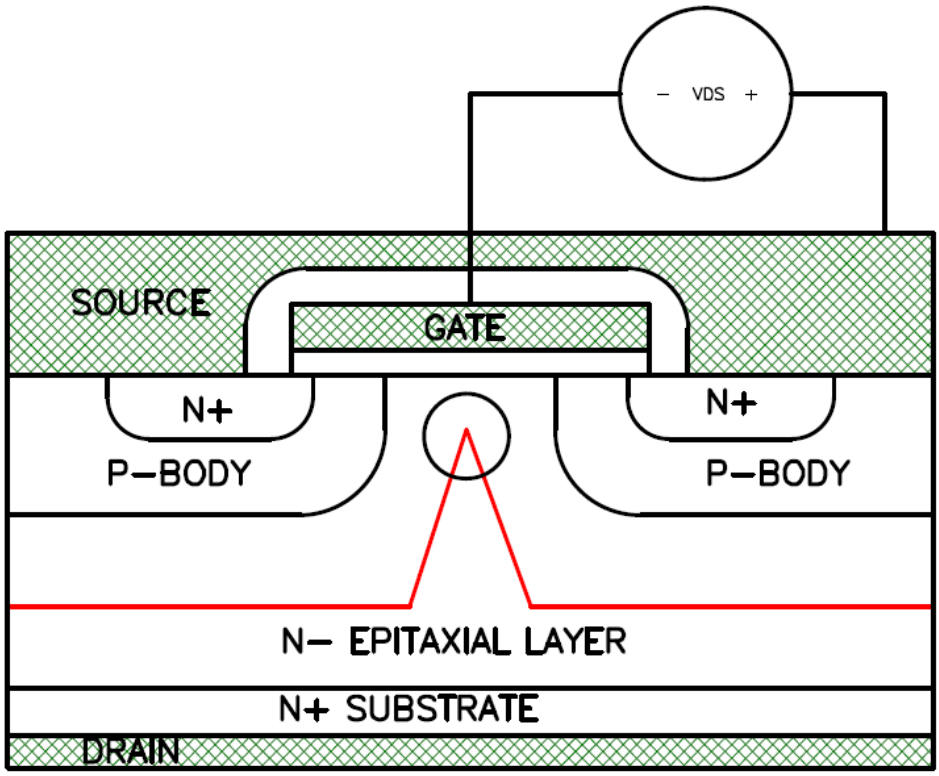
The impact of SEE on BJTs is minimal, however there are documented instances of Single Event Transient (SET). In these instances, it seems that the BE junction was approximately at the Bragg distance for the ion species. While the cause is not exactly known, it is believed that the ion caused a disturbance in the depletion region. The collector, of course, sees this event with gain. There was no damage imparted; rather a “click” noise was viewable on the biased collector, then it returned to normal bias.

The impact of SEE in MOSFETs is more dramatic. There are two main single events that impact the modern vertical MOSFET power switch. Single Event Burnout (SEB) occurs when the intrinsic NPN transistor (in an N-channel enhancement mode MOSFET) is turned on. This is caused by the holes in the electron hole pairs around the incident heavy ion attracting to the base of the intrinsic NPN.



In modern device designs this is difficult due to the source metalization physically shorting this BE junction. SEB is an unrecoverable event. When the intrinsic NPN is turned on, the gate drive command means nothing. Modern radiation-hardened MOSFETs are designed to minimize this effect

Single Event Gate Rupture (SEGR) is the more dominant SEE failure mechanism. This occurs when the MOSFET is biased in the off state. In an N-channel enhancement mode MOSFET, Vds is at maximum blocking voltage (positive on drain, negative on source). Vgs is at maximum negative voltage, usually −5V. The heavy ion then passes through the gate into the channel. It causes a sheath of electron hole pairs to form coaxially around the ion path. The negative bias on the gate (top side) attracts the holes; the positive bias on the drain (back side of die) attracts the electrons. There is then a sharp gradient formed under the gate.



Paul's presentation from the 2019 Space Forum event can be viewed here.

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RTG4 FPGA Product Change Notification (PCN) and Customer Notifications (CN)

The following Product Change Notifications and Customer Notifications have been published on the Microsemi web site. Designers of RTG4 FPGAs are encouraged to review the notifications, and follow the required actions stated therein.

CN19009B RTG4 PLL temperature-dependent loss of lock

CN20006 comprises three separate notifications:
CN20006.1 Loss of Programming Configuration for RTG4 FPGAs
CN20006.2 RTG4 New Global Net Clock Jitter
CN20006.3 RTG4 FPGA Datasheet Updates

PCN20005 RTG4 FPGA SET Filter Delay Calibration

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Events

Due to the global Covid-19 pandemic, almost all of the conferences planned through August 2020 have been either canceled or postponed. At this time, it is not clear whether, and to what degree, Microchip will support events through the remainder of 2020. We are all hoping for a rapid end to the pandemic and for an easing of restrictions on travel and congregating as soon as it is safe to do so. Hopefully, we will be able to provide more clarity in the next edition of Space Brief, which is planned to be published in August 2020.