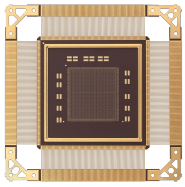
Welcome to Edition 27 of Microchip's Space Brief newsletter. Written for design engineers and design managers, system engineers and system architects, component engineers, radiation effects scientists and program managers in the space industry, Space Brief is a quarterly newsletter in which we aim to bring you the latest news about Microchip's radiation-tolerant and radiation-hardened products. Space Brief provides information about new products, updates on qualification and radiation testing, links to formal customer notifications and news about workshops and conferences at which Microchip will be presenting or exhibiting.

Please forward Space Brief to your colleagues, and let them know they can register to receive their own copy direct to their email inbox every three months by clicking here.

PRODUCT NEWS
RTG4™ FPGAs in CQ352 Achieved QML Class Q Qualification



The radiation-tolerant RTG4 FPGA family in the 352-pin Ceramic Quad Flat Pack (CQFP) package has achieved Qualified Manufacturers List (QML) Class Q qualification by the Defense Logistics Agency (DLA). This qualification validates the quality and reliability of RTG4 FPGAs in the CQ352 package, which provides a more cost-effective integration than higher pin count packages. CQFP is the industry-standard package for space applications with its well-established board integration and inspection procedures.

To achieve QML Class Q qualification for RTG4 CQ352, we leveraged the QML Class V qualification for RTG4 FPGAs in the 1657-pin Ceramic Column Grid Array (CCGA) package. A package qualification was then performed on RTG4 CQ352, in which RTG4 FPGAs passed a series of environmental tests to determine resistance to the deleterious effects of natural elements and conditions surrounding defense and space operations, as well as mechanical and electrical tests.

RTG4 CQ352 Standard Microcircuit Drawings (SMD) have been posted on the DLA website. Microchip plans to seek QML Class V qualification for RTG4 CQ352. Microchip's EV-flow, which is the equivalent of the QML Class V per MIL-PRF-38535, for RTG4 CQ352 is expected in March 2020. RTG4 FPGAs in the CQ352 package can be ordered now.

For more information, please contact Minh Nguyen, Principal Engineer, Product Marketing, Space and Aviation at Minh.Nguyen@microchip.com

Sub-QML FPGAs Bridge Gap Between QML and COTS Components

The burgeoning New Space private spaceflight industry and the trend toward small satellite constellations brings both new opportunities and challenges for mission developers in their selection of components. Until now, the two main component options have been Commercial Off-the-Shelf (COTS) products, which usually come with little to no radiation or reliability data, or QML Class Q/Class V components which are radiation-hardened but more expensive and have longer lead times.

Microchip's Sub-QML FPGAs combine the radiation tolerance of QML components with our spaceflight heritage that permits lower screening requirements, resulting in lower cost and shorter lead times. Because Sub-QML FPGAs are radiation tolerant, they meet very high standards for reliability and radiation protection. In addition to lower screening requirements, certain Sub-QML FPGA families also offer plastic packages which can further reduce component cost, making them well suited for small satellite applications or constellation deployments.

Sub-QML FPGA options are available for all Microchip radiation-tolerant FPGA families. The following table is an example of all screening flows, including traditional QML flows (V, E, B) and Sub-QML screening flows, available for the RTG4 FPGA family:

Flow	Purpose	Package	Qualification	Screening			
				Burn-In	Temp Test	Life Test	DPA
V	NSS, NASA Class1	Hermetic Ceramic	QML-V	Static Dynamic	-55°C – 125°C	Wafer-Lot	Assy Lot
E	Advanced Traditional Space	Hermetic Ceramic	QML-Q	Static Dynamic	-55°C – 125°C	Generic Group C	Optional
B	Entry Level Traditional Space	Hermetic Ceramic	QML-Q	Dynamic	-55°C – 125°C	Generic Group C	None
R	New Space, Strategic Programs	Hermetic Ceramic	MIL-STD-883 Class B	Dynamic	-55°C – 125°C	None	None
Mil Ceramic	New Space, Strategic Programs	Hermetic Ceramic	MIL-STD-883 Class B	None	-55°C – 125°C	None	None
PROTO	Prototyping	Ceramic (Hermeticity not Guaranteed)	MIL-STD-883 Class B	None	-55°C – 125°C	None	None
Mil Plastic	New Space, Strategic Programs	Plastic Non-Hermetic	JEDEC	None	-55°C – 125°C	None	None

Please reach out to your local Microchip sales team if you have a need for Sub-QML FPGAs or radiation-tolerant FPGAs in higher volume and at lower cost than traditional space applications, or contact Microchip's space marketing team:

Ken O'Neill, Director of Marketing, Space and Aviation:
Ken.ONeill@microchip.com

Julian Di Matteo, Senior Engineer, Product Marketing, Space and Aviation:
Julian.DiMatteo@microchip.com

Minh Nguyen, Principal Engineer, Product Marketing, Space and Aviation:
Minh.Nguyen@microchip.com

Deep Learning Inference with Microchip RTG4 FPGA

Microchip has partnered with ASIC Design Services to release their CoreDeepLearning (CDL) Object Detection Demo on the Microchip RTG4 FPGA. CoreDeepLearning allows our customers to implement deep learning networks efficiently inside Microchip FPGAs.

The CDL Compress software allows deep learning networks to be quantized down to 8 bits, increasing the performance while maintaining accuracy. 8-bit quantization allows the IP to use the dot product mode

available inside the RTG4 FPGA multiplier block, effectively doubling the computational throughput. With the latest release of the CDL Compress software, no quantization loss can be seen on the Tiny Yolo v2 reference demo. Using only 144 DSP blocks, CDL can achieve 10 frames per second (fps) on the RTG4 FPGA running at 125 MHz, delivering an effective 55.65 giga operations per second (GOPs/s) from a theoretical 72 GOPs/s.

CDL Demo with RTG4 Development Kit

To get a copy of the demo please contact Francois Labuschagne, Engineering Manager, ASIC Design Services. francois.labuschagne@asic.co.za

For additional information on CDL see https://youtu.be/hgQF9B8Wivs or visit www.coredeeplearning.ai

Vectron® DOC200103, Revision H

The Industry Standard for Space-Qualified, Radiation-Tolerant, Temperature-Compensated Crystal Oscillators

Since 2008, our general specification for High-Reliability, Radiation-Tolerant Space TCXOs has been used in place of customer-generated SCDs and has quickly become the industry standard for many of today's leading satellite OEMs.

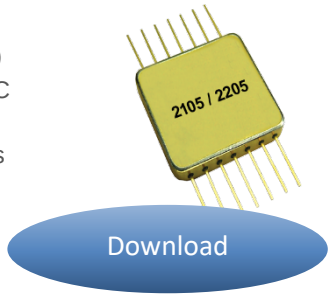
Revision H features the smallest Space TCXO (0.75" × 0.75" × 0.26") available on the market today and includes a lead forming option for all flatpack enclosures. In addition, DOC200103, Rev H also includes a new screening code that reflects full compliance with MIL-PRF-55310 Revision F Screening and Group C requirements for Product Level S devices. Utilizing DOC200103 will certainly reduce your design time and overall project cost.

New Features:

- Miniature enclosure: 0.75" × 0.75" × 0.26"
- New model numbers: 2105/2205 (ACMOS), 2115/2215 (Sine)
- MIL-PRF-55310, Revision F-compliant screening and Group C inspection options
- Standard leadforming now available on all flatpack enclosures
- Recommended pad layouts added for leadforming

Same Benefits:

- No OEM SCD required
- No additional qualification required
- Quicker delivery
- Lower overall cost
- Multiple screening options
- Multiple enclosure options



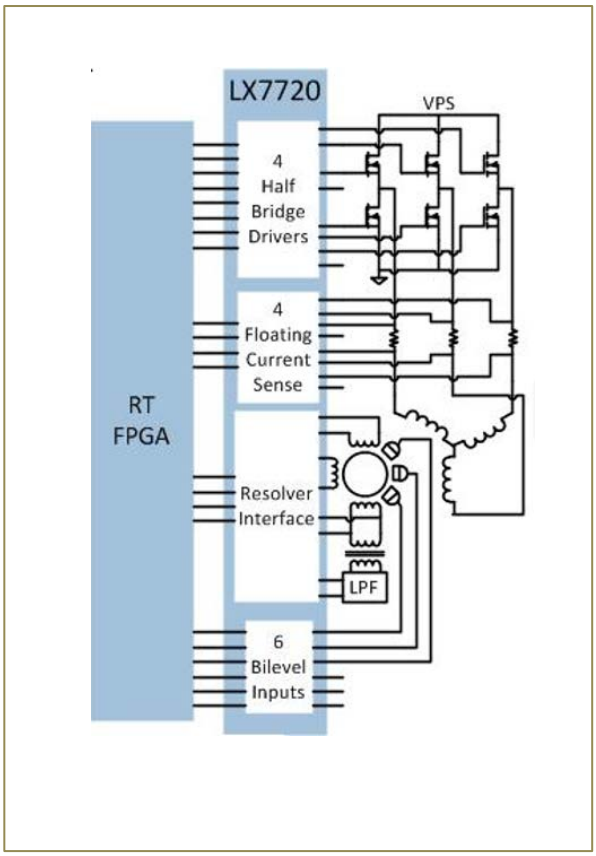
DOC200103, Rev H
HI-Rel Radiation-Tolerant TCXO
Specification

For more information, please contact Scott Murphy, Space and Hi-Rel Product Line Manager at Microchip's Vectron Oscillator Products Division at scott.murphy@microchip.com

NOW IN PRODUCTION:

LX7720 Motor Control/Position Sensing IC

Microchip's LX7720 Motor Control IC for space has successfully completed qualification and meets all requirements of the MIL-PRF-38535 Class Q flow.



As the industry's first highly integrated radiation-hardened-by-design motor control IC, the LX7720 significantly reduces weight and board space relative to conventional discrete implementations.

Key features:

- Four half-bridge N-channel MOSFET drivers
- Four floating differential current sensors
- Pulse modulated resolver transformer driver
- Three differential resolver sense inputs
- Six bi-level logic inputs
- Fault detection
- Radiation-tolerance: 100 krad TID, 50 krad ELDRS and single event immune

Ordering numbers:

- The **LX7720MFQ-EQ** is offered in a 132-pin hermetic ceramic quad flatpack and is available now.
- The **LX7720MFQ-EV**, built to the stringent V-flow requirements of the MIL-PRF-38535 specification, is expected to be in production in July 2020.
- The **LX7720MMF** is packaged in a 208-pin plastic quad flatpack for applications requiring reduced screening. Samples of the LX7720MMF will be available in CQ1 2020.

Development Tools:

The LX7720-DB is an evaluation daughter board also available for purchase. This board interfaces to any of three Microchip development platforms listed here to provide application specific evaluation tools.

- RTG4 Development Kit – The LX7720-DB connects directly to the RTG4 Development Kit's USB interface to communicate to the RTG4 UART
- SAMRH71F20-EK Evaluation Kit – The LX7720-DB connects via a supplied MCU interface
- ProASIC3E Starter Kit– The LX7720-DB connects via a supplied connector board (available March 2020).

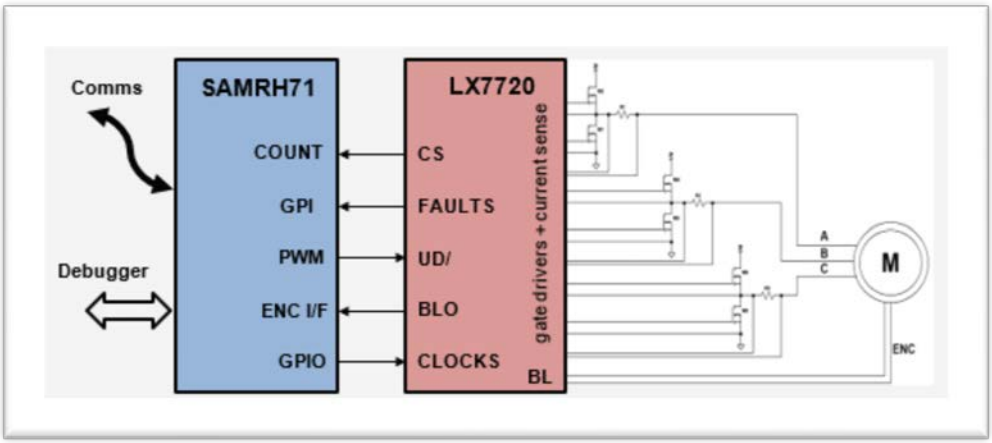
Click Here: To visit the product web page to find the datasheet, conference papers and radiation test reports

For more information, please contact Dorian Johnson, HiRel Product Line Marketing Manager at dorian.johnson@microchip.com

NEW DEMONSTRATION PLATFORM

LX7720 Motor Control IC as Companion Chip to SAMRH71 Microcontroller

A new demonstration platform for space applications was unveiled at our recent Space Forum event. The demonstration shows our LX7720 Motor Control IC working as a companion chip to our new SAMRH71 Arm® Cortex®-M7 based processor to provide closed-loop motor control. In this demonstration, the SAMRH71F20-EK Evaluation Kit connects to the LX7720-DB daughter board, which in turn is connected to a typical motor used in satellite systems.



The two radiation-hardened-by-design ICs interface as shown above:

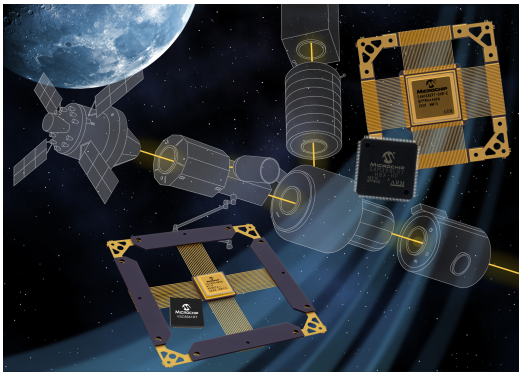
- LX7720 current sense DSM outputs drive SAMRH71 timer/counters
- LX7720 gate drivers' inputs are driven by SAMRH71 PWM
- LX7720 fault outputs drive SAMRH71 GPIOs
- Encoder drives LX7720 BLI inputs and corresponding BLO outputs drive SAMRH71 GPIOs
- SAMRH71 drives the DSM and charge pump clocks of LX7720
- LX7720 drives external MOSFETs and senses output currents
- SAMRH71 senses rotor position using an encoder interface

Both LX7720-DB and SAMRH71F20-EK development tools are available for purchase.

Please contact
dorian.johnson@microchip.com
for more information on the
LX7720-DB.

Please contact
yohann.bricard@microchip.com
for more information on the
SAMRH71F20-EK.

Microchip Enables Ethernet for Space Applications with Two New Rad Tolerant Devices



To support growing demand for Ethernet connectivity for use in space and other high-reliability applications, Microchip announced two new rad-tolerant devices, including the industry's first space-qualified Ethernet transceiver.

Ethernet connectivity technology is increasingly being used in space applications, including many human spaceflight missions such as the Deep Space Gateway, an international spaceport program for human and robotic exploration to the Moon and beyond.

The two new devices are the VSC8540/41RT Ethernet Transceiver in 100 Mbit (40) and 1 Gbit (41) versions; and the SAM3X8ERT Arm Cortex-M3 based microcontroller with embedded Ethernet controller. The new devices extend Microchip's rad-tolerant Ethernet solutions portfolio, which includes Ethernet transceivers, Ethernet-enabled System-on-Chips (SoCs), and IP for implementing Ethernet designs with radiation-tolerant Field-Programmable Gate Arrays (FPGAs).

The SAM3X8ERT rounds out our portfolio of 32-bit MCUs for space, which includes two Arm Cortex-M7 based SoCs; the SAMV71Q21RT radiation-tolerant MCU and the SAMRH71 radiation-hardened MCU. These devices enable Ethernet Time Sensitive Network (TSN) capabilities for more critical applications, making them ideal companion chips to the VSC854xRT transceiver.

As with other Microchip COTS-based radiation-tolerant devices, the VSC8540/41RT and SAM3X8ERT share the same design as the original industrial part. They are fully compatible with the already-available ecosystem of hardware, software, tools and application notes. They also share the same pin distribution in both plastic and ceramic versions to allow a fast design and system development ramp up when using these solutions.

Both devices are single event latch-up immune to at least 62 MeV-cm2/mg (as high as 78 MeV-cm2/mg for VSC854xRT) and a full SEU block-by-block characterization of the device is available with a detailed radiation report. Application notes are also available to help with system mitigation techniques when needed. With regard to total ionizing does (TID), VSC854xRT devices are qualified up to 100 Krad and SAM3X8ERT up to 30 Krad.

These devices are available in ceramic packages with space-grade screening equivalent to QML class Q and QML class V. All devices are proposed with a Hi-Rel Plastic qualification flow to support high-volume programs.

You can read the press release here: "Microchip Announces Industry's First Space-Qualified COTS-Based Radiation-Tolerant Ethernet Transceiver and Embedded Microcontroller"

Click Here for additional information.

For more information, please contact Nicolas Ganry, Product Marketing Manager, Aerospace Marketing at nicolas.ganry@microchip.com

An Engineer's Perspective on Radiation Effects in Semiconductors: TID In BJTs and MOSFETs

This brief article is based on the work that was presented at Microchip's 2019 Space Forum events.

By Paul L. Schimel PE, Senior Staff Engineer, Microchip Aerospace and Defense Group.

We've all seen the need for radiation-hardened semiconductors. We know that the outer Van Allen belt, the inner belt and the earth's atmosphere act as tremendous filters to cosmic particles. What then if we have to put a satellite into Geosynchronous orbit outside of the Van Allen belt? We know that there will be heavy charged particles interacting with our electronics, but how do they interact? How can we design for these interactions?

Historically, the engineers at Microchip have responded to this need for the last 60 years. We were one of the first companies to design and qualify radiation-hardened discrete devices. Our untiring work has made thousands of missions possible, and we continue to innovate in our discrete products and well beyond. Information on Microchip's discrete rad-hard and rad-tolerant products can be found here.

The first radiation interaction worthy of discussion is Total Ionizing Dose (TID). Qualification tests for this are carried out as per MIL STD 883, TM1019 to simulate the long-term exposure effects of space. The tests are carried out in a reactor over a fairly low dose rate, for a fairly long time to achieve a total fluence of 50 Krad to 300 Krad and beyond in some cases.

If we first look at the Bipolar Junction Transistor (BJT), the data always shows that TID impacts the gain of the structure (Hfe). Higher fluence shows more gain degradation.

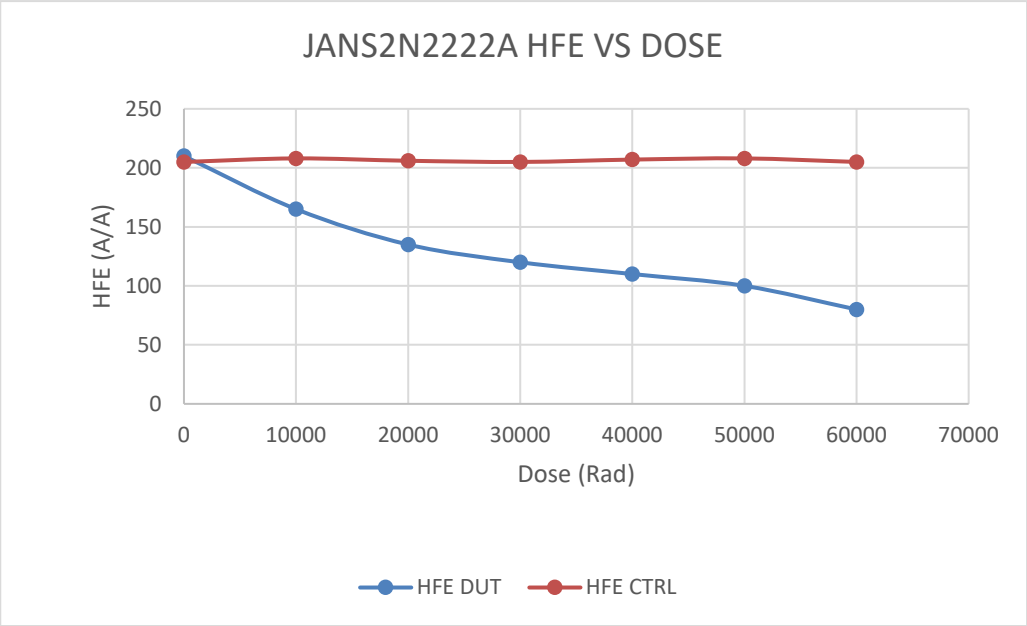


Figure 1: Hfe vs Fluence

The mechanism for this is fairly straight forward. The Co60 radiation source causes ionic interactions. On the surface of the BJT, electron hole pairs are formed at radiation interaction sites. These electron hole pairs tend toward the opposite charge, this is to say that in a biased NPN, that the electrons will tend toward the base (more positively biased), and the holes will tend toward the emitter (negatively biased WRT the base). The electrons recombine quickly and don't really cause a problem in the base region. The holes, however, are then attracted near the surface of a vertical BJT structure. For the same collector current in the presence of these holes, the base current has to be higher—a clear degradation of Hfe.

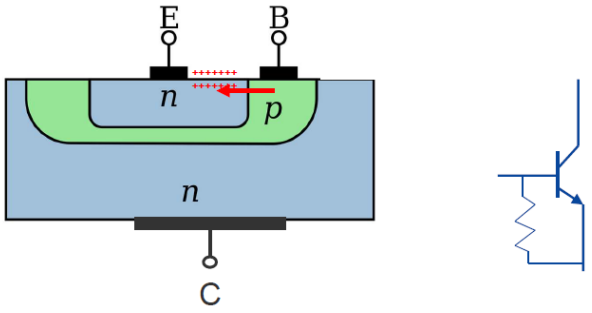


Figure 2: Picture of BJT structure and schematic symbol showing interaction and effect

The effects go beyond simply degrading the gain. The order of the BJT structure was disturbed. In this, we'd expect the off-state leakage current to go up and some impact on VCBO or VEBO. The good news is that the collector is a fairly thick region, well below the BE junctions near the surface of the BJT. The collector base junction isn't as heavily doped as the BE junction, thereby the CB junction is the faster of the two in terms of recombination. So much so that for most any BJT one may consider, VCBO is always higher than VCEO. The higher the gain of the structure, the larger the discrepancy. The collector base always blocks the off-state voltage first. The BE junction comes in sometime later, after the minority carriers in the BE junction recombine (emitter storage time). Higher gain in a BJT is higher storage time.

VCBO is usually unimpacted by TID, however VCEO rises with increasing fluence. The mechanism that causes the VCEO rise is a little counterintuitive. If Hfe degrades, then the emitter storage time has to drop, which is to say that the BE junction recombines faster with increasing fluence. Some might recall the old days of Baker clamps, proportional base drive and switched emitter technologies where this was often hard learned and well retained. If the BE storage time degrades, and VCBO remains unscathed by the radiation, VCEO can then only go up. To offset this, a power designer might consider the use of a Baker clamp to steer the initial base drive overage through the collector.

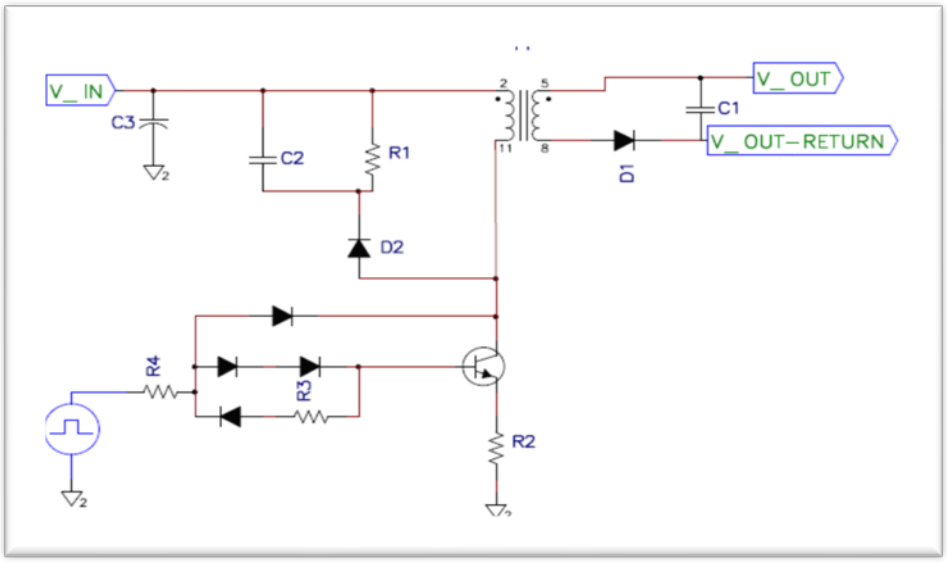


Figure 3: Baker clamp schematic in small flyback converter

As the mission is carried out and the gain drops, VCEsat of the BJT remains fairly constant and the Baker clamp steers less "overdrive" through the collector. It is important to recall that in a bipolar IC process there are MANY layers of BJT structures, with hundreds, perhaps thousands, of BJTs interacting. This discussion is scalable to these technologies.

A MOSFET has similar TID interactions, only with much different effects. The MOSFET tends to trap the charged particles in the gate oxide near the gate. For an N-channel enhancement mode MOSFET, this is when the device is in the off state where VGS is a maximal negative voltage and VDS is blocking. In the N-channel case, the threshold shifts downward with increasing fluence. For a P-channel MOSFET, this

means that the threshold voltage shifts upward with increasing fluence. Again, considering the order of the structure and the perturbation, RDSon can be degraded slightly by increasing fluence and off state leakage generally increases a bit.

To design for these things is simpler. Make absolutely certain the gate drive to the MOSFET is pristine. Make the on state much higher than the threshold, yet somewhat lower than VGS max to keep from stressing the gate oxide. Make the off state low enough to hold the device off through fastest commutation and Cdv/dt charging effects coupling into the drive circuitry through the Miller capacitance (Crss). This will counter the threshold drift effects (sometimes referred to as hole trapping) as well as bolster the off-state immunity of the device as temperature rises and threshold drops additionally.

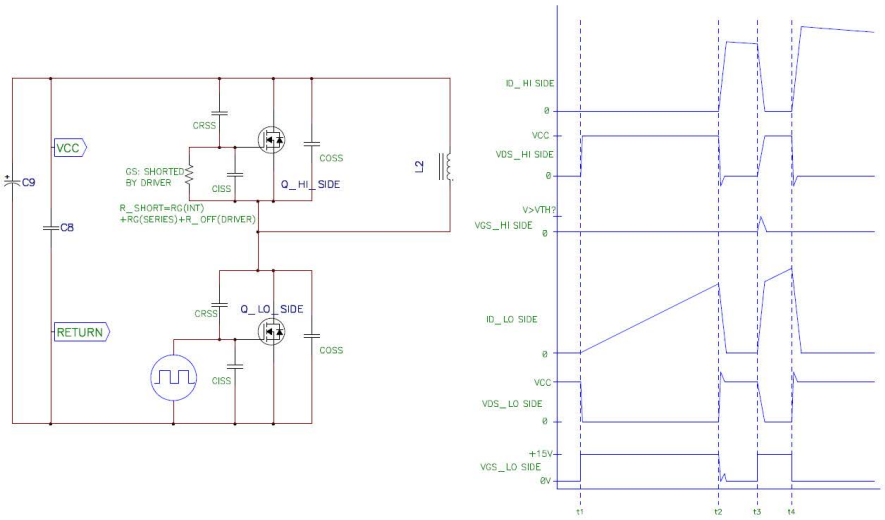


Figure 5: Double pulse circuit and waveform sketches showing Cdv/dt turn on at t3

The same extension for BJTs applies to MOSFETs in a BiCMOS process. The layers and interactions increase dramatically in a BiCMOS IC. In the next edition, I will briefly discuss single-event effects in these same devices.

For more information, please contact Paul L. Schimel PE, Senior Staff Engineer, Microchip Aerospace and Defense group at
Paul.schimel@microchip.com

NOTIFICATION

RTG4 PLL Lock Stability Customer Notification Addendum

Customer notification CN19009A is an addendum to CN19009 regarding the RTG4 FPGA PLL lock stability over temperature issue under investigation. This addendum provides a reminder of the issue's description, root cause, PLL loss of lock characterization status, and workarounds status. Microchip is actively investigating a workaround to completely mitigate the temperature dependence across the full military temperature operating range. CN19009A customer notification addendum can be downloaded here.

For more information, please contact Minh Nguyen, Principal Engineer, Product Marketing, Space and Aviation: Minh.Nguyen@microchip.com

EVENTS

Space Forum 2019 Archives

Microchip's most recent Space Forum events in October and November 2019 provided a showcase for our most innovative space-related products, capabilities, and system solutions. We provided demonstrations of how the interoperation of our latest products can accelerate your development time, and showed how Microchip's Sub-QML and COTS-to-RT components help address the challenges of meeting system performance and reliability goals while also saving costs. Updates on radiation testing, reliability and qualification testing were provided, and details on new products including FPGAs, clocks, oscillators, mixed signal devices, microcontrollers and microprocessors were presented. You can watch videos of our virtual events and download the presentations here.

Microelectronics Reliability and Qualification Workshop (MRQW) – El Segundo, CA (Feb. 4–6)

Hosted by the Aerospace Corporation, this workshop covered topics on microelectronics reliability and qualification for aerospace engineers, system designers and electrical engineers. This highly specialized workshop featured keynote speakers who shared the latest information and findings in microelectronics. Microchip presented "Saving Power and System Cost with Next-Generation Radiation Tolerant FPGAs," which discussed important updates to RTG4 and RT PolarFire FPGAs. Click here to learn more.

Space Parts Working Group (SPWG), Torrance, CA, (May 5–6)

SPWG is sponsored by The Aerospace Corporation in cooperation with the U.S. Air Force Space and Missile Systems Center and the National Reconnaissance Office. In its 48th year, SPWG is an unclassified, international forum for disseminating information to the aerospace industry and for resolving problems with high-reliability electronic piece parts for space applications. Microchip will present updates about its radiation-hardened and radiation-tolerant portfolio to suppliers, manufacturers, and government agencies.

Click here for more information. For questions please contact:

Ken O'Neill, Director of Marketing, Space and Aviation:
Ken.ONeill@microchip.com

Dorian Johnson, HiRel Product Line Marketing Manager:
Dorian.Johnson@microchip.com

Julian Di Matteo, Senior Engineer, Product Marketing, Space and Aviation:
Julian.DiMatteo@microchip.com

Single-Event Effects Symposium/Military and Aerospace Programmable Logic Design Conference (SEE/MAPLD) – La Jolla CA (May 18–21)

SEE/MAPLD brings together radiation experts, firmware engineers, digital design engineers and program managers to discuss important topics related to single-event effects and programmable electronics designed into military and aerospace applications. At this 29th annual event, Microchip will exhibit and provide important updates on its radiation-tolerant and radiation-hardened portfolio. We will demonstrate a Smart Embedded Vision (SEV) object recognition demo on a 28 nm SONOS PolarFire FPGA. Click here to learn more.

For questions please contact:

Dorian Johnson, HiRel Product Line Marketing Manager:
Dorian.Johnson@microchip.com

Julian Di Matteo, Senior Engineer, Product Marketing, Space and Aviation:
Julian.DiMatteo@microchip.com

Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, Arizona, USA 85224-6199
(480) 792-7200 | www.microchip.com