CCSDS Telemetry Transmitter IP Core

A considerable number of Earth Observation missions are based on small satellites class and embark payloads producing substantial data rates, thus requiring a reliable, efficient and economical payload data transmitter specialised for mid-range data rate, i.e. few hundred Mb/s.

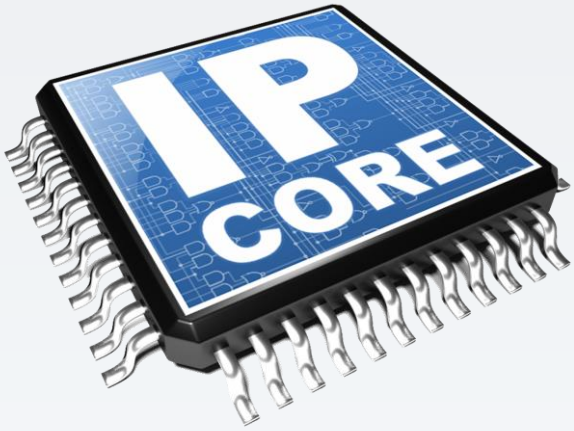
Such missions would benefit from employing state-of-the-art coding and modulation standard, allowing to exploit the protection offered by modern coding techniques while at the same time maximizing the supported data rates by using spectral efficient modulation formats.

The CCSDS Telemetry Transmitter IP Core is fully compliant with the CCSDS 131.2-B standard, combining powerful Serially Concatenated Convolutional Codes (SCCC) with modulations ranging from QPSK to 8PSK and 16-, 32- and 64-APSK, offers precisely such benefits, together with a high degree of flexibility. Such flexibility, thanks to the number of modulation and coding formats (ModCod) provided, will help configuring the system to better adapt to the specific target requirements.

The CCSDS Telemetry Transmitter IP core is in the process to be qualified as ESA IP core.

Key Features

- Fully compliant with CCSDS 131.2-B standard
- Support of all the 27 ModCods in a single instantiation for high capacity FPGA technologies for space
- High data-rate IP Core option for symbol rates higher than 400 Mbaud and input data rates higher than 2 Gb/s
- Low-complexity IP Core option for implementation on antifuse technology (e.g. RTAX2000 FPGA)
- Includes symbol pre-distortion to mitigate non linearity
- Optional Square-Root Raised Cosine baseband filtering
- Optional SEE mitigation mechanisms
- IP core generator Graphical User Interface to configure and generate the IP core according to the needs of the end-user
- Coded in technology-independent, highly configurable VHDL
- Validated on the new Microsemi RTG4 development kit



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Architectural features

The CCSDS Telemetry Transmitter IP core is composed of the following functional blocks:

The **Slicer** splits the input CADU stream into a sequence of information blocks of appropriate length for SCCC processing.

The **SCCC encoder** implements the encoding functions specified in the CCSDS standard, i.e., outer encoder, interleaver, inner encoder, row-column interleaver.

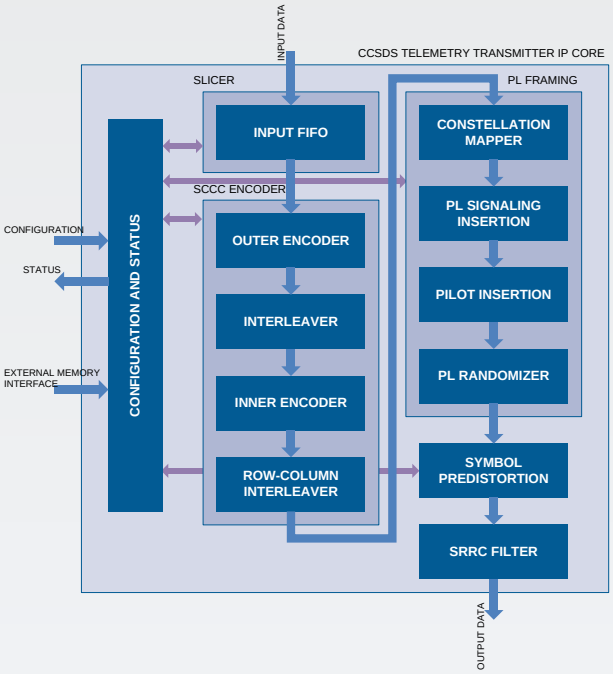
The **Physical Layer (PL) framing** implements symbol mapping according to the selected modulation scheme, frame header generation, optional pilot insertion and randomization.

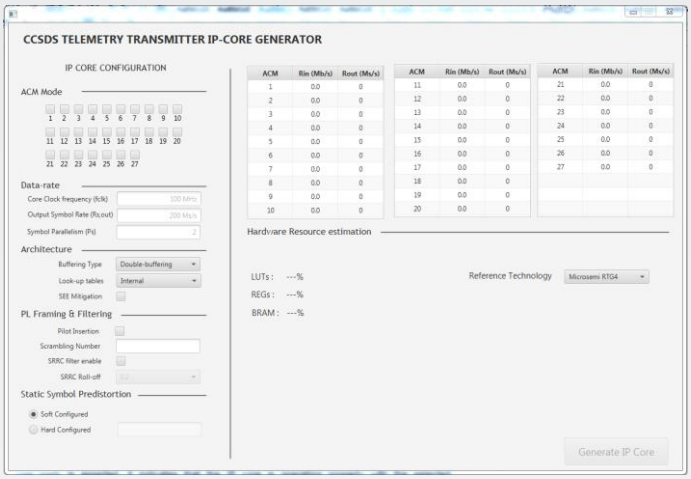
Symbol Pre-Distortion applies static pre-distortion parameters in order to compensate for amplitude/phase non-linearity in the transmitter power amplifier.

Square Root Raised Cosine (SRRC) filter is an optional block that performs pulse-shaping on I and Q arms, with selectable roll-off. This block can be excluded in case SRRC filtering is carried out by other components in the transmission chain.

The IP core was designed using a fully synchronous approach limiting clock-domain-crossings at IP core interfaces. The input asynchronous FIFO guarantees safe integration in the host system.

Several mitigation techniques are provided to reduce the effects of radiations, including register protection, safe finite-state machine implementation and RAM protection.





Configurability

The CCSDS Telemetry Transmitter IP core has many options for configuration, in order to be flexible and to be easily plugged into complex systems.

Hard configuration parameters allow architectural optimization to tailor the specific IP core instantiation to the target application. The IP core comes with a dedicated IP core generator software tool to easily set all those parameters. The user can just set system-level requirements and the tool generates the IP core accordingly. The IP core generator GUI also reports the estimated performance on some reference target technology.

Soft configuration allows the selection of ModCod, pre-distortion parameters at run-time and can be set through the Configuration & Status Interface.

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