PolarFire® SoC CPU Performance Benchmarking

Introduction

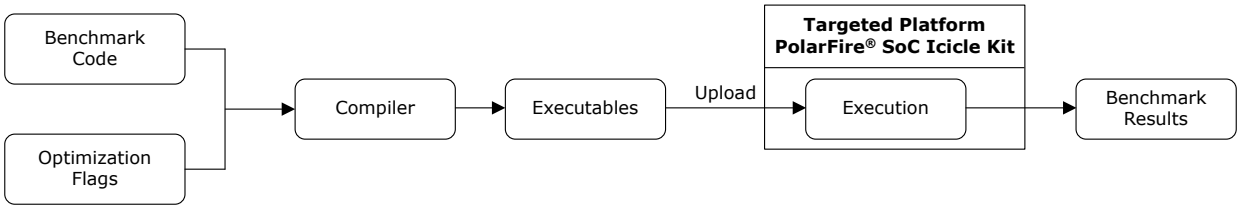
Microchip's PolarFire SoC FPGAs include the industry's RISC-V based Microprocessor Subsystem (MSS) and FPGA fabric that inherits all the features of the PolarFire family. The PolarFire SoC MSS includes 5x 64-bit RISC-V processor cores, AXI Switch, DDR Controller, Fabric Interface Controllers (FIC), and a rich set of peripherals. It also offers an unparalleled combination of low power consumption, thermal efficiency, and defence-grade security for smart, connected systems. It is the first SoC FPGA with a deterministic L2 memory subsystem enabling real-time applications. Built on the award-winning, mid-range, low power PolarFire FPGA architecture, PolarFire SoC devices deliver up to 50% lower power than alternative FPGAs, span from 25k to 460k logic elements, and feature 12.7G transceivers.

PolarFire SoC devices include L1 cache, L2 cache, DDR controller, and eNVM (embedded non-volatile memory) to execute user applications on U54 (Application Processor) cores. The L1 iCache can be used as ITIM (Instruction Tightly Integrated Memory) for code execution. The L2 Cache can be used as LIM (Loosely Integrated Memory) or Scratchpad. The external DDR memory such as LPDDR4 can also be interfaced using the DDR controller. The eNVM can be used for storing instructions and code execution. For more information, see PolarFire SoC FPGA MSS Technical Reference Manual.

This white paper describes CPU performance results based on the industry-standard performance benchmarking suites such as Dhrystone (Bare Metal), CoreMark (Bare Metal and Linux), and CoreMark-PRO (Linux) which are executed on the Application Processor Cores (U54, which uses RISC-V Architecture RV64GC) using the PolarFire SoC Icicle kit. The performance benchmarking suites are compiled with the GCC compiler on the RISC-V platform to evaluate the performance of embedded processors.

The following figure shows the execution methodology for the performance benchmarking suites. These performance suites are executed by applying different levels of optimization flags. All the computations are model-driven runtime (MDR), which uses all the aforementioned flags, trade-offs during the runtime to get the best performance results.

Figure 1. Execution Methodology for the Performance Benchmarking Suites



This white paper provides the summary of results after executing the benchmark applications from LIM, ITIM, eNVM, Scratchpad, and LPDDR4. The following table lists the system configuration common to all the performance benchmark suites.

Table 1. System Configuration

System Configuration	Description
Product and Architecture	Icicle kit, RISC-V
Platform	Dhrystone—Bare Metal
	CoreMark—Bare Metal and Linux
	CoreMark-PRO—Linux
CPU Core Frequency	600 MHz
External Memory Access	LPDDR4
LPDDR4 Frequency	800 MHz
Compiler	GCC
Toolchain for Linux	riscv64-oe-linux-gcc (v11.1.0)
Toolchain for Bare Metal	riscv64-unknown-elf-gcc (v8.3.0)

Attention: The benchmarking results depend on the tool chains, compiler flags such as optimization level, single core, or quad cores.

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1. Dhrystone

The industry standard Dhrystone v2.2 is executed on one of the RISC-V CPU cores of the PolarFire SoC target platform. The Dhrystone suite remains intact with the application even after changing the wrapper code that allows different levels of execution timings on the PolarFire SoC Icicle kit. Dhrystone suite is adapted to get the processor performance, which plays an important role in the non-numeric system programming and emulates the processor usage with the help of certain common set of programs. The benchmarking value shows the iterations of the program executed by the processor at a particular time frame and normalizes to per MHz of CPU clock frequency.

The Dhrystone program gets the comparative performance differences between the external and internal memory settings along with the system settings. The Dhrystone suite features a well-structured code base, which takes full advantage of the wrapper code resulting in optimal biased configuration to get the best performance results.

Following are the key features of Dhrystone:

- Well-suited for embedded CPUs
- Provides great comparison of the compiler performances
- Performs synthetic benchmarks to compare different system architectures
- Has a very small binary footprint, which determines the CPU's benchmarking quickly

For more information about Dhrystone, see en.wikipedia.org/wiki/Dhrystone.

1.1 Dhrystone on Bare Metal

To execute a benchmarking test suite, it must be self-contained to allow its execution on the hardware directly. This is necessary at the start of an SoC design to evaluate and establish correlations of expected integer performance.

1.1.1 Results

The following table lists the Dhrystone benchmarking results for one Application Processor Core U54 running Bare Metal using the PolarFire SoC Icicle Kit.

Table 1-1. Dhrystone Benchmarking Results on Bare Metal

Dhrystone	Bare Metal					
Memory Section	LIM (1.8 MB)	ITIM (28 KB)	eNVM (128 KB)	eNVM (128 KB)	Scratchpad mem (512 KB)	LPDDR4
Code (main loop is run from)	LIM	ITIM	eNVM	eNVM	Scratchpad	LPDDR4
Stack located in	LIM	Scratchpad	LIM	Scratchpad	Scratchpad	LPDDR4
Dhrystone Result (DMIPS/MHz)	**0.58**	**1.58**	**0.47**	**0.975**	**1.714**	**1.714**
Code Size	Full image size is around 70 KB. Dhrystone main loop is less than 2 KB.					Full image size is around 63 KB
Compiler Flags	-pipe -fno-builtin-printf -mexplicit-relocs -fpredictive-commoning -fprofile-report -fstack-usage -fmem-report -flto-report -fipa-pta -fipa-cp-clone -fdevirtualize-speculatively -fdevirtualize-at-ltrans -fira-region=all -fira-hoist-pressure -fira-loop-pressure -fno-stack-limit -fno-inline -fno-common -falign-functions=4 -ffunction-sections -fdata-sections					

2. CoreMark

CoreMark is a benchmarking suite that is intended for the performance of the CPU, when running with specific workloads. The internal CPU architecture is independent of the on-chip memory and peripherals. CoreMark focuses on processor core and cache memory read/write by utilizing the CPU pipeline architecture. The advantage of CoreMark is its size, which allows CoreMark to easily fit in a processor's memory and makes it suitable to get the performance outcome. To evaluate processor performance, CoreMark uses about 20k size of code, which includes I/O computations. All the computations are made at run time. CoreMark mainly focuses on basic read/write operations and integer operations. CoreMark uses realistic workloads. The CoreMark workload comprises of several commonly used algorithms, including:

- Matrix manipulation, to exercise common math operations.
- Linked list manipulation, to exercise the common use of pointers.
- State machine operation, to exercise data-dependent branches.
- Cyclic Redundancy Check (CRC) is a common function in the embedded systems.

The outcome of the CoreMark execution is as follows:

- The four bits of workload tested are matrix manipulation, linked lists, state machines, and CRCs. The output of each stage of the compilers is intended to get the best outcome of the performance results.
- PolarFire SoC device can load the entire test in the cache, DDR, and Flash memory.

The GCC on the RISC-V gives a good performance with -O2 optimization compiler flag and without a compressed extension (RVC).

For more information about CoreMark, see EEMBC.

2.1 CoreMark Benchmarking Results using Signed Index

The CoreMark benchmarking results are captured for one Application Processor Core U54 for both Bare Metal and Linux. The following table lists the CoreMark benchmarking results when signed index is used as loop counter. RISC-V is designed to be more efficient in handling the common case loop index variables in the form of “(signed) int”. Hence, a typedef in the header file was modified to be a signed data type (ee_u32).

Table 2-1. CoreMark Benchmarking Results when Signed Index is used as Loop Counter

CoreMark	Bare Metal						Linux
Memory Section	LIM (1.8 MB)	ITIM (28 KB)	eNVM (128 KB)	eNVM (128 KB)	Scratchpad mem (512 KB)	LPDDR4	LPDDR4
Code (main loop is run from)	LIM	ITIM	eNVM	eNVM	Scratchpad	LPDDR4	LPDDR4
Stack located in	LIM	Scratchpad	LIM	Scratchpad	Scratchpad	LPDDR4	LPDDR4
CoreMark Result (CoreMark/MHz)	**0.950**	**3.128**	**0.950**	**3.030**	**3.128**	**3.128**	**3.125**
Code Size	Full application image size is 70 KB. CoreMark code size is less than 20 KB.					Full image size is around 50 KB	

.....continued		
CoreMark	**Bare Metal**	**Linux**
Compiler Flags for Bare Metal	-Wno-maybe-uninitialized -fno-common -funroll-loops -finline-functions -falign-functions=16 -falign-jumps=4 -falign-loops=4 -finline-limit=1000 -fno-if-conversion2 -fselective-scheduling -fno-tree-dominator-opts	
Compiler Flags for Linux	-O3 -O2 -DPERFORMANCE_RUN=1 -DHAS_STDIO -DHAS_TIME_H -DUSE_CLOCK -fno-common -funroll-loops -finline-functions -falign-functions=16 -falign-jumps=4 -falign-loops=4 -finline-limit=1000 -fno-if-conversion2 -fselective-scheduling -fno-tree-dominator-opts -lpthread -DHAS_FLOAT=0 -mtune=sifive-7-series -lrt	

Note:
CoreMark application chooses heap or stack during its run. Here, it is configured for stack.

2.2 CoreMark Benchmarking Results using Unsigned Index

The following table lists the CoreMark Benchmarking results using default header file (with no modifications to the typedef unsigned int ee_u32).

Table 2-2. CoreMark Benchmarking Results when Unsigned Index is used as Loop Counter

CoreMark	**Bare Metal**						**Linux**
Memory Section	LIM (1.8 MB)	ITIM (28 KB)	eNVM (128 KB)	eNVM (128 KB)	Scratchpad mem (512 KB)	LPDDR4	LPDDR4
Code (main loop is run from)	LIM	ITIM	eNVM	eNVM	Scratchpad	LPDDR4	LPDDR4
Stack located in	LIM	Scratchpad	LIM	Scratchpad	Scratchpad	LPDDR4	LPDDR4
CoreMark Result (CoreMark/MHz)	**0.92**	**2.645**	**0.916**	**2.568**	**2.65**	**2.65**	**2.56**
Code Size	Full application image size is 70 KB. CoreMark code size is less than 20 KB.					Full image size is around 50 KB	
Compiler Flags for Bare Metal	-Wno-maybe-uninitialized -fno-common -funroll-loops -finline-functions -falign-functions=16 -falign-jumps=4 -falign-loops=4 -finline-limit=1000 -fno-if-conversion2 -fselective-scheduling -fno-tree-dominator-opts						
Compiler Flags for Linux	-O3 -O2 -DPERFORMANCE_RUN=1 -DHAS_STDIO -DHAS_TIME_H -DUSE_CLOCK -fno-common -funroll-loops -finline-functions -falign-functions=16 -falign-jumps=4 -falign-loops=4 -finline-limit=1000 -fno-if-conversion2 -fselective-scheduling -fno-tree-dominator-opts -lpthread -DHAS_FLOAT=0 -mtune=sifive-7-series -lrt						

Note:
CoreMark application chooses heap or stack during its run. Here, it is configured for stack.

3. CoreMark-PRO

CoreMark-PRO is a comprehensive, advanced processor benchmark working with CoreMark. When a CoreMark stresses the CPU pipeline, CoreMark-PRO tests the entire processor and memory subsystem, adding support for the following:

- Multi-core and a combination of integer
- Floating-point workloads
- Data sets for using larger memory subsystems

Data sets, depending on the task, ranging from 42 kB to 3 MB, stresses the multi-core devices that the code can launch multiple threads, with parallelism in the workload.

The CoreMark-PRO contains five integer workloads and four popular floating-point workloads. The integer workloads include JPEG compression, ZIP compression, an XML parser, the SHA-256 Secure Hash Algorithm (SHA), and a more memory-intensive version of the original CoreMark. The floating-point workloads include a Fast Fourier Transform (FFT), a linear algebra routine derived from LINPACK, a greatly improved version of the Livermore loops benchmark, and a neural net algorithm to evaluate patterns.

The CoreMark-PRO execution utilizes the MultiBench comprehensive suite to evaluate the performance of PolarFire SoC device. The MultiBench comprehensive suite utilizes Multi Instance Test Harness (MITH), which provides a framework to coordinate scalability analysis. The MultiBench framework evaluates the performance of scalability, Single-core, Multi-core, memory bandwidth, OS scheduling support, and compiler benchmarking.

For more information about CoreMark-PRO, see EEMBC.

3.1 CoreMark-PRO on Linux

To execute the CoreMark-PRO on Linux platform for optimal benchmarking results on PolarFire SoC Icicle kit, run each workload with single/multi workers, configure the number of workers to get the better scaling for each workload. These values are obtained by passing workloads using XCMD flags as XCMD='-c4 -w4 -v1 -i4 ' to the make command, which in turn utilizes the Perl script to get the values as listed in Table 3-1.

3.1.1 Results

The following table lists the CoreMark-PRO benchmarking results using four application U54 cores with L2 cache size configured to 1.5 MB. CoreMark-PRO provides a score (Iterations/Sec) for Multi-core and Single-core with a scaling factor. The scaling factor depends on the workload. For more information about the workloads and scaling factor, see EEMBC CoreMark-PRO User Guide.

Table 3-1. CoreMark-PRO Benchmarking Results on Linux

Workload	Multi-Core (Iterations/sec)	Single-core (Iterations/sec)	Scaling
core	0.35	0.09	3.89
loops-all-mid-10K-sp	0.65	0.20	3.25
nnet_test	0.93	0.28	3.32
parser-125k	8.47	2.34	3.62
zip-test	21.74	5.99	3.63
linear_alg-mid-100x100-sp	18.66	4.85	3.85
sha-test	26.53	8.00	3.32
radix2-big-64k	42.93	20.48	2.10
cjpeg-rose7-preset	47.17	12.21	3.86
Results	**802.42**	**237.68**	**3.38**

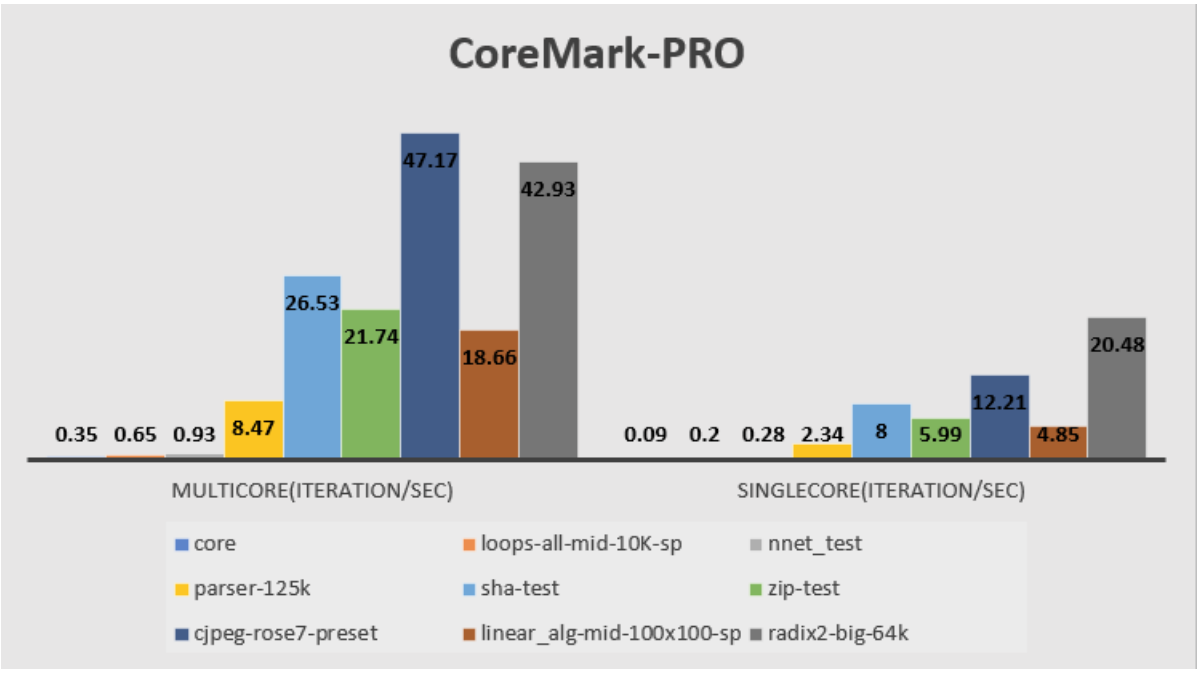
The following figure shows the CoreMark-PRO execution.

Figure 3-1. CoreMark-PRO Execution

```
WORKLOAD RESULTS TABLE

                                                  MultiCore SingleCore
Workload Name                                     (iter/s)  (iter/s)    Scaling
------------------------------------------------- --------- ---------- ---------
cjpeg-rose7-preset                                   47.17      12.21       3.86
core                                                  0.35       0.09       3.89
linear_alg-mid-100x100-sp                            18.66       4.85       3.85
loops-all-mid-10k-sp                                  0.65       0.20       3.25
nnet_test                                             0.93       0.28       3.32
parser-125k                                           8.47       2.34       3.62
radix2-big-64k                                       42.93      20.48       2.10
sha-test                                             26.53       8.00       3.32
zip-test                                             21.74       5.99       3.63

MARK RESULTS TABLE

Mark Name                                         MultiCore SingleCore    Scaling
------------------------------------------------- --------- ---------- ---------
CoreMark-PRO                                        802.42     237.68       3.38
make[2]: Leaving directory '/home/root/coremark-pro'
make[1]: Leaving directory '/home/root/coremark-pro'
root@icicle-kit-es:~/coremark-pro#
root@icicle-kit-es:~/coremark-pro#
root@icicle-kit-es:~/coremark-pro#
root@icicle-kit-es:~/coremark-pro# lscpu
Architecture:        riscv64
Byte Order:          Little Endian
CPU(s):              4
On-line CPU(s) list: 0-3
Thread(s) per core:  4
Core(s) per socket:  1
Socket(s):           1
CPU MHz:             0.00
L1d cache:           32 KiB
L1i cache:           32 KiB
root@icicle-kit-es:~/coremark-pro#
root@icicle-kit-es:~/coremark-pro#
root@icicle-kit-es:~/coremark-pro#
root@icicle-kit-es:~/coremark-pro#
```

The following figure shows the representation of CoreMark-PRO benchmarking results.

Figure 3-2. Comparison Between Mutli-core and Single-core



4. Summary of PolarFire SoC Benchmarking Results

The following table lists the summary of results of benchmarking suites. The best performance results are achieved by running the application code from the Scratchpad or LPDDR4.

Table 4-1. Summary of PolarFire SoC Benchmarking Results

Benchmarks	Platform	Result
Dhrystone	Bare Metal	1.714 DMIPS/MHz
CoreMark	Bare Metal	3.128 CoreMarks/MHz
	Linux	3.125 CoreMarks/MHz
CoreMark-PRO	Linux	Multi-Core 802.42 (Iterations/sec)
		Single-Core 237.68 (Iterations/sec)

5. Conclusion

This white paper describes the toolchain, compiler and optimization flags, and the process for running benchmarks such as Dhrystone, CoreMark, and CoreMark-PRO using the PolarFire SoC Icicle kit.

The best performance results are achieved when code is executed from L2 Scratchpad memory or LPDDR4 memory. When executing applications from LIM, the instructions and data are not cached. LIM is intended for executing applications with deterministic behavior.

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