RN0240
Release Notes
Core10GBaseR_PHY v2.0

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at www.microsemi.com.

51300240. 1.0 7/20

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

This is the first publication of this document. Created for Core10GBaseR_PHY v2.0

Contents

Tables

2 Core10GBaseR_PHY

2.1 Overview

This release notes accompanies the production release of Core10GBaseR_PHY v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

Core10GBaseR_PHY DirectCore is designed to be used with PolarFire and PolarFire SOC devices. This core is used to interface the transceiver with the XGMII compliant MAC.

The IP core has the following features:

- 64-bit XGMII interface (MAC side)
- 64-bit gearbox mode (Transceiver side)
- Supports only 64B66B PCS encoding in transceiver
- Converts the gearbox signals to the XGMII signals on the transmit interface
- Receives the gearbox signals and adds/Deletes skip characters to absorb the +/-100 ppm variation and converts to XGMII format towards the MAC side

2.3 Delivery Types

Core is obfuscated and License Locked.

2.4 Supported Families

- PolarFire® SoC
- PolarFire®

2.5 Supported Tool Flows

Core requires Libero v12.2 or later.

2.6 Installation Instructions

The core must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the Add Core catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create a SmartDesign project using IP cores, see the *SmartDesign User guide*.

2.7 Documentation

This release contains a copy of the core Handbook. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and implementation suggestions.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

User Testbench is not provided with the core.

2.9 Release History

Table 1 lists the release history.

Table 1 • **Release History**

Version	Date	Changes
2.0	July, 2020	Initial release.

2.10 Discontinued Features and Devices

There are no discontinued features and devices.

2.11 Known Limitations and Workarounds

There are no known limitations and workarounds.