HB0923
Handbook
Core10GBaseR_PHY v2.0

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at www.microsemi.com.

Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document. Created for Core10GBaseR_PHY v2.0.

2 References

This section lists documents that provide more information about concepts and features covered in this user guide.

- *UG0686 - Microsemi PolarFire FPGA User Guide*
- *UG0677 - PolarFire FPGA Transceiver User Guide*

3 Introduction

3.1 Overview

Core10GBaseR_PHY is an IP that converts the transceiver gearbox signals into the XGMII format. This IP is needed to interface the Transceiver with the XGMII compliant MAC.

3.2 Features

The IP core has the following features:

- 64-bit XGMII interface (MAC side)
- 64-bit gearbox mode (Transceiver side)
- Supported for only 64B66B PCS encoding in the transceiver
- Converts the gearbox signals to the XGMII signals on the transmit interface
- Receives the gearbox signals and adds/deletes skip characters to absorb the +/-100 ppm variation and converts to XGMII format towards the MAC side

3.3 Core Version

This handbook is for Core10GBaseR_PHY version 2.0.

3.4 Supported Families

- PolarFire® SoC
- PolarFire®

3.5 Device Utilization and Performance

Device utilization and performance data is provided in Table 1 for the supported device families. The data listed in this table is indicative only. The overall device utilization and performance of the core is system dependent.

Table 1 • **Device Utilization and Performance**

Family	Utilization (Logic Elements)				Performance (MHz)			
Device	Sequential	Combinational	uSRAM(1K)	Total %	I_TX_CLK	I_RX_CLK	I_XGMII_TXCLK	I_XGMII_RXCLK
PolarFire Soc	2657	1684	12	1.0	230	210	420	216
PolarFire	2738	1641	12	1.0	250	230	500	250

Note: The data in this table is achieved using typical synthesis and layout settings. Frequency (in MHz) was set to 100 and speed grade was -1.

4 Interface

4.1 Ports

All the input and output ports of the core are listed in the following table.

Table 2 • **Input and Output Signals**

Port name	Width	Direction	Description
Clock and Reset			
I_TX_CLK	1	Input	Transmit clock of 161.133 MHz provided by the transceiver.
I_RX_CLK	1	Input	Recovered clock of 161.133 MHz provided by the transceiver.
I_TXCLK_RESETN	1	Input	Active low asynchronous reset input to reset transmit logic. This reset is internally synchronized with I_TX_CLK.
I_RXCLK_RESETN	1	Input	Active low asynchronous reset input to reset receive logic. This reset is internally synchronized with I_RX_CLK.
Transceiver Rx Gearbox Interface			
I_PMA49_RX_GRBX_LOCK	1	Input	PMA Rx gearbox lock signal.
I_PMA49_RX_GRBX_SOS	1	Input	Start-of-sequence pulse. Sequence is the span of clock beats over which uniquely different parts of block symbols are transferred across the interface on each of the clock beats. Length of a sequence varies with block size and active width of interface. **Note:** For 66-bit blocks and a 64-bit interface the sequence length is 33 clock beats.
I_PMA49_RX_GRBX_HDR_EN	1	Input	Enable for header. When I_PMA49_RX_GRBX_HDR_EN =1 for a clock beat, then valid sync header bits are transferred.
I_PMA49_RX_GRBX_DATA_EN	1	Input	Data enable is 1 for a clock beat when data is present on I_PMA49_RX_GRBX_DATA. Over a sequence there are clock beats which convey no data. For 66-bit blocks and a 64-bit interface there is one dead cycle on beat 32.
I_PMA49_RX_GRBX_HDR	4	Input	Sync header corresponding to different encoding types. Bits [1:0] contain header in 64B66B mode while in 64B67B mode, bits [2:0] contain the header.
I_PMA49_RX_GRBX_DATA	64	Input	Data received from PMA in gearbox mode.
Transceiver Tx Gearbox Interface			
O_PMA49_TX_GRBX_SOS	1	Output	Start-of-sequence pulse. Length of a sequence varies with block size and active width of interface. **Note:** For 66-bit blocks and a 64-bit interface the sequence length is 33 clock beats.

Table 2 • **Input and Output Signals**

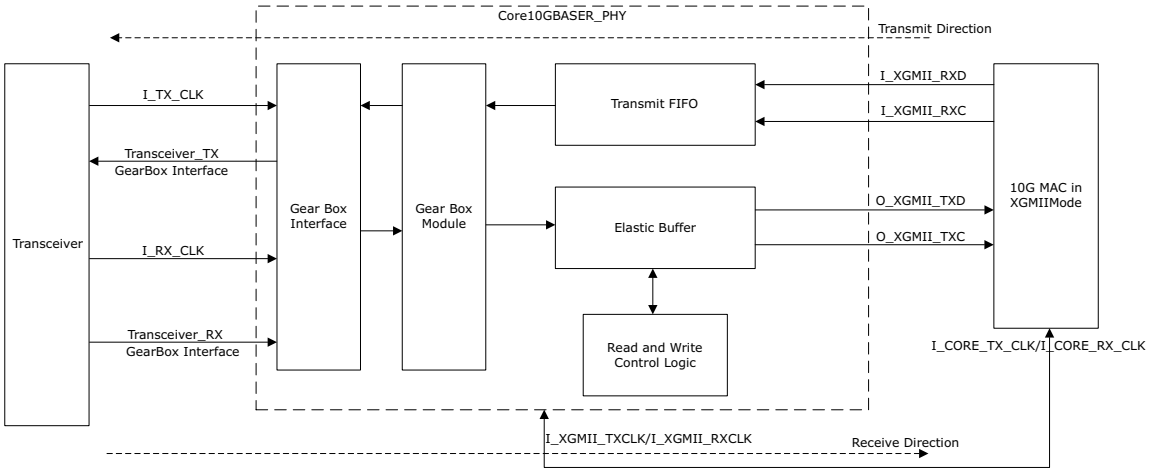
Port name	Width	Direction	Description
		Clock and Reset	
O_PMA49_TX_GRBX_HDR_EN	1	Output	Enable for header. When O_PMA49_TX_GRBX_HDR_EN =1 for a clock beat, then valid sync header bits are transferred.
O_PMA49_TX_GRBX_HDR	4	Output	Sync header corresponding to different encoding types. **Note:** Bits [1:0] contain header in 64B66B mode. The upper bits are driven [3:2} are driven with Logic'0'. In the transmit direction, the 64-bit transmit block is sent with the sync headers. For control blocks it carries value [1:0] = 'b10 Else [1:0] = 'b01.
O_PMA49_TX_GRBX_DATA_EN	1	Output	Data enable is 1 for a clock beat when data is present on O_PMA49_TX_GRBX_HDR_EN. Over a sequence there are clock beats which convey no data.
O_PMA49_RX_GRBX_DATA	64	Output	64-bit transmit data to PMA
		XGMII Signals	
I_XGMII_RXD	64	Input	XGMII RX data
I_XGMII_RXC	8	Input	XGMII RX control
O_XGMII_TXD	64	Output	XGMII TX data
O_XGMII_TXC	8	Output	XGMII TX control
		XGMII Clocks	
I_XGMII_TXCLK	1	Input	XGMII TX clock of 156.25 MHz
I_XGMII_RXCLK	1	Input	XGMII Rx clock of 156.25 MHz

5 Functional Description

Core10GBaseR_PHY is used to interface the transceiver to the XGMII compliant MAC. This IP has gearbox functionality to convert the transceiver transmit and receive gearbox signals to the XGMII format. It also performs the frequency/rate matching of the transceiver side clocks to the XGMII clocks.

The functional block diagram of the core is shown in Figure 1. Each of the functional blocks and the clocks/resets of the core is described as follows.

Figure 1 • **Functional Block Diagram**



5.1 Clocks and Reset

The Core10GBaseR_PHY IP operates in two frequency domains, one at the transceiver side and the other at the MAC side.

The transceiver transmit logic operates with the I_TX_CLK and the receive logic with I_RX_CLK. The transmit side of the MAC operates with the XGMII TX clock and receive side with XGMII RX clock.

The module has two reset signals as specified in the Reset section of Table 2, page 4 and both the resets are synchronized internally in the IP with the respective clocks.

5.2 Gearbox Interface

This module interfaces the gearbox's transmit and receive module with the Microchip's transceiver.

5.3 Gearbox Module

This module interfaces the gearbox interface logic to the transmit FIFO on the transmit path and with the elastic buffer on the receive path.

The gearbox module rate matches the transceiver's transmit clock with the transmit FIFO. This is achieved by inserting dead cycle every 32^{nd} cycle in the transmit sequence.

In the dead cycle there is no read performed. The transmit interface timing diagram is shown in Figure 3.

Similarly, the gearbox module rate matches the transceiver's receive clock with the elastic buffer. It is achieved by inserting the dead cycle every 32^{nd} clock cycle. The dead cycle is where the write is not performed. The receive timing diagrams are shown in Figure 2.

5.4 Transmit FIFO

It is a simple asynchronous FIFO of size 64x72 and used to interface the gearbox module with the MAC in the transmit path. The write logic of the transmit FIFO operates with the XGMII Tx clock and the read logic operates with the transceiver clock (I_TX_CLK).

5.5 Elastic Buffer

In the receive path, the elastic buffer interfaces between the gearbox and MAC. The elastic buffer has two functions:

- The elastic buffer performs write on transceiver's receive clock (I_RX_CLK) and reads on the XGMII clock (I_XGMII_RXCLK).
- The elastic buffer handles the ppm variation upto +/- 100PPM between the XGMII receive side MAC clock and the transceiver's receive clock.

5.6 Read and Write Control Logic

The read and write control logic controls the read and write into the elastic buffer module. This logic adds or deletes the idle characters depending upon the transceiver receive clock frequency.

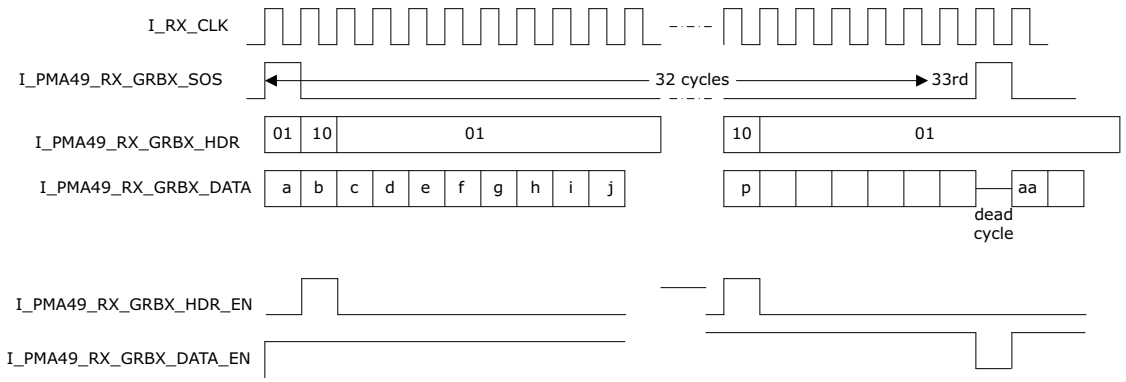
If the receive clock frequency (I_RX_CLK) is more than the XGMII MAC receive clock, the idles are removed, which means it is not written into the elastic buffer. If the receive clock frequency is less than the MAC receive clock, the idles are added after reading from the elastic buffer.

6 Timing Diagrams

6.1 Rx Gearbox interface

The following figure shows the timing diagram for Rx gearbox interface.

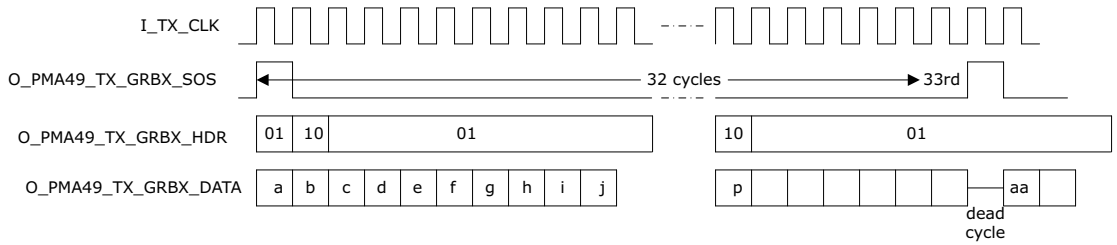
Figure 2 • **Timing diagram for Rx Gearbox Interface**



6.2 Tx Gearbox Interface

The following figure shows the timing diagram for Tx gearbox interface.

Figure 3 • **Timing diagram for Tx Gearbox Interface**



7 Tool Flow

7.1 License

Core is available as obfuscated.

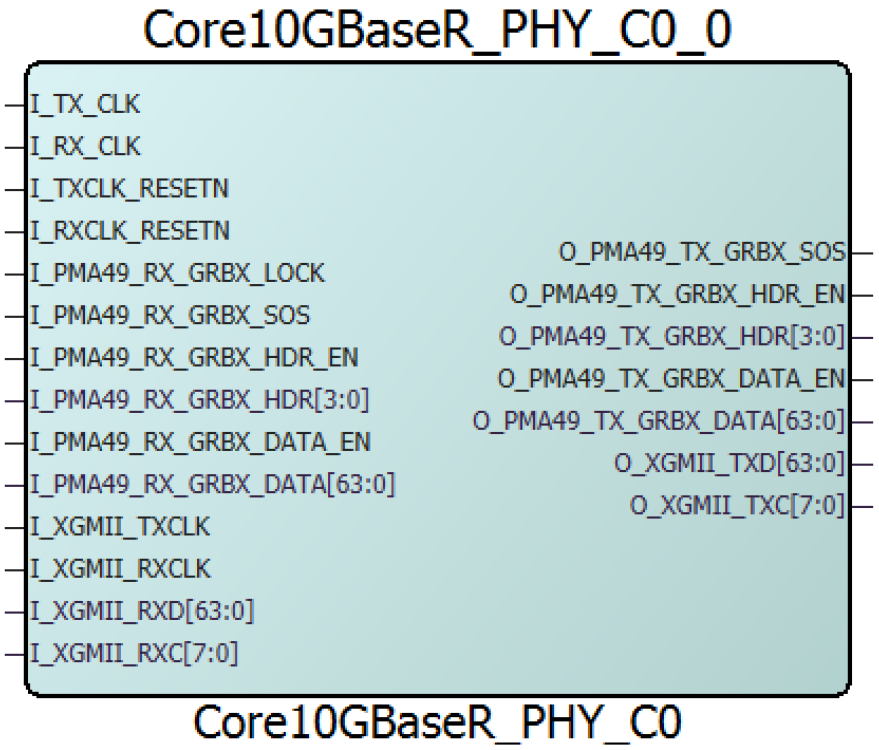
The obfuscated version is license locked and will be available only with Libero Gold and Platinum Licenses.

7.2 Using core in Libero SmartDesign

Core is pre-installed in the SmartDesign IP deployment design environment or can be downloaded from the online repository.

An example of the core instantiated in Libero SmartDesign is shown in Figure 4.

Figure 4 • **Core Instance Full I/O View in SmartDesign**



For more information about using the SmartDesign to instantiate and generate cores, see *Using DirectCore in Libero® SoC User Guide*.

7.3 Synthesis in Libero

To run synthesis on the core, set the design root to the IP component instance and run the **Synthesis** tool from the Libero **Design Flow** pane.

7.4 Place-and-Route in Libero

After the design is synthesized, run the **Place-And-Route** tool from the Libero **Design Flow** pane.

8 Testbench

A user testbench is not provided with the core.

9 System Integration

This section provides hints to ease the integration of the core. The block diagram Core10GBaseR_PHY IP connected to the 10G MAC over the XGMII interface is shown in Figure 5. The Libero SmartDesign is shown in Figure 6.

Figure 5 • **Block Diagram of 10G BaseR System**

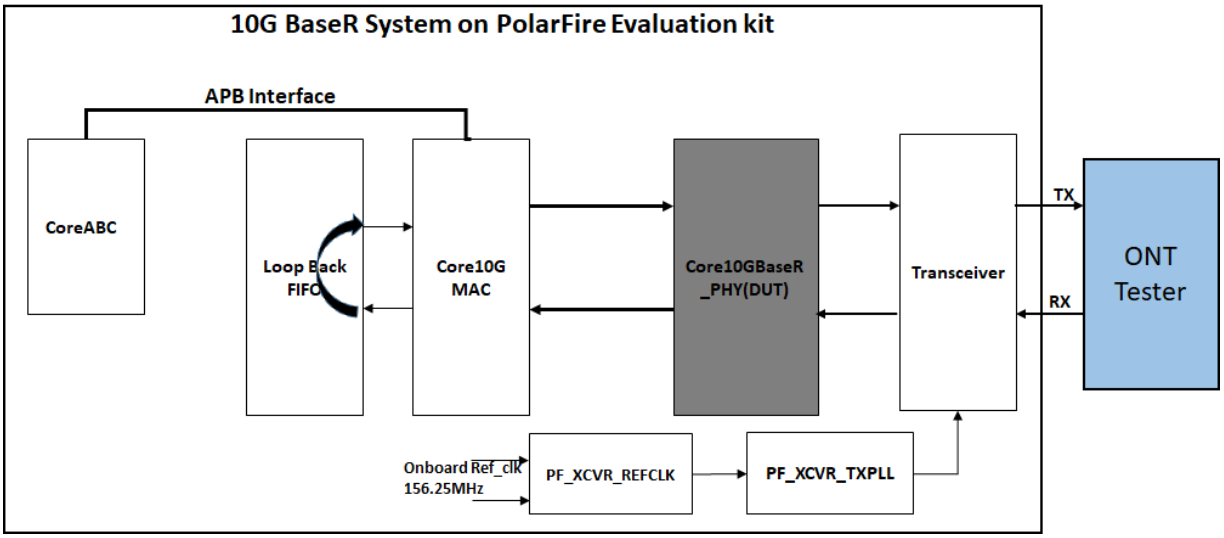


Figure 6 • **SmartDesign representation of 10G BaseR System**