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CoreRISCV_AXI4 v2.0 Release Notes

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About Microsemi

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Updated changes related to CoreRISCV_AXI4 v2.0.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreRISCV_AXI4 v1.0.

Contents

2 CoreRISCV_AXI4 v2.0 Release Notes

2.1 Overview

These release notes accompany the production release of CoreRISCV_AXI4 v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

CoreRISCV_AXI4 has the following features:

- Designed for low power ASIC microcontroller and FPGA soft-core implementations
- Integrated 8Kbytes instructions cache and 8 Kbytes data cache
- A Platform-Level Interrupt Controller (PLIC) can support up to 31 programmable interrupt with a single priority level
- Supports the RISCV standard RV32IM ISA
- On-Chip debug unit with a JTAG interface
- Two external AXI interfaces for IO and memory

2.3 Delivery Types

No License is required to use CoreRISCV_AXI4. Complete RTL source code is provided for the core.

2.4 Supported Families

- PolarFire
- RTG4™
- IGLOO®2
- SmartFusion®2

2.5 Supported Tool Flows

CoreRISCV_AXI4 v2.0 requires Libero® System-on-Chip (SoC) v11.7 or later.

2.6 Installation Instructions

The CoreRISCV_AXI4 CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the *CoreRISCV_AXI4 Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

No testbench is provided with CoreRISCV_AXI4.

The CoreRISCV_AXI4 RTL can be used to simulate the processor executing a program using a standard Libero generated HDL testbench.

2.9 Resolved History

Table 1 lists the release history for CoreRISCV_AXI4.

Table 1 • **Release History**

Version	Date	Changes
2.0	April 2017	• Separation of Top.v file into multiple files, one per module • Namespacing of files and module names • Added option to remove RAM for all inferences other than the ICache and DCache • Optimized DCache implementation which directly instantiates device specific LSRAM macros • Resolved debug instability issue allowing for a debug session to be restarted without an RST assertion • Added System Integration section to the handbook detailing the reset synchronization required on RST • Updated memory map in the handbook
1.0	November 2016	Initial release.

2.10 Known Limitations and Workarounds

There are no known limitations and workarounds for CoreRISCV_AXI4.