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MIV_RV32IMAF_L1_AHB v2.1 Release Notes

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 is the updated MIV_RV32IMAF_L1_AHB document, which adds ECC support for PolarFire and RTG4.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document. Created for MIV_RV32IMAF_L1_AHB v2.0.

Contents

3 MIV_RV32IMAF_L1_AHB v2.1 Release Notes

3.1 Overview

This release notes is included in the production release of MIV_RV32IMAF_L1_AHB v2.1. This document provides details about the features, enhancements, system requirements, supported families, implementations, known issues, and workarounds.

3.2 Features

MIV_RV32IMAF_L1_AHB features are:

- Designed for low power ASIC microcontroller and FPGA soft-core implementations.
- Integrated with 8Kbytes instructions cache and 8 Kbytes data cache.
- The Platform-Level Interrupt Controller (PLIC) can support up to 31 programmable interrupts with a single priority level.
- Supports the RISCV standard RV32IMAF ISA.
- Provides an On-Chip debug unit with a JTAG interface.
- Provides two external AHB interfaces for IO and memory.
- Supports Error-Correcting Code (ECC) caches on RTG4 and PolarFire.

3.3 Delivery Types

License is not required for MIV_RV32IMAF_L1_AHB. Complete RTL source code is provided for the core.

3.4 Supported Families

- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

3.5 Supported Tool Flows

MIV_RV32IMAF_L1_AHB requires Libero® System-on-Chip (SoC) software v11.8 or higher.

3.6 Installation Instructions

The MIV_RV32IMAF_L1_AHB CPZ file is installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature.When the CPZ file is installed in Libero, the core is configured, generated, and instantiated within SmartDesign, for inclusion in the Libero project.Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

3.7 Documentation

This release contains a copy of the MIV_RV32IMAF_L1_AHB *Handbook*. The handbook describes the core functionality and provides step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

3.8 Supported Test Environments

Testbench is not provided with MIV_RV32IMAF_L1_AHB.

The MIV_RV32IMAF_L1_AHB RTL can be used to simulate the processor executing a program using a standard Libero generated HDL testbench.

3.9 Resolved History

Table 1 lists the release history for MIV_RV32IMAF_L1_AHB.

Table 1 • **Release History**

Version	Date	Changes
2.1	May 2019	The following SARs were resolved in this version: • SAR103816: MIV_RV32IMAF_L1_AHB ModelSim reports bus mismatch warnings at the start of simulation. • SAR103165: MIV_RV32IMAF_L1_AHB has paths which are not radiated protected. • SAR103180: RTL Correction in Mi-V VHDL syntax • SAR105794: Add Simulation defines to core. • SAR105795: Enables ECC in MIV_RV32IMAF_L1_AHB • SAR105976: Resets in Handbook should be active low • SAR105978: AHB information to be added to Handbook • SAR105979: Adding additional text to memory map and debug spec to the core.
2.0	November 2017	First Production Release

3.10 Discontinued Features and Devices

SAR103180: Support for VHDL has been discontinued as Libero will create a VHDL wrapper for the Verilog code.

3.11 Known Limitations and Workarounds

3.11.1 Reset or Power Cycle the Target Hardware before each Debug Session

Presently, the debugger cannot effect a suitable MI-V RISC-V CPU/SoC reset, at the start of each debug session so one debug session may be impacted by what went previously – for example, a previous debug session leaves the CPU in an ISR, and a subsequent debug session does not behave as expected because of this. To remove this problem it is recommended that the target hardware or board is power cycled, or otherwise reset before each new debug session.