

RN0197

MIV_RV32IMA_L1_AXI V2.1 Release Notes



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Updated for MIV_RV32IMA_L1_AXI v2.1. Updated Discontinued Features and Devices and Known Limitations and Workarounds sections.

1.2 Revision 1.0

Revision 1.0 is the first publication of this document. Created for MIV_RV32IMA_L1_AXI v2.0.

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2 MIV_RV32IMA_L1_AXI v2.1 Release Notes

2.1 Overview

These release notes accompany the production release of MIV_RV32IMA_L1_AXI v2.1. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

MIV_RV32IMA_L1_AXI has the following features:

- Designed for low power ASIC microcontroller and FPGA soft-core implementations
- Integrated 8Kbytes instructions cache and 8 Kbytes data cache
- A Platform-Level Interrupt Controller (PLIC) can support up to 31 programmable interrupt with a single priority level
- Supports the RISC-V standard RV32IMA ISA
- On-Chip debug unit with a JTAG interface
- Two external interfaces for IO and memory

2.3 Delivery Types

No License is required to use MIV_RV32IMA_L1_AXI. Complete RTL source code is provided for the core.

2.4 Supported Families

- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

2.5 Supported Tool Flows

MIV_RV32IMA_L1_AXI v2.1 requires Libero® System-on-Chip (SoC) v11.8 or later.

2.6 Installation Instructions

The MIV_RV32IMA_L1_AXI CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the [Libero SoC Online Help](#) for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the *MIV_RV32IMA_L1_AXI Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the [Libero SoC Online Help](#) for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

<http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>.

2.8 Supported Test Environments

No testbench is provided with MIV_RV32IMA_L1_AXI.

The MIV_RV32IMA_L1_AXI RTL can be used to simulate the processor executing a program using a standard Libero generated HDL testbench.

2.9 Resolved History

Table 1 lists the resolved issue history for MIV_RV32IMA_L1_AXI releases.

Table 1 • Release History

Version	Date	Changes
2.0	March 2018	Initial release.
2.1	January 2019	<ul style="list-style-type: none"> Asynchronous reset issue fixed, SAR100845 Randomization feature added for simulation purposes Modifications to Handbook

2.10 Discontinued Features and Devices

There are no discontinued features and devices in this release of MIV_RV32IMA_L1_AXI.

2.11 Known Limitations and Workarounds

Recommendation to Reset/Power Cycle the Target Hardware before each Debug Session. For more information, refer to section 10.1 Reset/Power Cycle the Target Hardware before each Debug Session in HB0823: MIV_RV32IMA_L1_AXI V2.1 Handbook.