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Release Notes
CoreDDR_LiteAXI v2.0

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About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document. Created for CoreDDR_LiteAXI v2.0.

2 CoreDDR_LiteAXI v2.0 Release Notes

These release notes accompany the production release of CoreDDR_LiteAXI. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.1 Features

CoreDDR_LiteAXI supports the following features:

- AXI4 protocol
- 1:1 synchronous clock
- Interface data widths: 128, 256, and 512-bits
- 32 to 40-bit AXI address bus
- Single or burst transfers
- Only AXI4 increment transfers
- Maximum of 16-bit ID width

2.2 Delivery Types

CoreDDR_LiteAXI is licensed as register transfer level (RTL). Complete RTL source code is provided for the core.

2.3 Supported Families

- PolarFire®

2.4 Supported Tool Flows

CoreDDR_LiteAXI requires Libero® System-on-Chip (SoC) software v12.0 or later.

2.5 Installation Instructions

The CoreDDR_LiteAXI CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.6 Documentation

This release contains a copy of the *CoreDDR_LiteAXI Handbook*. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores

2.7 Supported Test Environments

User testbench is not provided with CoreDDR_LiteAXI.

2.8 Discontinued Features and Devices

There are no discontinued features in this release.

2.9 Known Limitations and Workarounds

1. FIXED and Wrap type burst transactions are not supported.
2. Data before address type transactions are not supported.