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CoreLNSQRT v2.0 Release Notes

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreLNSQRT v2.0.

Contents

3 CoreLNSQRT v2.0 Release Notes

3.1 Overview

These release notes accompany the production release of CoreLNSQRT v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

3.2 Key Features

The CoreLNSQRT provides the following features:

- Expanded hyperbolic function for wide input range (up to 64 bits)
- Selectable Sequential or pipelined architecture
- Square root and natural logarithm computation

3.3 Delivery Types

CoreLNSQRT is licensed with encrypted and plaintext RTL.

3.4 License

CoreLNSQRT clear RTL is license locked and the encrypted RTL is freely available.

3.4.1 Encrypted Version

Complete encrypted RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero software. The RTL code for the core is encrypted using the IP encryption (encryptP1735.pl) solution. Evaluation version will not be license locked and will be available for free.

3.4.2 RTL Version

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero software. The plaintext RTL code will be provided with this option. The License feature should be published for RTL core only.

3.5 Supported Families

- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

3.6 Supported Tool Flows

CoreLNSQRT v2.0 requires Libero® System-on-Chip (SoC) software v11.4 or later.

3.7 Installation Instructions

CoreLNSQRT is available for download in the Libero IP catalog through web repository. Once it is listed in the catalog, the core can be instantiated using the SmartDesign flow. For information on using SmartDesign to configure, connect, and generate cores, Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

After configuring and generating the core instance, the basic functionality can be simulated using the test-bench supplied with the CoreLNSQRT. The CoreLNSQRT can be instantiated as a component of a larger design.

3.8 Documentation

This release contains a copy of the *CoreLNSQRT Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

3.9 Supported Test Environments

The following test environments are supported:

- Verilog user testbench

3.10 Resolved History

Table 1, page 6 lists the release history for CoreLNSQRT.

Table 1 • **Release History**

Version	Date	Changes
2.0	August 2018	Initial Release.

3.11 Discontinued Features and Devices

There are no discontinued features for this release of CoreLNSQRT v2.0.

3.12 Known Limitations and Workarounds

No limitations are there.