

RN0208

CoreLNSQRT v2.0 Release Notes



a  **MICROCHIP** company



a  MICROCHIP company

Microsemi Headquarters

One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113

Outside the USA: +1 (949) 380-6100

Sales: +1 (949) 380-6136

Fax: +1 (949) 215-4996

Email: sales.support@microsemi.com

www.microsemi.com

©2018 Microsemi, a wholly owned subsidiary of Microchip Technology Inc. All rights reserved. Microsemi and the Microsemi logo are registered trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

About Microsemi

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at www.microsemi.com.

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreLNSQRT v2.0.

Contents

1	Revision History	3
1.1	Revision 1.0	3
2	CoreLNSQRT v2.0 Release Notes	5
2.1	Overview	5
2.2	Key Features	5
2.3	Delivery Types	5
2.4	License	5
2.4.1	Encrypted Version	5
2.4.2	RTL Version	5
2.5	Supported Families	5
2.6	Supported Tool Flows	5
2.7	Installation Instructions	5
2.8	Documentation	6
2.9	Supported Test Environments	6
2.10	Resolved History	6
2.11	Discontinued Features and Devices	6
2.12	Known Limitations and Workarounds	6

3 CoreLNSQRT v2.0 Release Notes

3.1 Overview

These release notes accompany the production release of CoreLNSQRT v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

3.2 Key Features

The CoreLNSQRT provides the following features:

- Expanded hyperbolic function for wide input range (up to 64 bits)
- Selectable Sequential or pipelined architecture
- Square root and natural logarithm computation

3.3 Delivery Types

CoreLNSQRT is licensed with encrypted and plaintext RTL.

3.4 License

CoreLNSQRT clear RTL is license locked and the encrypted RTL is freely available.

3.4.1 Encrypted Version

Complete encrypted RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero software. The RTL code for the core is encrypted using the IP encryption (encryptP1735.pl) solution. Evaluation version will not be license locked and will be available for free.

3.4.2 RTL Version

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero software. The plaintext RTL code will be provided with this option. The License feature should be published for RTL core only.

3.5 Supported Families

- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

3.6 Supported Tool Flows

CoreLNSQRT v2.0 requires Libero® System-on-Chip (SoC) software v11.4 or later.

3.7 Installation Instructions

CoreLNSQRT is available for download in the Libero IP catalog through web repository. Once it is listed in the catalog, the core can be instantiated using the SmartDesign flow. For information on using SmartDesign to configure, connect, and generate cores, Refer to the [Libero SoC Online Help](#) for further instructions on core installation, licensing, and general use.

After configuring and generating the core instance, the basic functionality can be simulated using the test-bench supplied with the CoreLNSQRT. The CoreLNSQRT can be instantiated as a component of a larger design.

3.8 Documentation

This release contains a copy of the *CoreLNSQRT Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

<http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>.

3.9 Supported Test Environments

The following test environments are supported:

- Verilog user testbench

3.10 Resolved History

Table 1, page 6 lists the release history for CoreLNSQRT.

Table 1 • Release History

Version	Date	Changes
2.0	August 2018	Initial Release.

3.11 Discontinued Features and Devices

There are no discontinued features for this release of CoreLNSQRT v2.0.

3.12 Known Limitations and Workarounds

No limitations are there.