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Release Notes
CoreAXI4DMAController v2.1

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Updated the document for CoreAXI4DMAController v2.1.
- Updated the following sections.
  - Delivery Types, page 6.
  - Supported Families, page 6.
  - Installation Instructions, page 6.
  - Documentation, page 7.
- Added Table 1, page 7 for SAR changes.

1.2 Revision 1.0

The first publication of this document. Created for CoreAXI4DMAController v2.0.

Contents

Tables

2 CoreAXI4DMAController v2.1

2.1 Overview

These release notes accompany the production release of CoreAXI4DMAController v2.1. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

CoreAXI4DMAController is a highly configurable core with the following features:

- AXI4-Lite slave control interface
- AXI4 master DMA interface
- AXI4-Stream slave interface to provide a bridge to AXI4 memory map
- Maximum transfer size of approximately 8 MB
- Maximum operating frequency of approximately 200 MHz
- Circular buffer support
- Scatter-gather support
- 2 internal 4 KB caches store & forward caches
- 1-4 interrupt outputs
- 4-32 internal descriptors
- External descriptor fetching support
- Fixed priority arbiter for DMA requests with configurable number of priority levels
- Configurable DMA bus width from 32- to 512-bit
- Prevents AXI4 transfers from crossing 4 KB boundaries

2.3 Delivery Types

CoreAXI4DMAController does not require a license. Complete RTL source code is provided for the core and testbenches.

2.4 Supported Families

CoreAXI4DMAController supports the following families:

- PolarFire® SoC
- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

2.5 Supported Tool Flows

- CoreAXI4DMAController requires Libero® System-on-Chip (SoC) software v12.0 or later.

2.6 Installation Instructions

The CoreAXI4DMAController CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. For more information, see the *Knowledge Based article*.

To know how to create SmartDesign project using the IP cores, refer to *Libero SoC documents page* and use the latest SmartDesign user guide.

2.7 Documentation

This release contains a copy of the *CoreAXI4DMAController Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC documents* for instructions on obtaining IP documentation.

For updates and additional information, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

The following test environments are supported:

- Verilog user testbench

2.9 Resolved Issues in the v2.1 Release

Table 1 • **Resolved Issues in the v2.1 Release**

SAR Number	Changes
111640	CoreAXI4DMAController hang issue when accessing register addresses in between the descriptor set.
107452	CoreAXI4DMAcontroller is shown in catalog for RTG4.
87996	PRIO_0_NUM_OF_BEATS min limit issue.
97934	TSTRB should be “AXI_DMA_DWIDTH/8”.
112271	Combinational loops when stream support is enabled.
113037	CoreAXI4DMAController query on “STRTDMAOP” behavior.
87912	Multiple chain DMA issue.
87913	Not getting TREADY in STREAM transaction.
85838	Not getting “invalid desc” bit set in the interrupt status.

2.10 Resolved Issues in the v2.0 Release

As this is the initial version, there were no SARs resolved in the v2.0 release.

2.11 Discontinued Features and Devices

There were no discontinued features and devices in the v2.1 release.

2.12 Known Limitations and Workarounds

There are no known limitations and workarounds.