HB0879

Handbook
CoreUSXGMII v2.0

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document. It is created for CoreUSXGMII v2.0.

2 Introduction

2.1 Overview

The CoreUSXGMII (Universal Serial Media Independent Interface) IP is used to carry single network port over a single SERDES between the MAC and the PHY for Multi-Gigabit technology at 1G/ 2.5G/ 5G/ 10G data rate.

2.2 Features

The following topics describes the various features of CoreUSXGMII.

2.2.1 Features Supported

- Convey Single network ports over an USXGMII MAC-PHY interface (USXGMII-S Only - USXGMII-Copper PHY: EDCS- 1150953)
- Supports operating speed rates of 1G/ 2.5G/ 5G/ 10G
- MAC side interface is 64-bit XGMII
- Operates System interface in full duplex mode only
- Provides a serial 10.3125 Gbps serial link on the transceiver side
- Provides 64-bit interface to Microsemi Transceiver operating in PCS 64B66B Clause 49
- Supports Clause 37 Auto-negotiation between MAC and PHY
- APB management interface for configuration / status

2.2.2 Features Not Supported

- Operating speed rates of 100M
- 32-bit XGMII interface on the MAC side
- Multiple network port over single SERDES (USXGMII-M)
- EEE (Clause 78)
- FEC (Clause 74)

2.3 Core Version

This handbook is for CoreUSXGMII version 2.0.

2.4 Supported Families

PolarFire®

2.5 Utilization and Performance

Table 1 • **Utilization and Performance**

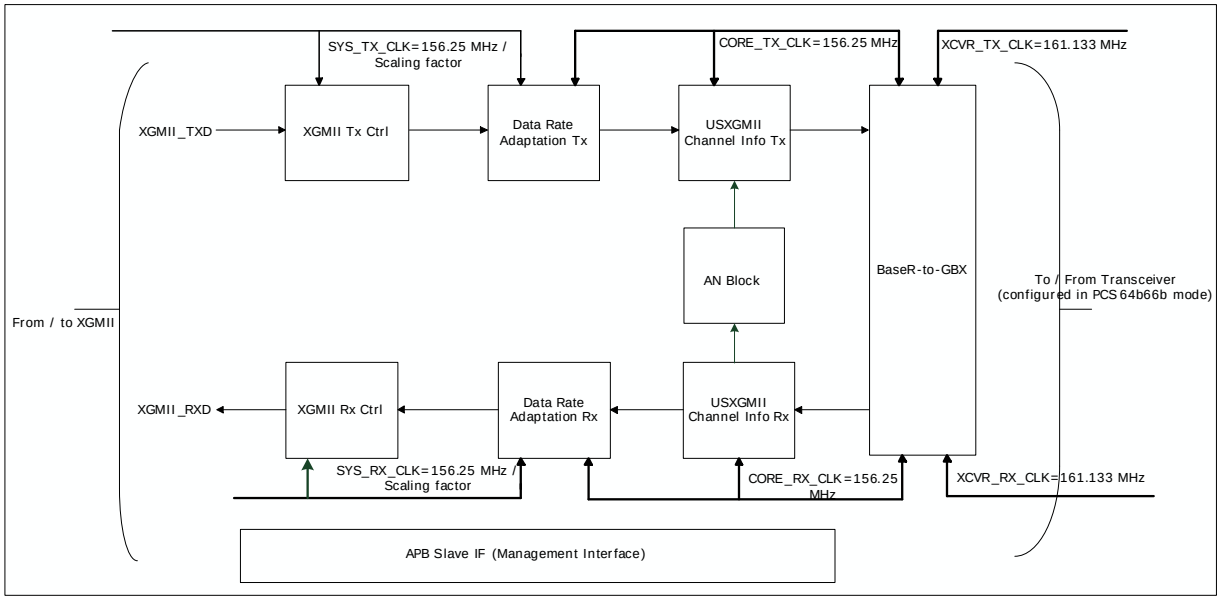
	Utilization (Logic Elements)					Performance (MHz)	
Device Family	**Sequential (DFF)**	**Combinatorial (4-LUT)**	**Total**	**%**	**RAM 1K20**	**CORE_TX_CLK**	**CORE_RX_CLK**
PolarFire (MPF500T)	6065	4165	10230	2.12	12	180	245

Note: The data in this table is achieved using typical synthesis and layout settings. Frequency (MHz) was set to 175 and the speed grade was -1.

3 Functional Description

The following figure describes the functionality of CoreUSXGMII:

Figure 1 • **CoreUSXGMII Block Diagram**



Note: Scaling factor is /10, /4, /2, /1 for 1G, 2.5G, 5G and 10G respectively.

Note: The clock description is provided in the Clocking, page 5 section.

3.1 XGMII Controller Interface

3.1.1 XGMII Interface

The XGMII interface connects the Reconciliation Sublayer (RS) with the IP and allows transferring information to/from as defined in Clause 46. The IP supports 64-bit wide data path interface only.

The XGMII Controller interface block interfaces with the Data rate adaptation block. This block contains the signals TXD (64-bits) (Transmit data), TXC (8-bits) (Transmit control), RXD (64-bits) (Receive data), and RXC (8-bits) (Receive control).

The XGMII Controller block works on SYS_TX_CLK and SYS_RX_CLK in the transmit and receive path respectively.

3.2 Data Rate Adaptation

3.2.1 Tx Path

In the Tx path, every 64-bit data from XGMII is replicated number of times based on the rate selected by the auto-negotiation (when enabled) with the link partner, else it is replicated based on the fixed configured rate.

Each 64-bit data is replicated 1/ 2/ 4/ 10 times for 10G/ 5G/ 2.5G/ 1G respectively.

For replication purpose, the SOP word byte is transmitted one time while in the remainder of the replicated words then it is replaced with 0xAA. This is compatible with the checks of the transmit PCS state machine that back-to-back SOPs are not allowed.

Each word of the preamble and payload is replicated 2/ 4/ 10 times for 5G/ 2.5G/ 1G respectively.

After the EOP is transmitted, the remaining 1/ 3/ 9 bytes are Idles. This is compatible with the checks of the Tx PCS state machine that back to back EOPs are not allowed.

Each idle byte is replicated 2/ 4/ 10 times. This ensures that the data rate in case of 2/ 4/ 10 does not exceed the frame rate.

All other sequence ordered sets and control sets are replicated 2/ 4/ 10 times for 5G/ 2.5G/ 1G respectively.

3.2.2 Rx Path

In the Rx path, the received SOP samples every 2nd, 4th, and 10th words to form RX data for 5G/ 2.5G/ 1G respectively. This is then passed to Receive XGMII control block and to the MAC subsequently.

The Data rate adaptation block works on CORE_TX_CLK and CORE_RX_CLK in the transmit and receive path respectively.

3.3 Auto-negotiation Mechanism

The CoreUSXGMII IP uses Clause 37 of IEEE 802.3 plus additional management control to select USXGMII mode. It conforms to EDCS-1150953 USXGMII- Copper PHY.

The PHY must provide a USXGMII enable control configuration through APB.

On Power Reset:

- USXGMII enable bit is de-asserted (logic “0”) and system interface on MAC and PHY must assume normal XGMII (Clause 46 / 49) operation for 10 Gbps.
- When USXGMII enable bit is enabled through APB, auto-neg operation should follow Clause 37-6 functions with the following modifications:
  - an_sync_status=fail changed to block_lock=false (restart Autoneg FSM), Autoneg FSM will restart whenever the link changes.
  - rudi(invalid) changed to idle received during an_restart, ability_detect, acknowledge_detect.
  - Link_timer changed to be configurable from 1 ms to 2 ms with difference of 0.1 ms.
  - Ability_match and acknowledge_match as per Clause 37-6
- Configuration words are transmitted during auto-negotiation on USXGMII interface in accordance to IEEE 802.3 Clause 37 auto-negotiation.
- During auto-negotiation, the packet data or idles on the XGMII interface of Tx MAC are discarded and not sent to Tx PCS.
- Instead, the auto-negotiation block drives the configuration words to Tx PCS on the XGMII interface.
- When auto-negotiation is completed, the Tx MAC output drives the Tx PCS using the XGMII interface.

Fault Handling:

- If Tx MAC transmits errors or link faults, the auto-negotiation is interrupted, and error / link fault information is passed to the XGMII interface from Tx MAC to Tx PCS.
- Other than data / idles all other control words are pass-through. For example, errors and link faults.

AN Restart:

- USXGMII Auto-negotiation is not re-started due to error/link fault conditions.
- Auto-negotiation is started due to network interface link changes or forced through software control.

AN Ordered Sets:

- The USXGMII implementation defines new ordered sets (IEEE 802.3ae Clause 46) to carry Auto-negotiation message besides the local and remote fault message.
- The UsxgmiiChannelInfo carries the auto-negotiation information. It is used to transfer configuration words (16-bits) between the MAC and the PHY.
- The configuration word is defined in Table 2 EDCS-1150953 USXGMII- Copper PHY specification.
- UsxgmiiChannelInfo uses 1.6 ms link timer. Any change in status of link requires PHY to re-signal UsxgmiiChannelInfo message until it is acknowledged by setting bit 14 (USXGMII_AN_ADV register) or for the duration of the link timer.

XGMII – AN message format:

The AN ordered set definition is in-line with Clause 46 definition of sequence ordered sets.

Table 2 • **Sequence Ordered Set**

TXC [3:0]	Lane0 [31:24]	Lane1 [23:16]	Lane2 [15:8]	Lane3 [7:0]
0x1	Character Control Code = 0x9C	Config [15:8]	Config [7:0]	Opcode for auto-neg = 0x03 (Cisco Specific)

3.4 BaseR_PHY

The BaseR_PHY converts the XGMII signaling to gearbox signaling and interfaces with Microchip's transceiver. Refer to Figure 2 and Figure 3 for the timing information.

The BaseR_PHY block works on CORE_TX_CLK/ CORE_RX_CLK and XCVR_TX_CK/ XCVR_RX_CLK in the transmit and receive path respectively. It contains the CDC FIFO to synchronize the signals for the clock rate change between the transceiver and the IP BaseR_PHY block.

3.5 Management Interface

The CoreUSXGMII registers are accessed through the APB interface. The APB slave interface is used to read and write the control and status registers of the IP.

The auto - negotiation function is managed through the APB slave interface.

3.6 Transceiver Interface

The Transceiver operates in the 64-bit PCS mode with scrambler enabled.

The Transceiver's 64B66B performs PCS operation as per the Clause 49. Also, the scrambler is enabled.

3.7 Clocking

Refer to Figure 1 for information on the clocking scheme used in the IP.

Table 3 • **IP Clocking**

Clock Name	Description
XCVR_TX_CLK, XCVR_RX_CLK	Transceiver transmit / receive clock to the fabric 64-bit @161.133 MHz.
CORE_TX_CLK, CORE_RX_CLK	Core transmit / receive clock 156.25 MHz @ 64-bit interface, transmit / receive clock is derived from the transceiver transmit/receive clock through CCC block.
SYS_TX_CLK, SYS_RX_CLK	System side (MAC-side clock) transmit / receive clock. It is based on the operating speed. 156.25 MHz/scaling factor Where Scaling factor = /10, /4, /2, and /1 for 1G, 2.5G, 5G, and 10G respectively.

3.7.1 Core Clocking

The core transmit clock must be derived from the transceiver transmit clock. The frequency for 64-bit interface is 156.25 MHz.

The core receive clock must be derived from the transceiver receive clock. The frequency for 64-bit interface is 156.25 MHz.

Note: The reference clock to the CCC's are driven by the transceiver Tx/Rx clock (XCVR_TX_CLK/ XCVR_RX_CLK) accordingly.

3.7.2 System-side (MAC) Clocking

For the 1G/ 2.5G/ 5G/ 10G Ethernet use, the clocks on the XGMII interface are scaled at the design level by using Clock Conditioning blocks (CCC's) to their respective data rates that is /10, /4, /2, and /1 respectively.

The reference clock to the CCC's are driven by the transceiver Tx/Rx clock (XCVR_TX_CLK/ XCVR_RX_CLK) accordingly.

3.7.3 Transceiver Clocking

The transceiver provides the transmit clock (XCVR_TX_CLK) to the fabric. The frequency for 64-bit interface is 161.133 MHz.

The transceiver provides the receive clock (XCVR_RX_CLK) to the fabric. The frequency for 64-bit interface is 161.133 MHz.

The transceiver clocks are used to generate the CORE_TX_CLK / CORE_RX_CLK and SYS_TX_CLK/ SYS_RX_CLK using Clock Conditioning blocks (CCC's) at the design level (external to the IP).

Refer to Figure 7 USXGMII System-level clocking.

4 Register Map and Descriptions

The following registers are accessed through the APB slave interface.

The register block contains the management registers specified in IEEE 802.3, Clause 37 – Control, Status, Auto Negotiation Advertisement, and Link Partner Ability.

Table 4 • **Register Map**

Register	Offset Address	Default Value (hex)
USXGMII_CONTROL_REG	0x00	0000_0601
USXGMII_STATUS_REG	0x04	0000_0088
USXGMII_AN_ADV	0x08	0000_1601
USXGMII_AN_LP_ADV	0x0C	0000_1600
USXGMII_LINK_TIMER	0x10	000F_C000

Table 5 • **Register Details**

Address	Register Name	Description		Type	Default
0x00	USXGMII_CONTROL_REG	**Control**			
		Bit [0]	USXGMII Mode Enable 0 – 10GBaseR mode 1 – USXGMII mode	R/W	1
		Bit [1]	USXGMII AN Enable 0 – Disables USXGMII Auto-Negotiation and the operating speed is configured manually. 1 – Enables USXGMII Auto-negotiation and automatically configures the operating speed based on the abilities advertised by the other link partner during Auto-negotiation. **Note:** This bit is used when bit [0] (That is USXGMII Mode enable Bit [0]) is set to 1.	R/W	0
		Bit [4:2]	Reserved	-	0
		Bit [5]	Restart Auto-negotiation The bit is cleared by hardware when the AN is restarted. This action is only available when Auto-Negotiation has been enabled.	R/W, SC	0
		Bit [6]	Loopback Setting This bit causes the transmit output of the CoreUSXGMII to be connected to the receive inputs. Clearing this bit result in normal operation.	R/W	0

Table 5 • **Register Details**

Address	Register Name	Description		Type	Default
		Bit [7]	PHY Reset Setting this bit causes the Data Rate Adaptation and Auto-Negotiation sub-modules in the CoreUSXGMII core to be reset. This bit is self-clearing.	R/W, SC	0
		Bit [8]	Soft Reset This is active high reset. It resets the functional modules within the CoreUSXGMII. The register values remain intact during the soft reset.	R/W	0
		Bit [11:9]	USXGMII_SPEED_CFG It is the operating speed in USXGMII mode and when USXGMII AN Enable bit [1] is set to 0. 3'b000: Reserved 3'b001: Reserved 3'b010: 1G 3'b011: 10G 3'b100: 2.5G 3'b101: 5G 3'b110: Reserved 3'b111: Reserved **Note:** This is used when the USXGMII AN Enable is set to 0.	R/W	3'b011
		Bit [12]	Shortcut Link Timer Set this bit 1 to reduce the value of Go Link Timer and Sync. Status Fail Timer to 64 clock pulse. This reduces the simulation time needed to time the Link Timer. Clear it for normal operation. In normal operation, the value of Go Link Timer is set using the AN Link Timer register (USXGMII_LINK_TIMER).	R/W	0
		Bit [31:13]	Reserved	-	0
0x08	USXGMII_AN_ADV	**AN Advertisement**			
		Bit [0]	Set to 1	R/W	1
		Bit [6:1]	Reserved	-	0
		Bit [7]	EEE Clock Stop capability Indicates whether or not Energy Efficient Ethernet (EEE) clock stop is supported. 0 – Not supported 1 – Supported **Note:** The IP CoreUSXGMII core does not support EEE.	R/W	0

Table 5 • **Register Details**

Address	Register Name	Description		Type	Default
		Bit [8]	EEE capability Indicates whether or not EEE is supported. 0 – Not supported 1 – Supported **Note:** The IP CoreUSXGMII core does not support EEE.	R/W	0
		Bit [11:9]	Speed Selection (SPEED_O) 3'b000: Reserved (10M) 3'b001: Reserved (100M) 3'b010: 1G 3'b011: 10G 3'b100: 2.5G 3'b101: 5G 3'b110: Reserved 3'b111: Reserved	R/W	3'b011
		Bit [12]	Duplex Indicates the duplex mode. 0 – Half duplex 1 – Full duplex **Note:** Only Full duplex supported	R/W	1
		Bit [13]	Reserved	-	0
		Bit [14]	AN Acknowledge 1 – Indicates that the device has received three consecutive matching ability values from its link partner.	R/W	0
		Bit [15]	Link Indicates the link status. 0 – Link down 1 – Link up	R/W	0
		Bit [31:16]	Reserved		
0x04	USXGMII_STATUS_REG	**Status**			
		Bit [1:0]	Reserved	-	0
		Bit [2]	Link Status indicates link status for USXGMII at all speeds. 1 – Indicates that a valid link has been established between the CoreUSXGMII and the PHY. 0 – No valid link has been established.	R/O	0
		Bit [3]	AN Ability 1 – Indicates that the CoreUSXGMII has the ability to perform Auto-negotiation. 0 – Indicates that the CoreUSXGMII does not have the ability to perform Auto-negotiation. **Note:** USXGMII IP has the AN ability hence the bit is always set.	R/O	1
		Bit [4]	Reserved	-	0

Table 5 • **Register Details**

Address	Register Name	Description		Type	Default
		Bit [5]	AN Complete 1 – Indicates that the auto-negotiation is completed.	R/O	0
		Bit [9:6]	AN FSM State 4'b0001: Disable Link ok 4'b0010: AN Enable 4'b0011: Restart 4'b0100: Ability Detect 4'b0101: Acknowledge Detect 4'b0110: NP WAIT 4'b0111: Complete Ack 4'b1000: Idle Detect 4'b1001: Link Ok **Note:** On power-on or on reset the AN FSM moves to AN ENABLE state.	R/O	4'b0010
		Bit [31:10]	Reserved	-	0
0x0C	USXGMII_AN_LP_ADV	**AN Link Partner Base Page Ability**			
		Bit [6:0]	Reserved	-	0
		Bit [7]	EEE Clock Stop capability Indicates whether or not Energy Efficient Ethernet (EEE) clock stop is supported 0 – Not supported 1 – Supported **Note:** The IP CoreUSXGMII core does not support EEE.	R/O	0
		Bit [8]	EEE capability Indicates whether or not EEE is supported. 0 – Not supported 1 – Supported **Note:** The IP CoreUSXGMII core does not support EEE.	R/O	0
		Bit [11:9]	Speed Selection (SPEED_O) 3'b000: Reserved (10M) 3'b001: Reserved (100M) 3'b010: 1G 3'b011: 10G 3'b100: 2.5G 3'b101: 5G 3'b110: Reserved 3'b111: Reserved	R/O	3'b011
		Bit [12]	Duplex Indicates the duplex mode. 0 – Half duplex 1 – Full duplex	R/O	1
		Bit [13]	Reserved	-	-
		Bit [14]	Acknowledge 1 – Indicates that the device has received three consecutive matching ability values from its link partner.	R/O	0

Table 5 • **Register Details**

Address	Register Name	Description		Type	Default
		Bit [15]	Link Indicates the link status. 0 – Link down 1 – Link up	R/O	0
		Bit [31:16]	Reserved	-	-
0x10	USXGMII_LINK_TIMER	**Auto-negotiation Link Timer**			
		Bit [13:0]	Reserved	-	0
		Bit [19:14]	Sets the link timer value in bit [19:14] from 1 ms to 2 ms in 0.1 ms steps. The Link timer value must be set so that it matches with the link timer value of the external NBASE-T PHY. Reset value sets the timer value to 1.6 ms.	R/W	1F
		Bit [31:20]	Reserved.	-	-

5 Interface

CoreUSXGMII has the following three interfaces:

APB Slave interface

An APB slave interface is used to provide access to the configuration and status registers in the CoreUSXGMII IP.

Transceiver Interface

The Gearbox interface of the CoreUSXGMII IP is connected to the transceiver interface in 64-bit mode with the transceiver operating in internal 64b66b PCS mode with scrambler enabled.

XGMII Interface

The IP provides the XGMII interface to connect to the Reconciliation Sublayer (RS) (as defined in Clause 46). The IP supports 64-bit wide data path interface only.

5.1 Parameters

There are no parameters required for the CoreUSXGMII IP.

5.2 Ports

The following table describes the input/output ports:

Table 6 • **Input / Output Signals**

Signal	Input / Output	Port width, bits	Description
Clocks and Resets			
SYS_TXCLK	Input	1	System-side (MAC) Transmit clock The clock is derived clock from the transceiver receive clock and is based on the operating speed. Example: For 10G – 156.25 MHz For 5G – 156.25/ 2 MHz = 78.125 MHz For 2.5G – 156.25/ 4 MHz = 39.0625 MHz For 1G – 156.25/ 10 MHz = 15.625 MHz
SYS_RXCLK	Input	1	System-side (MAC) Receive clock The clock is derived clock from the transceiver receive clock and is based on the operating speed. Example: For 10G – 156.25 MHz For 5G – 156.25/ 2 MHz = 78.125 MHz For 2.5G – 156.25/ 4 MHz = 39.0625 MHz For 1G – 156.25/ 10 MHz = 15.625 MHz
CORE_TXCLK	Input	1	Core Transmit clock (156.25 MHz); The CORE_TXCLK is the derived clock from the transceiver transmit clock
CORE_RXCLK	Input	1	Core Receive clock (156.25 MHz); The CORE_RXCLK is the derived clock from the transceiver receive clock.
XCVR_TX_CLK	Input	1	Transceiver Transmit clock to the fabric. The clock is 161.133 MHz.

Table 6 • **Input / Output Signals**

Signal	Input / Output	Port width, bits	Description
XCVR_RX_CLK	Input	1	Transceiver Receive clock to the fabric. The clock is 161.133 MHz.
RESETN	Input	1	Active low asynchronous reset This reset will be synchronized to the respective clock domains internally to the IP core.
XGMII Interface			
XGMII_TXD	Input	64	Transmitter Data
XGMII_TXC	Input	8	Transmitter Control
XGMII_RXD	Output	64	Receiver Data
XGMII_RXC	Output	8	Receiver Control
APB Slave Interface			
PCLK	Input	1	APB clock
PRESETN	Input	1	Active low asynchronous reset
PWRITE	Input	1	APB write/read enable, active high
PADDR	Input	16	APB address
PSEL	Input	1	APB select
PENABLE	Input	1	APB enable
PWDATA	Input	32	APB data input
PRDATA	Output	32	APB read data output
PREADY	Output	1	Ready. The Slave uses this signal to extend an APB transfer.
PSLVERR	Output	1	This signal indicates a transfer failure.
Transceiver Interface			
O_PMA49_TX_SOS	Output	1	Start-of-sequence pulse for a super frame, the length of which varies with the mode.
O_PMA49_TX_HDR	Output	4	Sync header corresponding to different encoding types.
O_PMA49_TX_DATA	Output	64	Input encoded data from CoreUSXGMII core IP to transceiver.
O_PMA49_TX_BYPASS_DATA	Output	1	Reserved – tie low
I_PMA49_RX_LOCK	Input	1	Receive sync lock 0 - Indicates that the sync header boundary is not locked. 1 - Indicates that the sync lock is achieved.
I_PMA49_RX_SOS	Input	1	Start-of-sequence pulse for a super frame, the length of which varies based on the mode. High output indicates start of sequence.
I_PMA49_RX_DATA_VAL	Input	1	Valid when there is data on RX_DATA.
I_PMA49_RX_DATA	Input	64	Receive encoded data from 64b66b to the fabric. The Bit 63 arrives first in the serial data.
I_PMA49_RX_HDR_VAL	Input	1	Enable for header data.

Table 6 • **Input / Output Signals**

Signal	Input / Output	Port width, bits	Description
I_PMA49_RX_HDR	Input	4	Sync header corresponding to different encoding types.
I_PMA49_RX_IDLE	Input	1	Receive electrical-idle detection flag. LANE#_Rx_IDLE peak detector logic is only valid for a limited minimum density of transitions on the Rx data and not to be used in applications above 6 Gbps.
I_PMA49_RX_READY	Input	1	Rises asserted or set when the CDR is phase-locked to the incoming data transitions and the de-serializer is powered-up. If there is no incoming data to the CDR then the RX_READY is low. The primary purpose of this pin is communicating to fabric that the CDR is locked to serial input data and is producing valid clocking.
Miscellaneous Signals			
USXGMII_SPEED	Output	3	Indicates the USXGMII operating speed. 3’b000: Reserved (10M) 3’b001: Reserved (100M) 3’b010: 1G 3’b011: 10G 3’b100: 2.5G 3’b101: 5G 3’b110: Reserved 3’b111: Reserved

6 Timing Diagrams

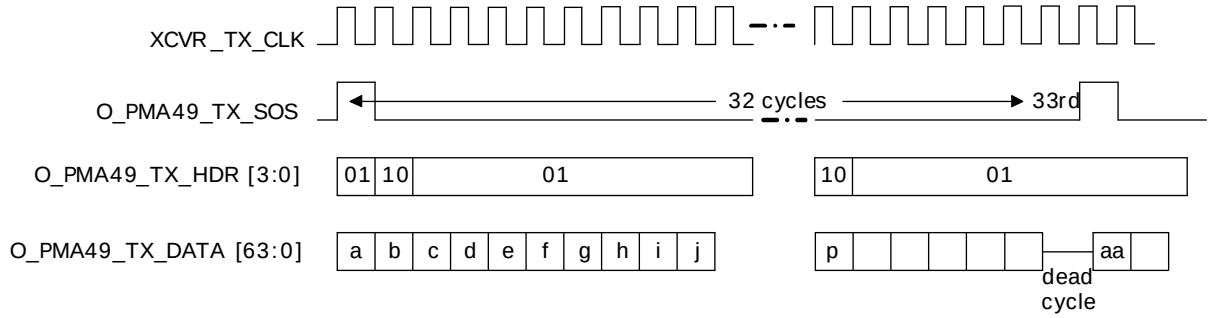
6.1 XGMII Interface Timings

The IP complies to the XGMII interface timings as defined in IEEE Clause 46.

6.2 Transceiver Interface

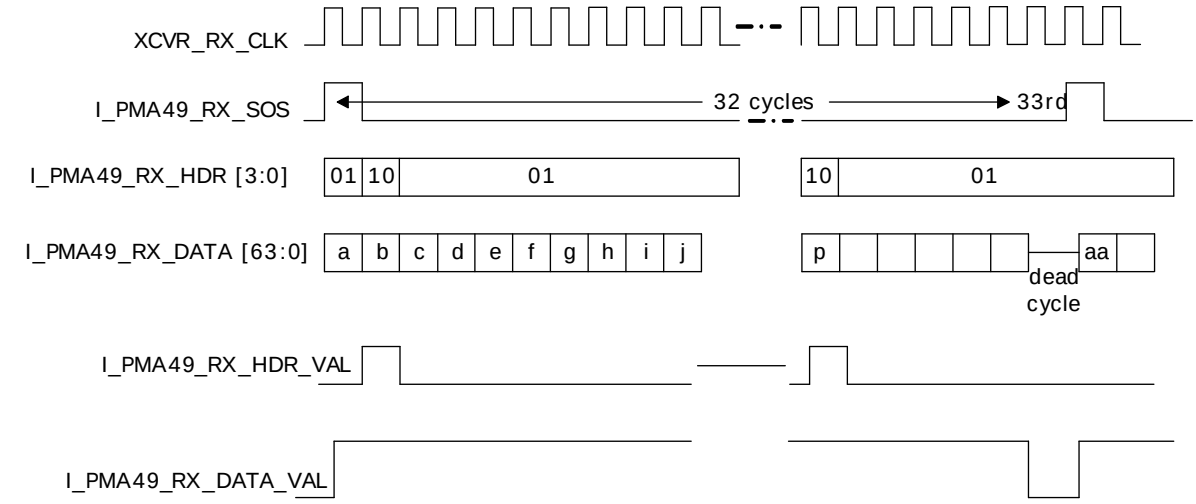
The following timing diagram shows the behavior of TXD and TXC frame transmission:

Figure 2 • **64B66B Transmit Sequence for the 64-Bit Interface**



The following timing diagram shows the behavior of RXD and RXC frame reception:

Figure 3 • **64B66B Receive Sequence for the 64-Bit Interface**



7 Tool Flow

7.1 License

CoreUSXGMII is licensed with evaluation and obfuscated RTL.

7.1.1 Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign.

Simulation, Synthesis, and Layout can be performed with Libero software. The RTL code for the core is obfuscated using the IP encryption (encryptP1735.pl) solution.

7.1.2 Evaluation

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign.

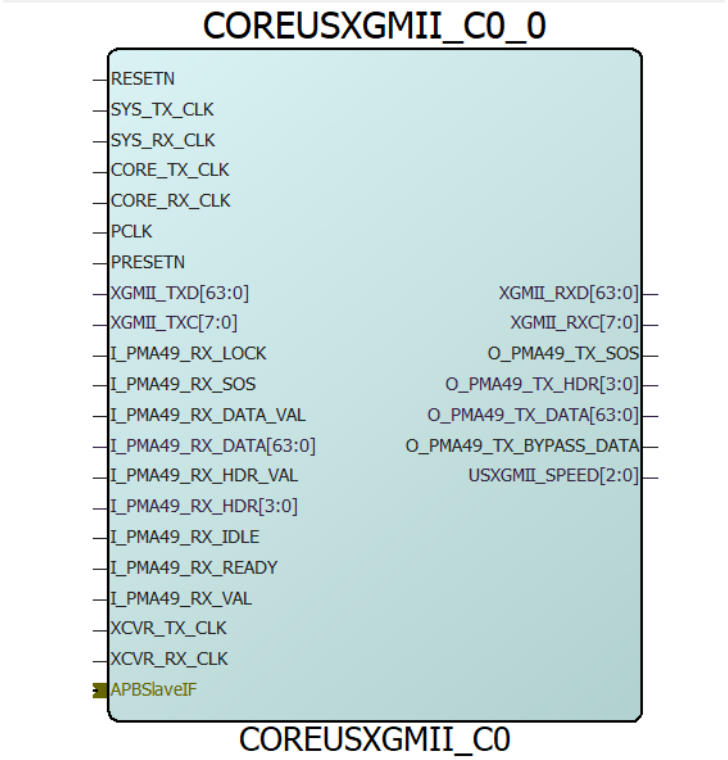
Simulation, Synthesis, and Layout can be performed with Libero software. The RTL code for the core is obfuscated using the IP encryption (encryptP1735.pl) solution and has a self-destruct feature which will stop functioning after 4 hours at 10 Gbps data rate using 64bit at 156.25 MHz.

7.2 SmartDesign

CoreUSXGMII is pre-installed in the SmartDesign IP Deployment design environment. Figure 4 shows an example of instantiated CoreUSXGMII IP. The core can be configured using the configuration window in the SmartDesign, as shown in Figure 5.

For more information on using the SmartDesign to instantiate and generate cores, refer Using DirectCore in Libero® SoC User Guide.

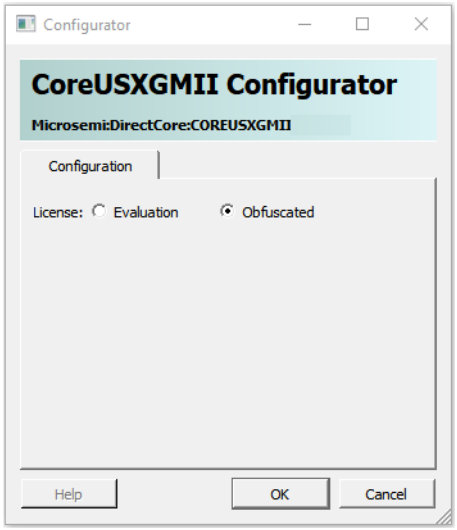
Figure 4 • **SmartDesign CoreUSXGMII Instance View**



7.3 Configuring CoreUSXGMII in SmartDesign

The core is configured using the configuration GUI within SmartDesign, as shown in following figure:

Figure 5 • **Configuring CoreUSXGMII in SmartDesign**



7.4 Simulation Flows

There is no User Testbench provided with this release of the IP.

7.5 Synthesis in Libero

Click **Synthesis** icon in Libero SoC. The Synthesis window displays the Synplify® project. Set Synplify to use the Verilog 2001 standard, if Verilog is being used. To run the synthesis, click **Run**.

7.6 Place-and-Route in Libero

Click **Layout** icon in the Libero software to invoke the Designer. CoreUSXGMII does not require any special place-and-route settings.

8 Testbench

There is no User Test bench provided with this release of the IP.

9 System Integration

This section provides hint to ease the integration of CoreUSXGMII.

Figure 6 • **CoreUSXGMII System Integration**

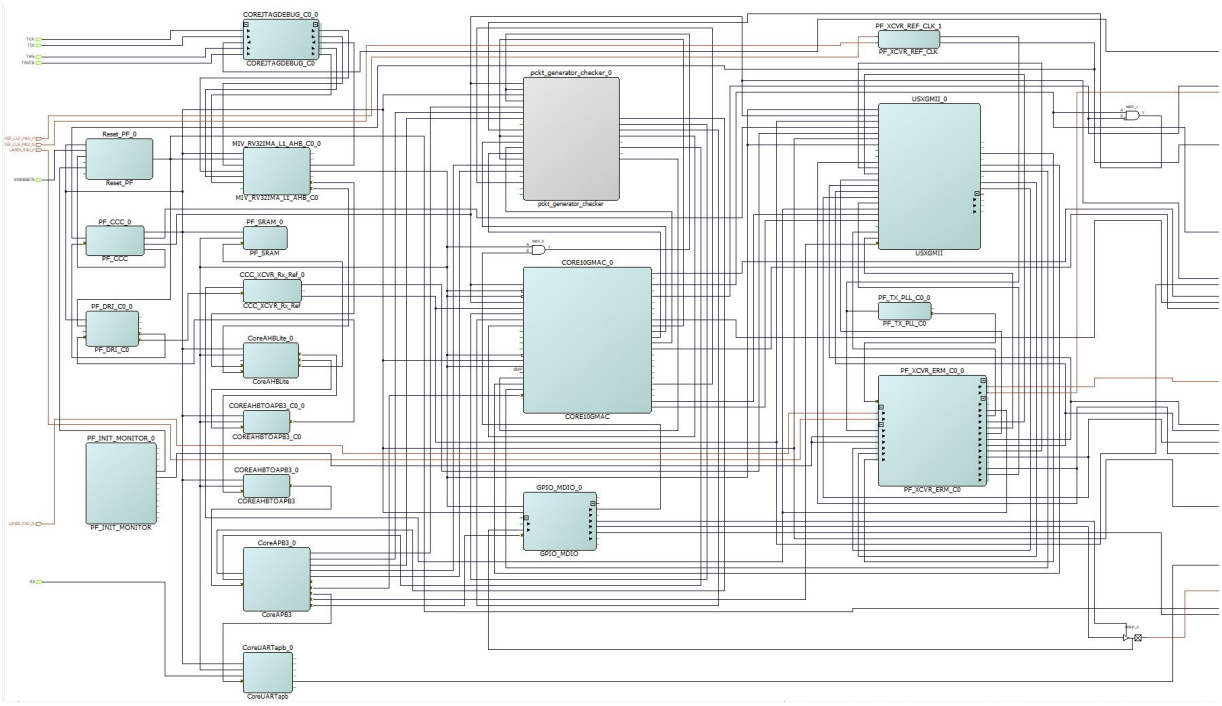


Figure 7 • **CoreUSXGMII System-level Clocking Diagram**

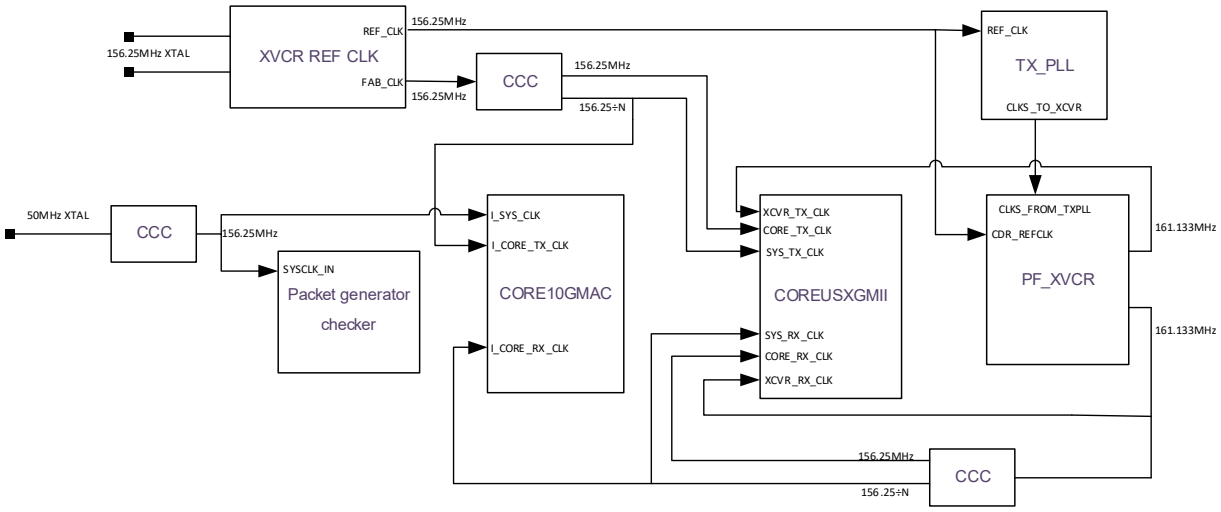
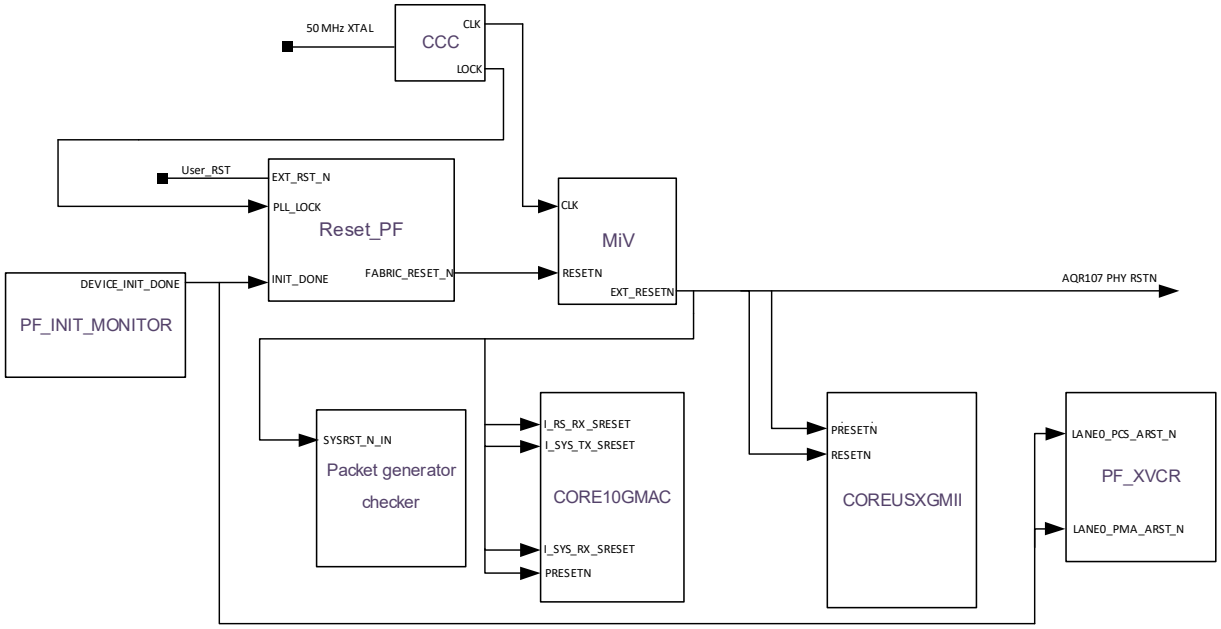


Figure 8 • **CoreUSXGMII System-level Reset Structure**



Note: N indicates the scaling factor and depends on the speed data rate. The scaling factor N = 10, 4, 2, and 1 for 1G, 2.5G, 5G and 10G respectively. Refer to Table 7, page 20.

Table 7 • **Clocking Speed Data Rate**

Speed Data Rate	N (Scaling Factor)
10G	1
5G	2
2.5G	4
1G	10

10 Ordering Codes

CoreUSXGMII can be ordered through your local Microsemi sales representative. It should be ordered using the following number scheme: CoreUSXGMII-XX, where XX is listed the following table.

Table 8 • **Core ordering Codes**

XX	Description
OM	Obfuscated RTL multi-use license