RN0198

CoreQSGMII v2.0 Release Notes

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

51300198-1/4.18

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document. Created for CoreQSGMII v2.0.

Contents

2 CoreQSGMII v2.0 Release Notes

2.1 Overview

These release notes accompany the production release of CoreQSGMII v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

CoreQSGMII implements the following features:

- Compliant with Cisco Systems' proprietary QSGMII Specification, Revision 1.2
- Four independent 10/100/1000 Mbps ports
- Implement SGMII adaptation for 10/100/1000 operation of each port
- Implements 8b/10b encoder/decoder and PCS Transmit function for each port in accordance with IEEE Standard 802.3 Clause 36 modified to support QSGMII
- K28.5 swapper on Port 0 in the transmit path as per the QSGMII specification
- Comma alignment and K28.1 swapper on Port 0 in the receive path as per the QSGMII specification
- Supports auto-negotiation functionality per port
- Supports management interface for register configuration through MDIO interface
- The SerDes interface on the QSGMII IP is configured for 40-bit, single lane operating at 5.0 Gbps speed with fabric interface running at 125MHz

2.3 Delivery Types

- Obfuscated
- Evaluation

The Evaluation version is freely available and the Obfuscated version will be license locked at the time of packaging.

2.4 Supported Families

- PolarFire®

2.5 Supported Tool Flows

CoreQSGMII v2.0 requires Libero SoC PolarFire.

2.6 Installation Instructions

The CoreQSGMII CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the *CoreQSGMII Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

User testbench is provided with CoreQSGMII.

2.9 Resolved History

Table 1 lists the release history for CoreQSGMII.

Table 1 • **Release History**

Version	Date	Changes
2.0	April 2018	Initial release.

2.10 Known Limitations and Workarounds

There are no known limitations and workarounds for CoreQSGMII. CoreQSGMII is tested for 1G mode only.