CoreUART v5.6 Release Notes

This is the production release for the CoreUART IP core. These release notes describe the features and enhancements for CoreUART IP v5.6. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

CoreUART is a highly configurable core and has the following features:

- Asynchronous mode to interface with industry standard UART
- Optional Transmit and Receive FIFOs

Delivery Types

CoreUART is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero® System-on-Chip (SoC). The RTL code for the core is obfuscated.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3E
- ProASIC3L
- SmartFusion®
- SmartFusion2
- Fusion
- ProASIC PLUS®
- Axcelerator®
- RTAX-S
- SX-A
- RTSX-S
- IGLOO®2
- RTG4™
- PolarFire

Supported Tool Flows

This version of the core requires Libero v8.6 or later.

Installation Instructions

For RTL and Obfuscated versions of the core, the FLEXlm license must be installed before the core can be exported. Refer to the *Libero SoC Online Help* for further instructions regarding core installation and licensing.

Documentation

This release contains a copy of the *CoreUART Handbook*. The handbook describes the core functionality and gives implementation suggestions.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages at www.microsemi.com.

Supported Test Environments

The following test environments are supported for CoreUART:

- Verilog user testbench
- VHDL user testbench

New Features and Devices

The following new features and devices are included in the v5.6 release:

- Support for PolarFire added

Release History

Table 1 provides the release history of CoreUART.

Table 1 • **Release History of CoreUART**

Version	Date	Changes
5.6	March 2016	Added support for PolarFire.
5.5	August 2015	Updated handbook for v5.5 core release.
5.4	November 2014	Added support for RTG4.
5.3	February 2014	Added support for IGLOO2 devices.
5.2	September 2012	Added support for SmartFusion2 devices.
5.1	March 2012	A programmable option for fractional baud value was added to give extra precision.
4.2	October 2010	Maintenance release. Fixed performance SAR 20741, usability SAR 18238, and other minor changes.
4.1	July 2009	Maintenance release. Fixed major SAR No. 19041, and others (see Table 5).
4.0	February 2009	Widened baud value Added Framing error functionality
3.1	February 2007	Added support for IGLOO and Fusion devices Removed synchronous mode
3.0	June 2005	Added TX and RX FIFOs
2.1	February 2005	Added support for ProASIC3 devices
2.0	December 2003	Initial version of the core

Resolved Issues in the v5.6 Release

No additional SARs were resolved in the v5.6 release.

Resolved Issues in the v5.5 Release

Table 2 lists the SARs that were resolved in the CoreUART v5.5 release.

Table 2 • **Resolved Issues in the CoreUART v5.5 Release**

SAR No.	Description
66586	Baudval zero is not supported, to be updated in the handbook.

Resolved Issues in the v5.4 Release

No additional SARs were resolved in the v5.4 release.

Resolved Issues in the v5.3 Release

No additional SARs were resolved in the v5.3 release.

Resolved Issues in the v5.2 Release

No additional SARs were resolved in the v5.2 release.

Resolved Issues in the v5.1 Release

Table 3 lists the software action requests (SARs) that were resolved in the CoreUART v5.1 release.

Table 3 • **Resolved Issues in the CoreUART v5.1 Release**

SAR No.	Description
37390	Addition of the fractional baud value feature

Resolved Issues in the v4.2 Release

Table 4 lists the software action requests (SARs) that were resolved in the CoreUART v4.2 release.

Table 4 • **Resolved Issues in the CoreUART v4.2 Release**

SAR No.	Description
18238	CoreUART and CoreUARTapb can be instantiated in the same design without module name conflicts.
20741	Performance improvement for continuous transmission when TX FIFO enabled; there is no longer a 3-bit delay between byte transmissions.

Resolved Issues in the v4.1 Release

Table 5 lists the software action requests (SARs) that were resolved in the CoreUART v4.1 release.

Table 5 • **Resolved Issues in the CoreUART v4.1 Release**

SAR No.	Description
19342	Framing error is cleared on byte receive in FIFO mode.
19282	FIFO overflow error has been fixed.
19041	RXRDY in FIFO mode fixed.

Resolved Issues in the v4.0 Release

Table 6 lists the software action requests (SARs) that were resolved in the CoreUART v4.0 release.

Table 6 • **Resolved Issues in the CoreUART v4.0 Release**

SAR No.	Description
12177	Added URL resource links to CoreUART package.
11848	Core naming rules fixed.
11849	Device name fixed for SX-A in handbook.
11928	Fixed FIFO error during synthesis for IGLOO family.
12126	Fixed RXRDY assertion bug, whereby RXRDY is asserted when RX stays low for an entire byte. This is fixed by adding a FRAMING_ERR signal to indicate a missing stop bit.

Resolved Issues in the v3.1 Release

Table 7 lists the software action requests (SARs) that were resolved in previous releases of CoreUART.

Table 7 • **Resolved Issues in the CoreUART (previous releases)**

SAR No.	Description
59866	Changed the RECEIVED_FULL signal name to RXRDY in order match its functionality.
54173	Added explanation for the default parameters in the handbook.
61666	Modified the FIFO flags to match the programmed FIFO level signals.

Known Issues and Workarounds

There are no known limitations or workarounds in the CoreUART v5.6 release.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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