CoreSF2Reset v3.0

Handbook

Microsemi

Table of Contents

Introduction

Core Overview

CoreSF2Reset handles sequencing of reset signals in a SmartFusion®2 device. This core deals with the resets related to the peripheral blocks including the microcontroller subsystem double data rate (MDDR) controller, fabric DDR (FDDR) controller, and high speed serial interface blocks (SERDESIF).

Figure 1 shows an overview of how CoreSF2Reset is connected to other components.

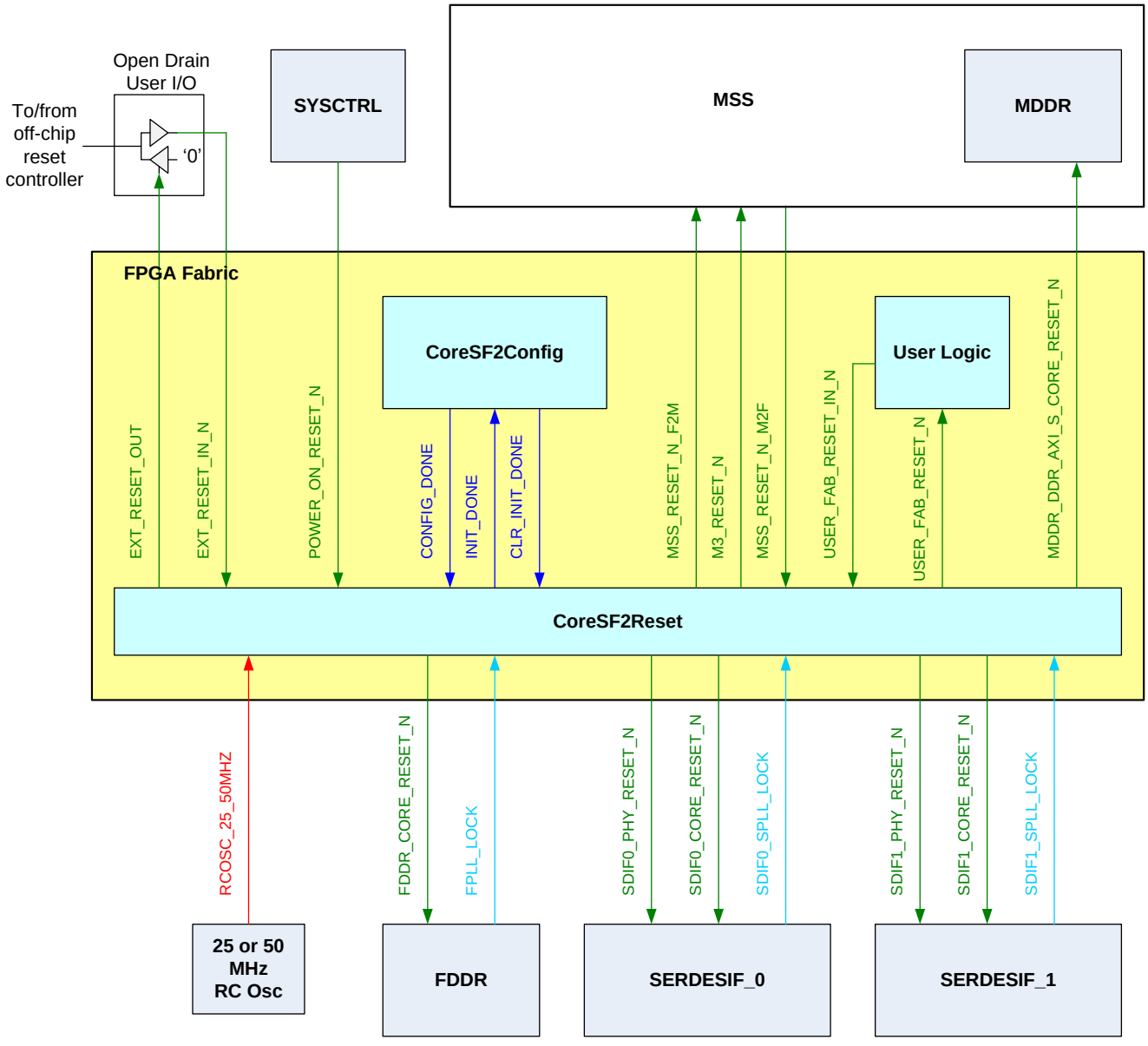

Figure 1 CoreSF2Reset Connections

Key Features

- Sequences reset signals in a SmartFusion2 device

Supported Microsemi® FPGA Families

CoreSF2Reset supports the following family:

- SmartFusion2

Core Version

This handbook supports CoreSF2Reset v3.0.

Interface Description

Ports

The ports present on CoreSF2Reset are listed in Table 1.

Table 1 CoreSF2Reset Ports

Port Name	Type	Description
RCOSC_25_50MHZ	Input	25 or 50 MHz clock from RC oscillator.
POWER_ON_RESET_N	Input	Active low power on reset from system controller.
EXT_RESET_IN_N	Input	Active low reset input from an external source.
EXT_RESET_OUT	Output	Output suitable for driving an external reset pin.
MSS_RESET_N_F2M	Output	Active low reset signal to MSS. Resets MSS.
M3_RESET_N	Output	Active low reset signal to MSS. Resets Cortex-M3 processor.
MSS_RESET_N_M2F	Input	Active low reset from MSS.
MDDR_DDR_AXI_S_CORE_RESET_N	Output	Active low reset to MSS. Resets MDDR AXI interface.
INIT_DONE	Output	Indicates the completion of the Initialization. Asserted when peripheral configuration and reset sequencing are completed. Normally, connected to CoreSF2Config. It can also be used as an interrupt to MSS.
CLR_INIT_DONE	Input	When asserted, the INIT_DONE output negates. Normally, connects to CoreSF2Config.
CONFIG_DONE	Input	Indicates the completion of the configuration from CoreSF2Config.
USER_FAB_RESET_IN_N	Input	Active low reset input from user logic in fabric. Optional. ANDed internally with EXT_RESET_IN_N.
USER_FAB_RESET_N	Output	Active low reset to user logic in fabric
FPLL_LOCK	Input	Indicates phase-locked loop (PLL) lock from FDDR block.
FDDR_CORE_RESET_N	Output	Active low reset to FDDR block. Resets FDDR AXI interface.
SDIF0_SPLL_LOCK	Input	Indicates PLL lock from SERDESIF_0 block.
SDIF0_PHY_RESET_N	Output	Active low PHY reset to SERDESIF_0 block
SDIF0_CORE_RESET_N	Output	Active low core reset to SERDESIF_0 block
SDIF1_SPLL_LOCK	Input	Indicates PLL lock from SERDESIF_1 block.
SDIF1_PHY_RESET_N	Output	Active low PHY reset to SERDESIF_1 block
SDIF1_CORE_RESET_N	Output	Active low core reset to SERDESIF_1 block
SDIF2_SPLL_LOCK	Input	Indicates PLL lock from SERDESIF_2 block.
SDIF2_PHY_RESET_N	Output	Active low PHY reset to SERDESIF_2 block
SDIF2_CORE_RESET_N	Output	Active low core reset to SERDESIF_2 block

Port Name	Type	Description
SDIF3_SPLL_LOCK	Input	Indicates PLL lock from SERDESIF_3 block.
SDIF3_PHY_RESET_N	Output	Active low PHY reset to SERDESIF_3 block
SDIF3_CORE_RESET_N	Output	Active low core reset to SERDESIF_3 block

Note: All signals in this table are active high unless otherwise stated.

Tool Flows

SmartDesign

Connecting CoreSF2Reset in SmartDesign

Peripheral blocks can be selected using check boxes available in the configuration GUI for CoreSF2Reset. If a peripheral block is not in use, the ports related to that peripheral do not appear for connection on the CoreSF2Reset symbol.

Aside from peripheral specific signals, connection to some ports of CoreSF2Reset is optional. In particular, the EXT_RESET_* ports do not have to be used. That means, an I/O pad is not required to be used as an external reset source (and/or driver), if this functionality is not needed.
Similarly, the USER_FAB_RESET_IN_N port does not necessarily have to be used, if it is not required to initiate a reset from the fabric. The USER_FAB_RESET_N output from CoreSF2Reset is used to reset logic within the fabric.

Configuring CoreSF2Reset in SmartDesign

The CoreSF2Reset configuration GUI is shown in Figure 2 on page 10. Essentially, there are four aspects of interest:

- The condition(s) under which the EXT_RESET_OUT signal is asserted.
  Note: Use of this signal to drive an external reset pin is optional. It does not have to be used.
- Device voltage. The device voltage determines the frequency of the RC oscillator clock which is used to clock interval timers within CoreSF2Reset. When device voltage is 1.0 V, RC oscillator frequency will be 25 MHz. When device voltage is 1.2 V, RC oscillator frequency will be 50 MHz.
- Peripheral blocks being used. If a particular block is not in use, the ports related to that block do not appear for connection on the CoreSF2Reset symbol.
- Settling time allowed for DDR memory. After the reset signals to the MDDR and FDDR blocks have been released, some time must be allowed before the DDR memory can be accessed. A waiting time in the range of 5 to 5000 microseconds can be specified. This sets the minimum time that must have elapsed after the release of the FDDR_CORE_RESET_N and MDDR_CORE_RESET_N signals before USER_FAB_RESET_N is released, and INIT_DONE is asserted.

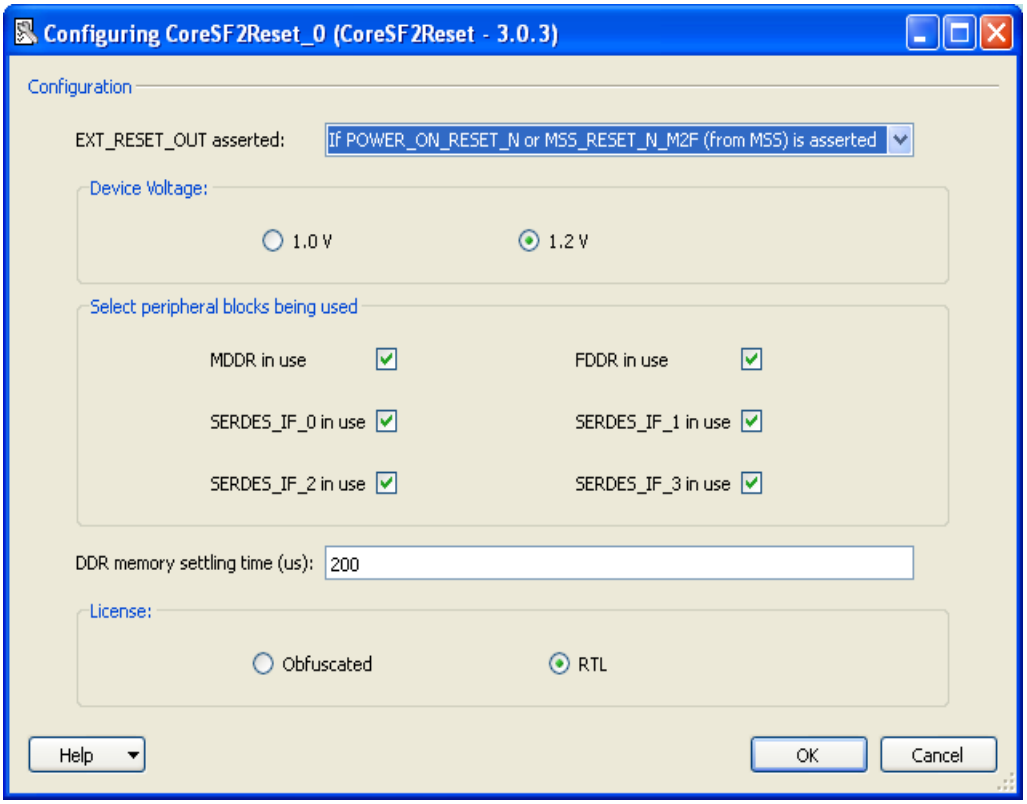

Figure 2 CoreSF2Reset Configuration GUI

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Microsemi SoC Products Group Customer Support website for more information and support (http://www.microsemi.com/soc/support/search/default.aspx). Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on website.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

50200406-0/06.13