CoreSDR_AHB v4.3 Release Notes

This is the production release for the CoreSDR_AHB IP core. This release notes describe the CoreSDR_AHB IP for the SmartFusion®2 and IGLOO®2 supports. It also contains information about system requirements, supported families, implementations, and known issues and workarounds.

Features

CoreSDR_AHB supports the following:

- Provides high performance, single-data-rate (SDR) controller for standard SDRAM chips, and dual in-line memory modules (DIMMs)
- Provides synchronous interface, fully pipelined internal architecture
- Supports up to 1024 MB of memory
- Bank management logic monitors status of up to 8 SDRAM banks
- Support for advanced high-performance bus (AHB) slave interface
- Data access of 8, 16, and 32 bits are allowed by masters

Interfaces

Supported interface is AHB.

Delivery Types

The CoreSDR_AHB is licensed as register transfer level (RTL).

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- ProASIC®3
- ProASIC3E
- ProASIC3L
- Fusion
- SmartFusion2
- IGLOO2

Supported Tool Flows

Use Libero SoC v10.0 or later with this CoreSDR_AHB release.

Installation Instructions

Within Libero SoC, a local CCZ file can be located and installed by clicking Add Core in the IP Catalog, or the automatic web update feature can be used in Libero SoC. Once the CCZ file is installed in Libero SoC, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero SoC project.

Refer to the *Using DirectCore in Libero IDE User Guide* or *Libero SoC online help* for further instructions on core installation, licensing, and general use.

Documentation

The release contains a copy of the *CoreSDR_AHB Handbook*. The handbook describes the core functionality, gives implementation suggestions, and provides step-by-step instructions on how to simulate, synthesize, and place-and-route this core.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: www.microsemi.com/soc.

Supported Test Environments

The following test environments are supported:

- VHDL User testbench
- Verilog User testbench

Release History

Table 1 lists the release history for this core.

Table 1. Release History

Core Version	Date	Changes
4.3	August 2014	As listed in Table 2.
4.1	March 2011	As listed in Table 3.
4.0	June 2009	Initial version.

Resolved Issues in the v4.3 Release

Table 2 lists the software action requests (SARs) that were resolved in the CoreSDR_AHB v4.3 release.

Table 2. Resolved SARs in CoreSDR_AHB v4.3 Release

SAR	Description
58830	Added SmartFusion2 and IGLOO2 support.
44307	Write data is wrote in to the memory before its latched on AHB interface

Resolved Issues in the v4.1 Release

Table 3 lists the SARs that were resolved in the CoreSDR_AHB v4.1 release.

Table 3. Resolved SARs in CoreSDR_AHB v4.1 Release

SAR	Description
19346	Added support to IGLOO, IGLOOe, IGLOO PLUS and SmartFusion device family.

Discontinued Features and Devices

There are no discontinued features or devices.

Known Limitations and Workarounds

There are no known issues in this release.

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