

**RN0089**

**CoreRMII v3.0 Release Notes**





**Microsemi Corporate Headquarters**

One Enterprise, Aliso Viejo,  
CA 92656 USA

Within the USA: +1 (800) 713-4113

Outside the USA: +1 (949) 380-6100

Sales: +1 (949) 380-6136

Fax: +1 (949) 215-4996

E-mail: [sales.support@microsemi.com](mailto:sales.support@microsemi.com)

[www.microsemi.com](http://www.microsemi.com)

© 2017 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

**About Microsemi**

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 4,800 employees globally. Learn more at [www.microsemi.com](http://www.microsemi.com).

# 1 Revision History

---

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 2.0

Updated changes related to CoreRMII v3.0.

## 1.2 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreRMII v2.0.

# Contents

---

<b>1</b>	<b>Revision History</b>	<b>3</b>
1.1	Revision 2.0	3
1.2	Revision 1.0	3
<b>2</b>	<b>CoreRMII v3.0 Release Notes</b>	<b>5</b>
2.1	Overview	5
2.2	Features	5
2.3	Delivery Types	5
2.4	Supported Families	5
2.5	Supported Tool Flows	5
2.6	Installation Instructions	5
2.7	Documentation	5
2.8	Supported Test Environments	6
2.9	Resolved History	6
	2.9.1 Resolved Issues in the v3.0 Release	6
	2.9.2 Resolved Issues in the v2.0 Release	6
2.10	Discontinued Features and Devices	6
2.11	Known Limitations and Workarounds	6

## 2 CoreRMII v3.0 Release Notes

---

### 2.1 Overview

These release notes accompany the production release of CoreRMII v3.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

### 2.2 Features

CoreRMII has the following features:

- Provides reduced pin-count interface for Ethernet PHYs.
- Provides media independent interface (MII) interface towards the microcontroller subsystem (MSS)-side and reduced media independent interface (RMII) on the PHY side.
- Supports 25 MHz clock operation on the MII-side, 50 MHz on the RMII-side for 10/100 Mbps mode operation.
- Provides MDIO interface as defined in clause 22 of IEEE 802.3 standard to control the transfer type, the link speed and the loopback mode.

### 2.3 Delivery Types

No License is required to use CoreRMII. A complete hardware description language (HDL) source code is provided for the core and testbenches.

### 2.4 Supported Families

- PolarFire
- IGLOO®2
- SmartFusion®2

### 2.5 Supported Tool Flows

CoreRMII v3.0 requires Libero® System-on-Chip (SoC) v11.0 or later.

### 2.6 Installation Instructions

The CoreRMII CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the [Libero SoC Online Help](#) for further instructions on core installation, licensing, and general use.

### 2.7 Documentation

This release contains a copy of the *CoreRMII Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the [Libero SoC Online Help](#) for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

<http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>.

## 2.8 Supported Test Environments

- Verilog user testbench
- VHDL user testbench

## 2.9 Resolved History

Table 1 lists the release history for CoreRMII.

**Table 1 • Release History**

Version	Date	Changes
3.0	April 2017	Resolved SARs listed in Table 2.
2.0	July 2013	Initial release.

### 2.9.1 Resolved Issues in the v3.0 Release

**Table 2 • Resolved Issues in the v3.0 Release**

SAR Number	Changes
63024	CoreRMII display name should arguably be "CoreRMII" and not "CORERMII".
81496	CoreRMII requirement to support MDIO/MDC interface.

### 2.9.2 Resolved Issues in the v2.0 Release

There were no unresolved SARs for CoreRMII v2.0. This was the first production release.

## 2.10 Discontinued Features and Devices

Parameters TRANSFER\_SPEED, TRANSFER\_TYPE and LOOPBACK, which were used for core configuration are removed in CoreRMII v3.0.

## 2.11 Known Limitations and Workarounds

There are no known limitations and workarounds for CoreRMII v3.0.