CoreResetP v7.1

Handbook

Microsemi

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Introduction

Core Overview

CoreResetP handles sequencing of reset signals in a SmartFusion®2 or IGLOO®2 device. This core deals with the resets related to the peripheral blocks including the double data rate (DDR) controllers and high speed serial interface (SERDESIF) blocks.

If the System Builder tool is used within the Libero® System-on-Chip (SoC) software to construct a design targeted at a SmartFusion2 or IGLOO2 device, CoreResetP will automatically be instantiated and connected within the design if required.

Figure 1 shows an overview of how CoreResetP is connected to other components.

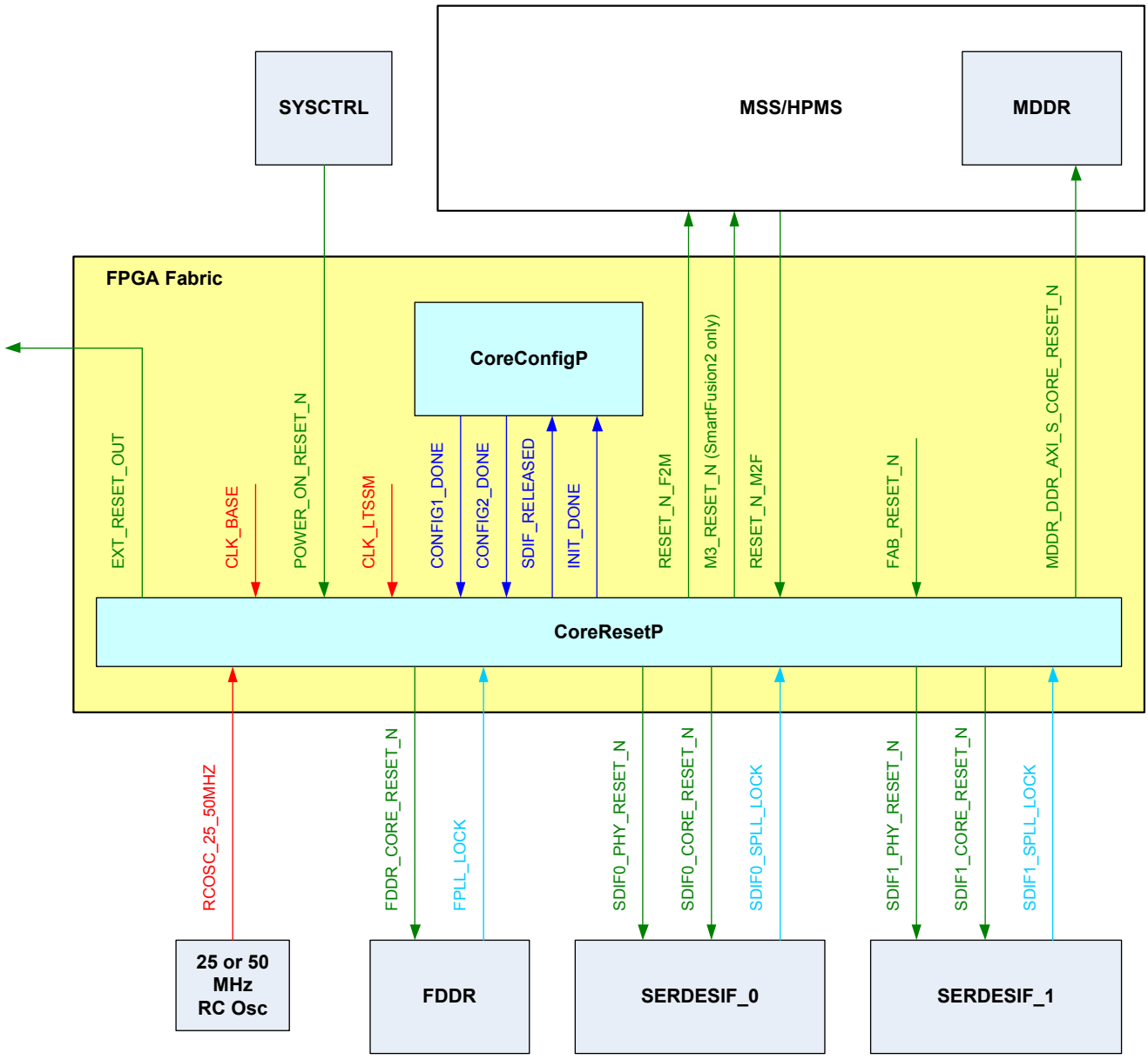

Figure 1 CoreResetP Connections

Key Features

- Sequences reset signals in a SmartFusion2 or IGLOO2 device

Supported Microsemi® FPGA Families

CoreResetP supports the following families:

- SmartFusion2
- IGLOO2

Core Version

This handbook supports CoreResetP v7.1.

Interface Description

Parameters

The parameters present on CoreResetP are listed in Table 1.

Table 1 CoreResetP Parameters

Parameter	Description
EXT_RESET_CFG	0 = EXT_RESET_OUT is never asserted 1 = EXT_RESET_OUT is asserted if the POWER_ON_RESET_N input is asserted 2 = EXT_RESET_OUT is asserted if the MSS_HPMS_READY output is not asserted 3 = EXT_RESET_OUT is asserted if the POWER_ON_RESET_N input is asserted or the MSS_HPMS_READY output is not asserted
DEVICE_VOLTAGE	1 = 1.0 V (RC oscillator frequency = 25 MHz) 2 = 1.2 V (RC oscillator frequency = 50 MHz)
MDDR_IN_USE	1 = MDDR block is in use.
FDDR_IN_USE	1 = FDDR block is in use.
SDIF0_IN_USE	1 = SERDESIF_0 block is in use.
SDIF1_IN_USE	1 = SERDESIF_1 block is in use.
SDIF2_IN_USE	1 = SERDESIF_2 block is in use.
SDIF3_IN_USE	1 = SERDESIF_3 block is in use.
SDIF0_PCIE	1 = SERDESIF_0 block is used for PCIe.
SDIF1_PCIE	1 = SERDESIF_1 block is used for PCIe.
SDIF2_PCIE	1 = SERDESIF_2 block is used for PCIe.
SDIF3_PCIE	1 = SERDESIF_3 block is used for PCIe.
SDIF0_PCIE_HOTRESET	1 = If SERDESIF_0 block is used for PCIe, include support for Hot Reset. SDIF0_PCIE_HOTRESET should be set to 0 in an 060 or 090 device because the SERDESIF block present in an 060 or 090 device inherently supports PCIe Hot Reset.
SDIF1_PCIE_HOTRESET	1 = If SERDESIF_1 block is used for PCIe, include support for Hot Reset. SDIF1_PCIE_HOTRESET should be set to 0 in an 060 or 090 device because the SERDESIF block present in an 060 or 090 device inherently supports PCIe Hot Reset.
SDIF2_PCIE_HOTRESET	1 = If SERDESIF_2 block is used for PCIe, include support for Hot Reset. SDIF2_PCIE_HOTRESET should be set to 0 in an 060 or 090 device because the SERDESIF block present in an 060 or 090 device inherently supports PCIe Hot Reset.
SDIF3_PCIE_HOTRESET	1 = If SERDESIF_3 block is used for PCIe, include support for Hot Reset. SDIF3_PCIE_HOTRESET should be set to 0 in an 060 or 090 device because the SERDESIF block present in an 060 or 090 device inherently supports PCIe Hot Reset.

Parameter	Description
SDIF0_PCIE_L2P2	1 = If SERDESIF_0 block is used for PCIe, include support for L2/P2 power states. SDIF0_PCIE_L2P2 should be set to 0 in an 060 or 090 device because the SERDESIF block present in an 060 or 090 device inherently supports PCIe L2/P2 power states.
SDIF1_PCIE_L2P2	1 = If SERDESIF_1 block is used for PCIe, include support for L2/P2 power states. SDIF0_PCIE_L2P2 should be set to 0 in an 060 or 090 device because the SERDESIF block present in an 060 or 090 device inherently supports PCIe L2/P2 power states.
SDIF2_PCIE_L2P2	1 = If SERDESIF_2 block is used for PCIe, include support for L2/P2 power states. SDIF0_PCIE_L2P2 should be set to 0 in an 060 or 090 device because the SERDESIF block present in an 060 or 090 device inherently supports PCIe L2/P2 power states.
SDIF3_PCIE_L2P2	1 = If SERDESIF_3 block is used for PCIe, include support for L2/P2 power states. SDIF0_PCIE_L2P2 should be set to 0 in an 060 or 090 device because the SERDESIF block present in an 060 or 090 device inherently supports PCIe L2/P2 power states.
ENABLE_SOFT_RESETS	1 = SOFT_* input signals can be used to assert corresponding reset outputs. The SOFT_* inputs are normally driven by an instance of the CoreConfigP core.
DEVICE_090	1 = The target device is a 060 or 090 sized device.

Ports

The ports present on CoreResetP are listed in Table 2.

Table 2 CoreResetP Ports

Port Name	Type	Description
RCOSC_25_50MHZ	Input	25 MHz or 50 MHz clock from RC oscillator.
CLK_BASE	Input	Should be driven by the same clock signal that drives the CLK_BASE input of the MSS/HPMS.
CLK_LTSSM	Input	Clock signal used to sample Link Training and Status State Machine (LTSSM) data that's present on the APB read data buses from the SERDESIF blocks during idle APB cycles. The frequency of CLK_LTSSM should be high enough to track the transitions in the LTSSM data. A frequency in the range 100 to 125 MHz is recommended.
POWER_ON_RESET_N	Input	Active low power on reset from system controller.
EXT_RESET_OUT	Output	Output suitable for driving an external reset pin.
RESET_N_F2M	Output	Active low reset signal to MSS/HPMS. Resets MSS/HPMS.
M3_RESET_N	Output	Active low reset signal to MSS. Resets Cortex-M3 processor. This signal is only relevant when CoreResetP is used in a SmartFusion2 device.
RESET_N_M2F	Input	Active low reset from MSS/HPMS.
FIC_2_APB_M_PRESET_N	Input	Active low reset from MSS/HPMS.
MDDR_DDR_AXI_S_CORE_RESET_N	Output	Active low reset to MSS/HPMS. Resets MDDR AXI interface.
MSS_HPMS_READY	Output	After power on or reset this signal will be low until the

Port Name	Type	Description
		MSS/HPMS is ready for use, at which point it will go high.
DDR_READY	Output	After power on or reset this signal will be low until the DDR controllers are ready for use, at which point it will go high.
SDIF_READY	Output	After power on or reset this signal will be low until the SERDESIF blocks are ready for use, at which point it will go high.
INIT_DONE	Output	Indicates the completion of the initialization. Asserted when peripheral configuration and reset sequencing are completed. Normally, connected to CoreConfigP.
SDIF_RELEASED	Output	Indicates that the SERDESIF blocks have been released from reset. Normally connected to CoreConfigP.
CONFIG1_DONE	Input	Indicates the completion of the first stage of configuration from CoreConfigP.
CONFIG2_DONE	Input	Indicates the completion of the second stage of configuration from CoreConfigP.
FAB_RESET_N	Input	Active low reset input from user logic in fabric.
FPLL_LOCK	Input	Indicates phase-locked loop (PLL) lock from FDDR block.
FDDR_CORE_RESET_N	Output	Active low reset to FDDR block. Resets FDDR AXI interface.
SDIF0_SPLL_LOCK	Input	Indicates PLL lock from SERDESIF_0 block.
SDIF0_PHY_RESET_N	Output	Active low PHY reset to SERDESIF_0 block
SDIF0_CORE_RESET_N	Output	Active low core reset to SERDESIF_0 block This signal is used in devices that have a single PCIe controller within the SERDESIF_0 block.
SDIF0_0_CORE_RESET_N	Output	Active low core reset to SERDESIF_0 block. This signal is used in devices that have two PCIe controllers within the SERDESIF_0 block.
SDIF0_1_CORE_RESET_N	Output	Active low core reset to SERDESIF_0 block. This signal is used in devices that have two PCIe controllers within the SERDESIF_0 block.
SDIF1_SPLL_LOCK	Input	Indicates PLL lock from SERDESIF_1 block.
SDIF1_PHY_RESET_N	Output	Active low PHY reset to SERDESIF_1 block
SDIF1_CORE_RESET_N	Output	Active low core reset to SERDESIF_1 block
SDIF2_SPLL_LOCK	Input	Indicates PLL lock from SERDESIF_2 block.
SDIF2_PHY_RESET_N	Output	Active low PHY reset to SERDESIF_2 block
SDIF2_CORE_RESET_N	Output	Active low core reset to SERDESIF_2 block
SDIF3_SPLL_LOCK	Input	Indicates PLL lock from SERDESIF_3 block.
SDIF3_PHY_RESET_N	Output	Active low PHY reset to SERDESIF_3 block.
SDIF3_CORE_RESET_N	Output	Active low core reset to SERDESIF_3 block.
SDIF0_PERST_N	Input	SERDESIF_0 active low PCIe reset signal
SDIF1_PERST_N	Input	SERDESIF_1 active low PCIe reset signal
SDIF2_PERST_N	Input	SERDESIF_2 active low PCIe reset signal
SDIF3_PERST_N	Input	SERDESIF_3 active low PCIe reset signal

Port Name	Type	Description
SDIF0_PSEL	Input	SERDESIF_0 APB select signal
SDIF0_PWRITE	Input	SERDESIF_0 APB write signal
SDIF0_PRDATA[31:0]	Input	SERDESIF_0 APB write data
SDIF1_PSEL	Input	SERDESIF_1 APB select signal
SDIF1_PWRITE	Input	SERDESIF_1 APB write signal
SDIF1_PRDATA[31:0]	Input	SERDESIF_1 APB write data
SDIF2_PSEL	Input	SERDESIF_2 APB select signal
SDIF2_PWRITE	Input	SERDESIF_2 APB write signal
SDIF2_PRDATA[31:0]	Input	SERDESIF_2 APB write data
SDIF3_PSEL	Input	SERDESIF_3 APB select signal
SDIF3_PWRITE	Input	SERDESIF_3 APB write signal
SDIF3_PRDATA[31:0]	Input	SERDESIF_3 APB write data
SOFT_EXT_RESET_OUT	Input	When high, the EXT_RESET_OUT output is asserted (high)
SOFT_RESET_F2M	Input	When high, the RESET_N_F2M output is asserted (low)
SOFT_M3_RESET	Input	When high, the M3_RESET_N output is asserted (low)
SOFT_MDDR_DDR_AXI_S_CORE_RESET	Input	When high, the MDDR_DDR_AXI_S_CORE_RESET_N output is asserted (low)
SOFT_FDDR_CORE_RESET	Input	When high, the FDDR_CORE_RESET_N output is asserted (low)
SOFT_SDIF0_PHY_RESET	Input	When high, the SDIF0_PHY_RESET_N output is asserted (low)
SOFT_SDIF0_CORE_RESET	Input	When high, the SDIF0_CORE_RESET_N output is asserted (low)
SOFT_SDIF1_PHY_RESET	Input	When high, the SDIF1_PHY_RESET_N output is asserted (low)
SOFT_SDIF1_CORE_RESET	Input	When high, the SDIF1_CORE_RESET_N output is asserted (low)
SOFT_SDIF2_PHY_RESET	Input	When high, the SDIF2_PHY_RESET_N output is asserted (low)
SOFT_SDIF2_CORE_RESET	Input	When high, the SDIF2_CORE_RESET_N output is asserted (low)
SOFT_SDIF3_PHY_RESET	Input	When high, the SDIF3_PHY_RESET_N output is asserted (low)
SOFT_SDIF3_CORE_RESET	Input	When high, the SDIF3_CORE_RESET_N output is asserted (low)
SOFT_SDIF0_0_CORE_RESET	Input	When high, the SDIF0_0_CORE_RESET_N output is asserted (low)
SOFT_SDIF0_1_CORE_RESET	Input	When high the SDIF0_1_CORE_RESET_N output is asserted (low)

Note: All signals in this table are active high unless otherwise stated.

Tool Flows

SmartDesign

If the System Builder tool is used within the Libero SoC software to construct a design targeted at a SmartFusion2 or IGLOO2 device, CoreResetP will automatically be instantiated and connected within the design if required. You can manually instantiate and configure CoreResetP within a SmartDesign design if required.

Connecting CoreResetP in SmartDesign

Peripheral blocks can be selected using check boxes available in the configuration GUI for CoreResetP. If a peripheral block is not in use, the ports related to that peripheral do not appear for connection on the CoreResetP symbol.

Configuring CoreResetP in SmartDesign

The CoreResetP configuration GUI is shown in Figure 2 on page 10. There are a number of aspects of interest as outlined below:

- The condition(s) under which the EXT_RESET_OUT signal is asserted.
  Note: Use of this signal to drive an external reset pin is optional. It does not have to be used.
- Device voltage. The device voltage determines the frequency of the RC oscillator clock which is used to clock interval timers within CoreResetP. When device voltage is 1.0 V, RC oscillator frequency will be 25 MHz. When device voltage is 1.2 V, RC oscillator frequency will be 50 MHz.
- DDR usage. Select MDDR and FDDR checkboxes to select MDDR and FDDR usage. You can also configure the DDR memory settling time. After the reset signals to the MDDR and FDDR blocks are released, some time must be allowed before the DDR memory can be accessed. A waiting time of between 5 to 5000 microseconds can be specified. This sets the minimum time that must have elapsed after the release of the FDDR_CORE_RESET_N and MDDR_CORE_RESET_N signals before INIT_DONE is asserted.
- SERDES interface usage. There is a panel for each SERDES interface block. There are options to select if a SERDES interface is in use and if it is used for PCIe. When a SERDESIF block is used for PCIe, support for PCIe Hot Reset and L2/P2 compatibility can be selected. When a 060 or 090 device is targeted, the checkboxes for PCIe Hot Reset and L2/P2 support should be left unchecked because the SERDESIF block in a 060 or 090 device inherently supports PCIe Hot Reset and L2/P2 power states.
- A checkbox allows support for soft reset inputs to be selected. When this checkbox is checked, the SOFT_* inputs to the core can be used to assert the various reset outputs from the core. The SOFT_* inputs are typically driven by an instance of the CoreConfigP block.

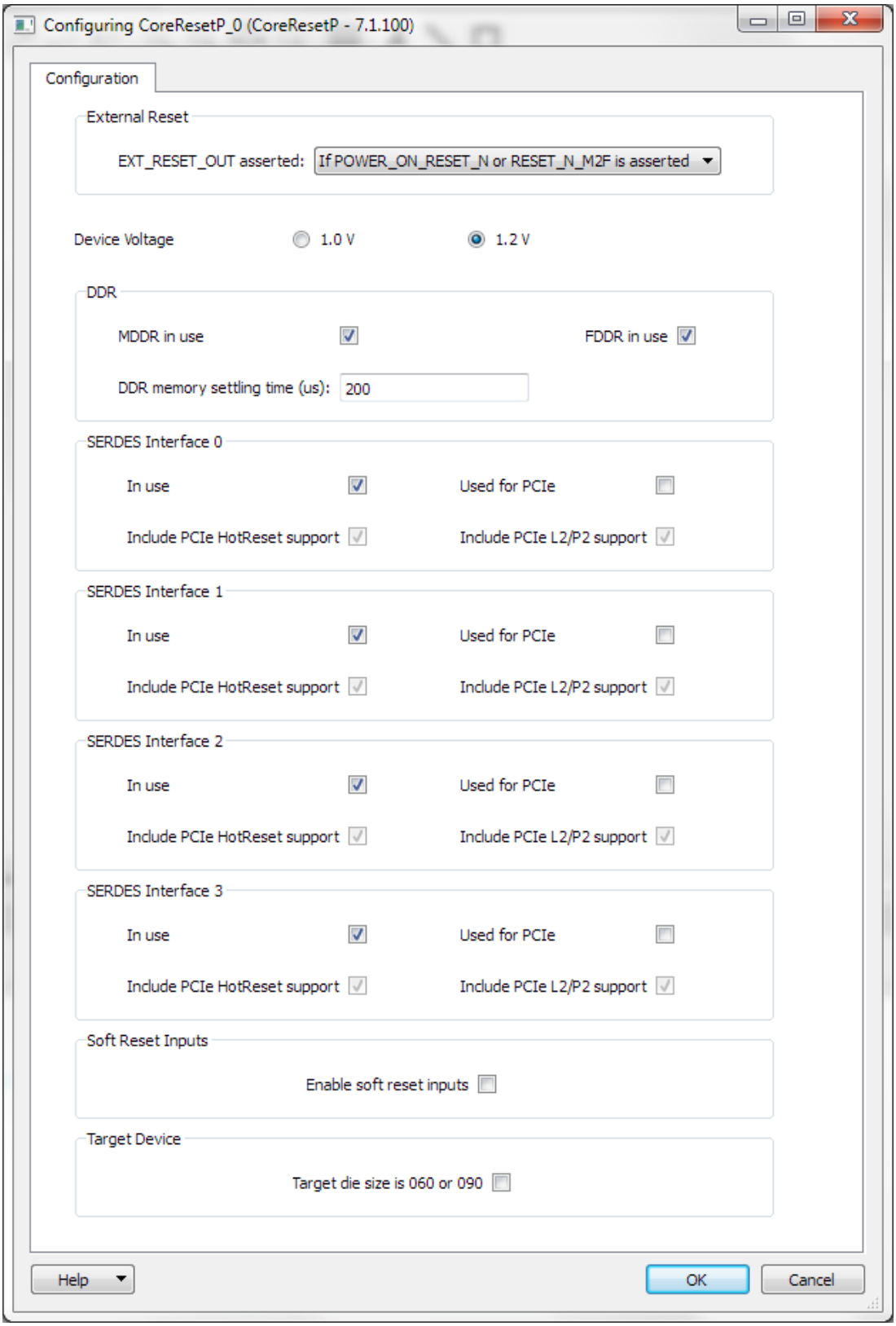

Figure 2 CoreResetP Configurations Window

Timing Diagrams

Figure 3 to Figure 5 show the timing of reset signals for reset sequences initiated by the assertion of POWER_ON_RESET_N, FIC_2_APB_M_PRESET_N, and FAB_RESET_N signals.

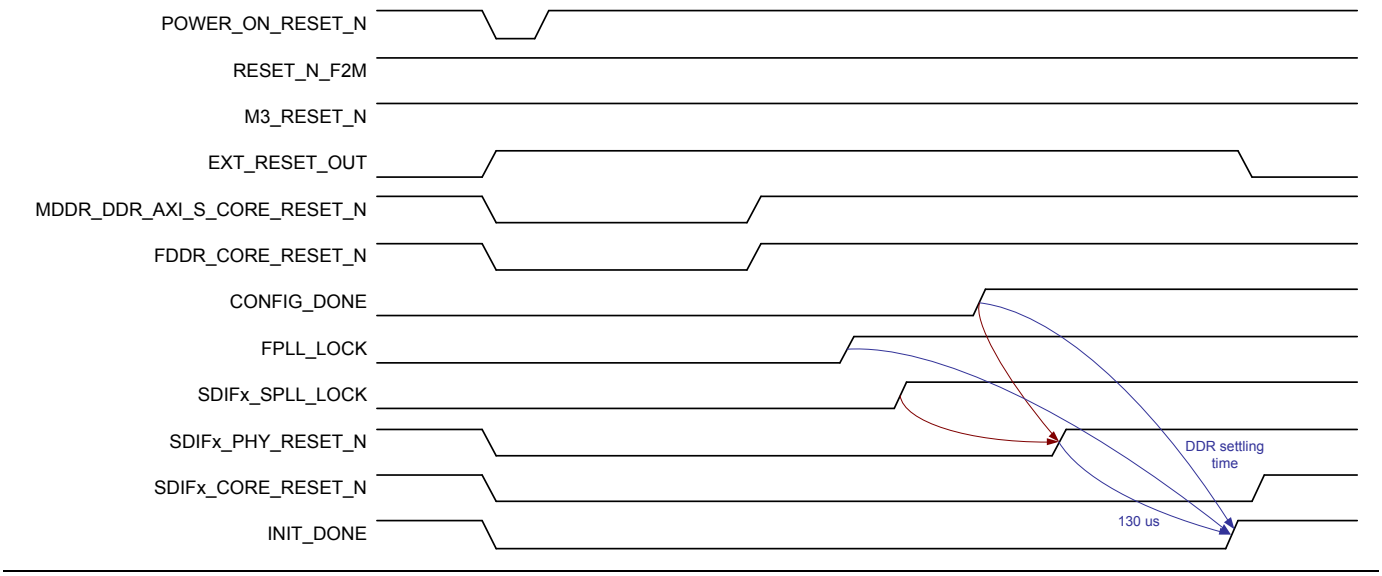

Figure 3 Timing for Reset Signals Initiated by the Assertion of POWER_ON_RESET_N

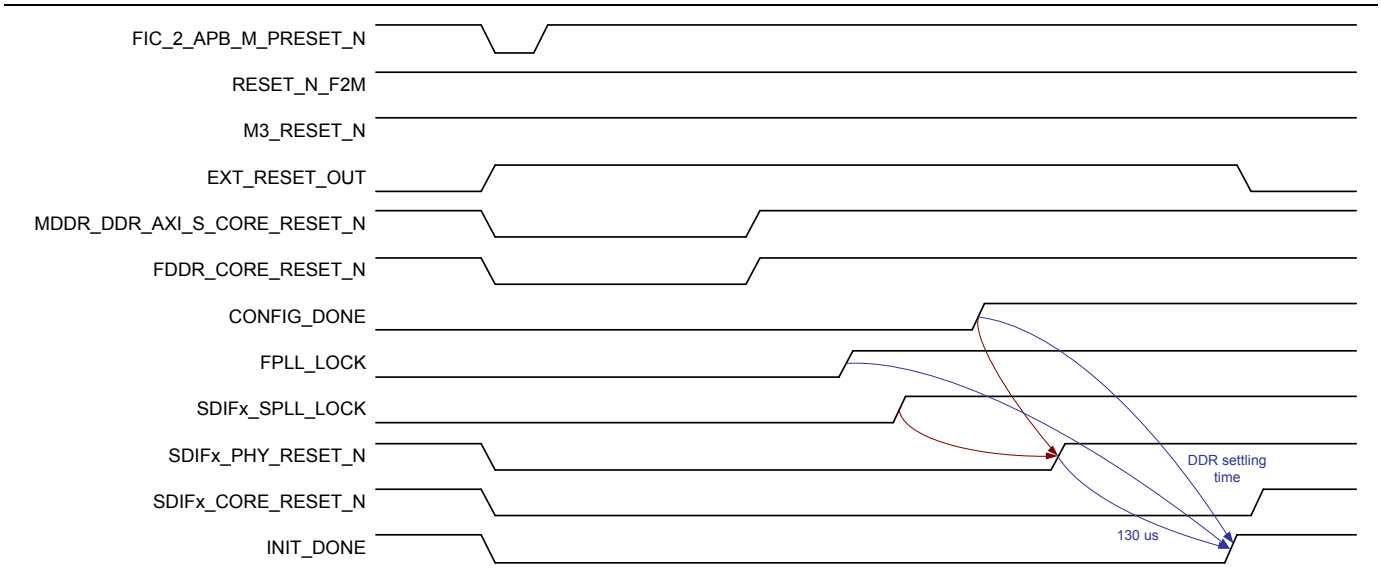

Figure 4 Timing for Reset Signals Initiated by the Assertion of FIC_2_APB_M_PRESET_N

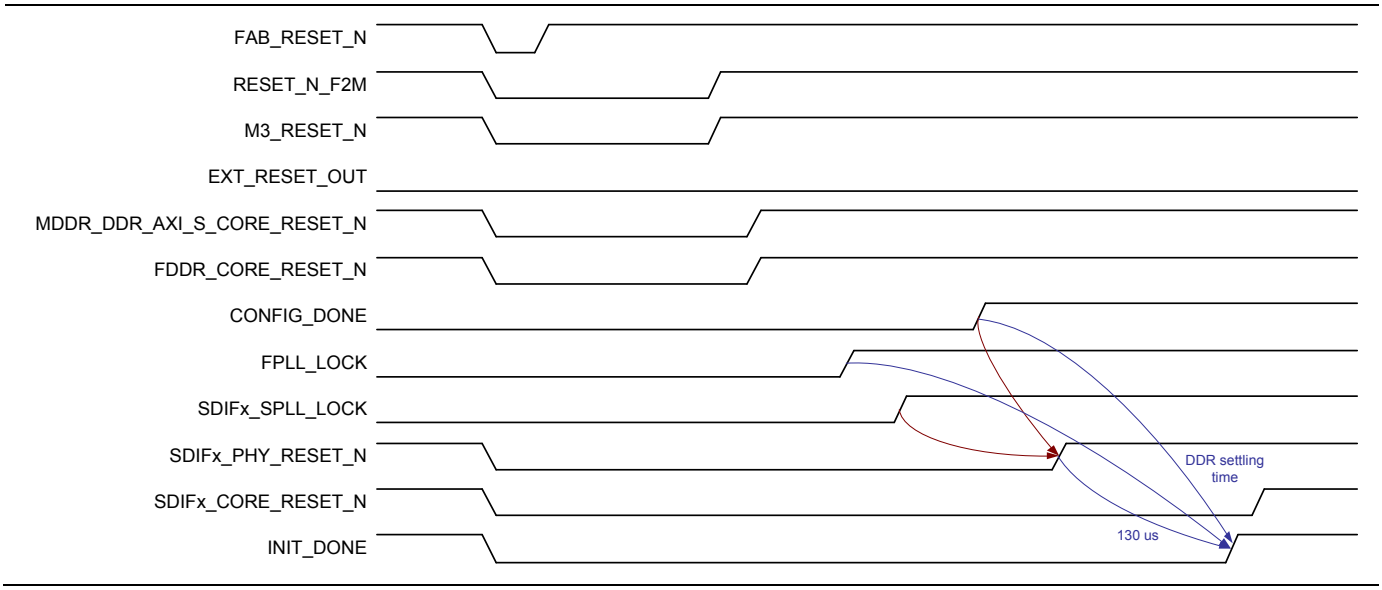

Figure 5 Timing for Reset Signals Initiated by the Assertion of FAB_RESET_N

List of Changes

The following table lists important changes that were made in each revision of the document.

Date	Change	Page
May 2016	CoreResetP v7.1 release.	N/A
June 2014	CoreResetP v7.0 release.	N/A
January 2014	CoreResetP v5.1 release.	N/A
July 2013	CoreResetP v4.0 release.	N/A
June 2013	CoreResetP v3.0 release.	N/A

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