CoreQEI v2.0

Handbook

Actel
POWER MATTERS

Actel Corporation, Mountain View, CA 94043

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Trademarks

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Introduction

The Quadrature Encoder Interface (QEI) decodes speed and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback.

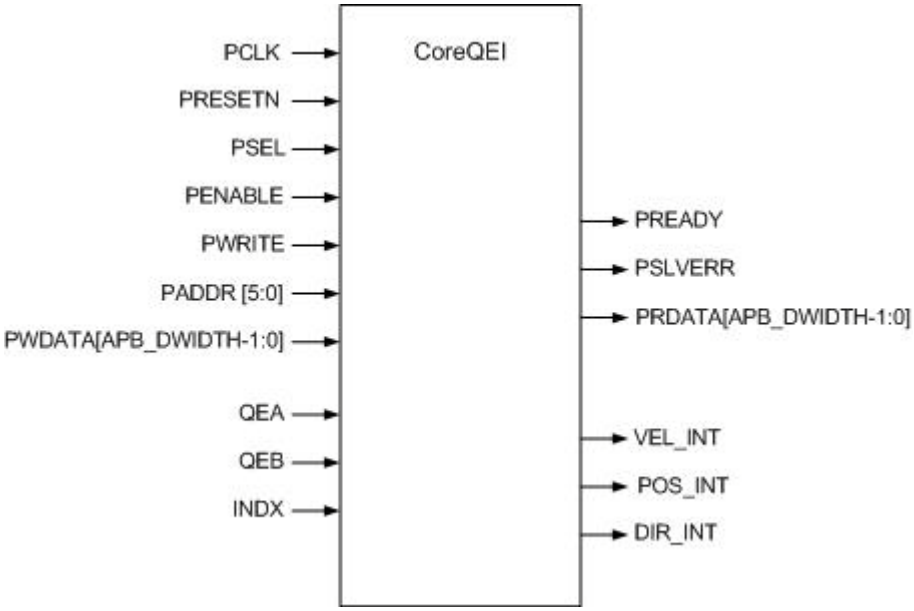

Figure 1 CoreQEI I/O Signal Diagram

Key Features

- Two phase signals (QEA) and QEB) and one index signal (INDX)
- Direction of movement detection with a direction change interrupt
- Programmable input noise filters on QEA, QEB, and INDX
- 16-bit up/down position counter
- Standard and high-precision position tracking modes
- Two position update modes (x2 and x4)
- Velocity measurement with a programmable postscaler for high-speed velocity measurement
- Position counter interrupt
- Velocity control interrupt

Supported Actel FPGA Families

- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC3
- ProASIC3E
- ProASIC®3L
- SmartFusion
- Fusion
- ProASIC PLUS®
- Axcelerator®
- RTAX-S
- RTAX-DSP

Core Version

This handbook supports CoreQEI v2.0.

Supported Interfaces

CoreQEI supports an AMBA3 APB slave interface.

Utilization and Performance

CoreQEI has been implemented in several of Actel's device families using standard speed grades. A summary of various implementation data is listed in Table 1.

Table 1 CoreQEI Device Utilization and Performance

Family	Tiles			Utilization		Performance (MHz)
	Sequential	Combinatorial	Total	Device	Total %	
SmartFusion	140	343	483	A2F500	4%	84
Fusion	140	343	483	M1AFS1500	1%	84
IGLOO®/e, IGLOO PLUS	140	362	502	M1AGL1000V2	2%	46
ProASIC®3/E/L	140	341	481	M1A3P600	4%	77
ProASIC PLUS®	141	470	611	APA600	3%	68
Axcelerator®	140	157	297	AX500	4%	80
RTAX-S, RTAX-DSP	140	157	297	RTAX1000S	2%	76

Note: Data in this table were achieved with typical synthesis and layout settings.

Design Description

The CoreQEI has three main blocks: the control logic, the position counter, and velocity postscaler. Figure 2 below shows the top-level block diagram of the proposed design.

The QEI control logic detects the leading edge on the QEA or QEB phase input pins and generates the count pulse, which is sent to the position counter logic. It also samples the index input signal (INDX) and generates the direction of rotation signal (up/down) and the velocity event signals.

The position counter acts as an integrator for tracking distance traveled. The QEA and QEB input edges serve as the stimulus to create the input clock, which advances the Position Counter register (POSCNT). The register is incremented on either the QEA input edge or the QEA and QEB input edges, depending on the operating mode. It is reset either by a rollover on match to the Period register, MAXCNT, or on the external index pulse input signal (INDX).

The velocity postscaler down-samples the velocity pulses used to increment the velocity counter by a specified ratio. It essentially divides down the number of velocity pulses to one output per so many inputs, preserving the pulse width in the process. Velocity capture uses an internal timer and count register. The timer counts down from the timer load register value and when the timer reaches zero, it reloads the value from the timer load register. The timer counts the number of phase edges (using the postscaler velocity pulses) in a given time period. The edge count from the previous time period is available to the controller via the velocity register. As soon as the current time period is complete, the total number of edges counted in that time period is made available in the velocity register (overwriting the previous value), and counting commences on a new time period. The number of edges counted in a given time period is directly proportional to the velocity of the encoder.

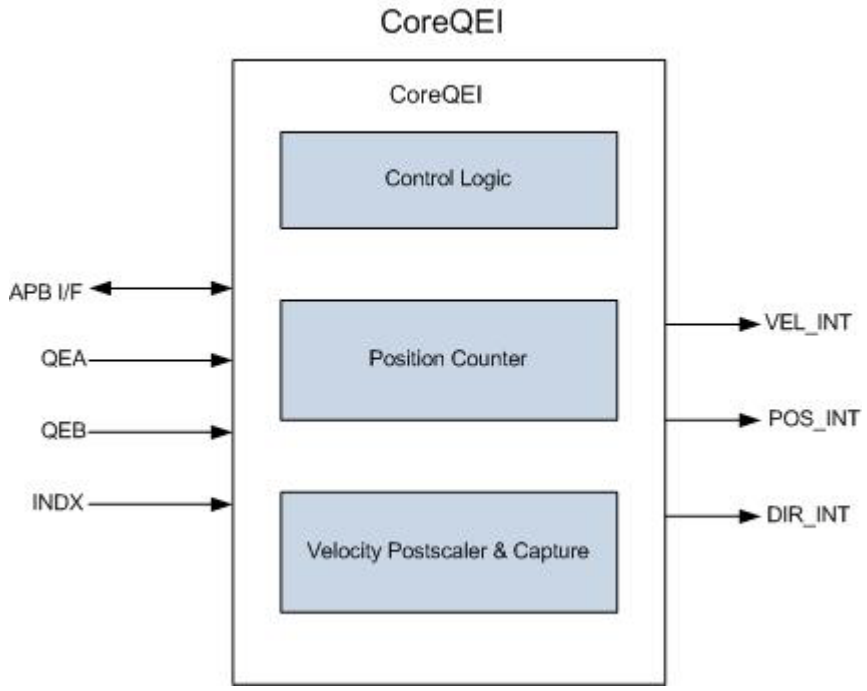

Figure 2 : CoreQEI block diagram

Verilog/VHDL Parameters

CoreQEI has parameters (Verilog) or generics (VHDL) for configuring the RTL code, described in Table 2. The parameter or generic is integer type.

Table 2 CoreQEI Parameters/Generics Descriptions

Parameter Name	Valid Range	Default	Description
APB_DWIDTH	8, 16, 32	8	APB data bus width can be 8, 16, or 32

I/O Signals

The port signals for the CoreQEI macro are illustrated in Figure 1 on page 5 and defined in Table 3.

Table 3 CoreQEI I/O Signal Descriptions

Port Name	Type	Description
APB Interface		
PCLK	Input	System clock – all operations and status shall be synchronous to the rising-edge of this clock signal.
PRESETN	Input	Active low synchronous reset
PSEL	Input	Select line for CoreQEI
PENABLE	Input	Enable signal for APB transfer
PWRITE	Input	Write enable if high, read enable if low
PADDR[5:0]	Input	Register address
PWDATA[APB_DWIDTH-1:0]	Input	Write data input
PREADY	Output	Ready signal, tied high
PSLVERR	Output	Transfer error signal, tied low
PRDATA[APB_DWIDTH-1:0]	Output	Read data output
QEI Interface		
QEA	Input	Phase A
QEB	Input	Phase B
INDX	Input	Index
VEL_INT	Output	Velocity register update interrupt
POS_INT	Output	Position measurement update interrupt
DIR_INT	Output	Direction change interrupt

Note: All signals are active High (logic 1) unless otherwise noted.

Register Map and Descriptions

Register Summary (APB_DWIDTH = 8)

All registers are based on APB width parameter selection; default is 8 bits. Values shown in tables are in hexadecimal format; type designations: R = read only; W = write only; R/W = read/write.

Table 4 CoreQEI Internal Register Address Map (8-bit mode, APB_DWIDTH = 8)

Address	Register Name	Type	Width	Reset Value	Description
0x00	QEI_CR	R/W	8	0x00	Control Register
0x04	QEI_VELOCITY_H	R	8	0x00	Velocity Register, High Byte
0x08	QEI_VELOCITY_L	R	8	0x00	Velocity Register, Low Byte
0x0C	QEI_POSITION_H	R	8	0x00	Position Counter Register, High Byte
0x10	QEI_POSITION_L	R	8	0x00	Position Counter Register, Low Byte
0x14	QEI_LIMIT_H	R/W	8	0x00	Maximum Count Limit Register, High Byte
0x18	QEI_LIMIT_L	R/W	8	0x00	Maximum Count Limit Register, Low Byte
0x1C	QEI_IER	R/W	8	0x00	Interrupt Enable Register
0x20	QEI_SR	R/W	8	0x00	Status Register
0x24	QEI_TIMER_LOAD_H	R/W	8	0x00	Load Timer Value, High Byte
0x28	QEI_TIMER_LOAD_L	R/W	8	0x00	Load Time Value, Low Byte

Control Register

Table 5 Control Register

PADDR [5:0]	Register Name	Type	Width	Reset Value	Description
0x00	QEI_CR	R/W	8	0x00	Control Register

Table 6 Control Register Bit Definitions

Bits	Name	Type	Description
7:6	–	–	Reserved
5	FILTER_EN	R/W	Filter Enable/Disable bit 0 – Disable noise filter on input signals QEA, QEB and INDX 1 – Enable noise filter on input signals QEA, QEB and INDX
4:2	QEIM[2:0]	R/W	QEI Mode bits 100-111 = reserved 011 = QEI enabled in 4x Update mode; position counter reset on period match (POSCNT = MAXCNT) 010 = QEI enabled in 4x Update mode; INDX resets the position counter 001 = QEI enabled in 2x Update mode; position counter reset on period match (POSCNT = MAXCNT) 000 = QEI enabled in 2x Update mode; INDX resets the position counter

1:0	VPPR[1:0]	R/W	Velocity Pulse Reduction Ratio bit 11 =1:64 10 =1:16 01 =1:4 00 =1:1

Velocity Register

Table 7 Velocity Register

PADDR[5:0]	Register Name	Type	Width	Reset Value	Description
0x04	QEI_VELOCITY_H	R	8	0x00	Velocity Register, High Byte. This register contains the most recently measured velocity of the quadrature encoder. This value corresponds to the number of velocity pulses counted in the previous velocity timer period.
0x08	QEI_VELOCITY_L	R	8	0x00	Velocity Register, Low Byte. This register contains the most recently measured velocity of the quadrature encoder. This value corresponds to the number of velocity pulses counted in the previous velocity timer period.

Position Register

Table 8 Position Register

PADDR[5:0]	Register Name	Type	Width	Reset Value	Description
0x0C	QEI_POSITION_H	R	8	0x00	Position Register, High Byte
0x10	QEI_POSITION_L	R	8	0x00	Position Register, Low Byte

Maximum Count Limit Register

Table 9 Limit Register

PADDR[5:0]	Register Name	Type	Width	Reset Value	Description
0x14	QEI_LIMIT_H	R/W	8	0x00	Maximum Count Limit Register, High Byte
0x18	QEI_LIMIT_L	R/W	8	0x00	Maximum Count Limit Register, Low Byte

Interrupt Enable Register

Table 10 Interrupt Enable Register

PADDR[5:0]	Register Name	Type	Width	Reset Value	Description
0x1C	QEI_IER	R/W	8	0x00	Interrupt Enable Register

Table 11 Interrupt Enable Register Bit Definition

Bits	Name	Type	Description
7:3	–	–	Reserved
2	DIR_INT	R/W	Enable/Disable Direction of Rotation Interrupt (DIR_INT) 1 = Enables the Direction of Rotation Interrupt (DIR_INT) 0 = Disables the Direction of Rotation Interrupt (DIR_INT)
1	POS_INT	R/W	Enable/Disable Position Counter Interrupt (POS_INT) 1 = Enables Position Counter Interrupt (POS_INT) 0 = Disables Position Counter Interrupt (POS_INT)
0	VEL_INT	R/W	Enable/Disable Velocity Register Update (VEL_INT) 1 = Enables Velocity Register Update (VEL_INT) 0 = Disables Velocity Register Update (VEL_INT)

Status Register

Table 12 Interrupt Status Register

PADDR[5:0]	Register Name	Type	Width	Reset Value	Description
0x20	QEI_SR	R/W	8	0x00	Status Register

Table 13 Interrupt Status Register Bit Definition

Bits	Name	Type	Description
7:5	–	–	Reserved
4	ERROR	R	QEI error bit 1 = Position counter overflow or underflow 0 = No overflow or underflow
3	UP/DOWN	R	Direction of Rotation Status bit 1 = Forward 0 = Reverse
2	DIR_INT	R/W	Direction of Rotation Interrupt (DIR_INT) 1 = Direction of rotation has changed. Must be cleared by writing a ‘1’. 0 = Direction of rotation has not changed.

1	POS_INT	R/W	Position Counter Interrupt (POS_INT) 1 = The QEI position counter has reached the MAXCNT value or the index pulse, INDX, has been detected. Depends on the QEI operating mode enabled. Must be cleared by writing a '1'. 0 = The QEI position counter has not reached the MAXCNT value or the index pulse has not been detected.
0	VEL_INT	R/W	Velocity Register Update (VEL_INT) 1 = Velocity register updated. Must be cleared by writing a '1'. 0 = Velocity register not updated.

Timer Load Register

Table 14 Timer Load Register

PADDR[5:0]	Register Name	Type	Width	Reset Value	Description
0x24	QEI_TIMER_LOAD_H	R/W	8	0x00	Timer Load Register, High Byte. Load the time interval value for velocity.
0x28	QEI_TIMER_LOAD_L	R/W	8	0x00	Timer Load Register, Low Byte. Load the time interval value for velocity.

Register Summary (APB_DWIDTH = 16 or 32)

All registers are based on APB width parameter 16 or 32. Values shown in tables are in hexadecimal format; type designations: R = read only; W = write only; R/W = read/write.

Table 15 CoreQEI Internal Register Address Map (16- or 32-bit mode, APB_DWIDTH = 16 or 32)

Address	Register Name	Type	Width	Reset Value	Description
0x00	QEI_CR	R/W	16	0x0000	Control Register
0x04	QEI_VELOCITY	R	16	0x0000	Velocity Register. This register contains the most recently measured velocity of the quadrature encoder. This value corresponds to the number of velocity pulses counted in the previous velocity timer period.
0x08	QEI_POSITION	R	16	0x0000	Position Register
0x0C	QEI_LIMIT	R/W	16	0x0000	Maximum Count Limit Register
0x10	QEI_IER	R/W	16	0x0000	Interrupt Enable Register
0x14	QEI_SR	R/W	16	0x0000	Status Register
0x18	QEI_TIMER_LOAD	R/W	16	0x0000	Timer Load Register. Load the time interval value for velocity.

Control Register

Table 16 Control Register

PADDR[5:0]	Register Name	Type	Width	Reset Value	Description
0x00	QEI_CR	R/W	16	0x0000	Control Register

Table 17 Control Register Bit Definitions

Bit	Name	Type	Description
15:6	–	–	Reserved
5	FILTER_EN	R/W	Filter Enable/Disable bit 0 – Disable noise filter on input signals QEA, QEB and INDX 1 – Enable noise filter on input signals QEA, QEB and INDX
4:2	QEIM[2:0]	R/W	QEI Mode bits 100-111 = Reserved 011 = QEI enabled in 4x Update mode; position counter reset on period match (POSCNT = MAXCNT) 010 = QEI enabled in 4x Update mode; INDX resets the position counter 001 = QEI enabled in 2x Update mode; position counter reset on period match (POSCNT = MAXCNT) 000 = QEI enabled in 2x Update mode; INDX resets the position counter
1:0	VPRR[1:0]	R/W	Velocity Pulse Reduction Ratio bit 11 = 1:64 10 = 1:16 01 = 1:4 00 = 1:1

Velocity Register

Table 18 Velocity Register

PADDR[5:0]	Register Name	Type	Width	Reset Value	Description
0x04	QEI_VELOCITY	R	16	0x0000	Velocity Register. This register contains the most recently measured velocity of the quadrature encoder. This value corresponds to the number of velocity pulses counted in the previous velocity timer period.

Position Register

Table 19 Position Register

PADDR[5:0]	Register Name	Type	Width	Reset Value	Description
0x08	QEI_POSITION	R	16	0x0000	Position Register

Maximum Count Limit Register

Table 20 Limit Register

PADDR[5:0]	Register Name	Type	Width	Reset Value	Description
0x0C	QEI_LIMIT	R/W	16	0x0000	Maximum Count Limit Register

Interrupt Enable Register

Table 21 Interrupt Enable Register

PADDR[5:0]	Register Name	Type	Width	Reset Value	Description
0x10	QEI_IER	R/W	16	0x0000	Interrupt Enable Register

Table 22 Interrupt Enable Register Bit Definition

Bits	Name	Type	Description
15:3	–	–	Reserved
2	DIR_INT	R/W	Enable/Disable Direction of Rotation Interrupt (DIR_INT) 1 = Enables the Direction of Rotation Interrupt (DIR_INT) 0 = Disables the Direction of Rotation Interrupt (DIR_INT)
1	POS_INT	R/W	Enable/Disable Position Counter Interrupt (POS_INT) 1 = Enables Position Counter Interrupt (POS_INT) 0 = Disables Position Counter Interrupt (POS_INT)
0	VEL_INT	R/W	Enable/Disable Velocity Register Update (VEL_INT) 1 = Enables Velocity Register Update (VEL_INT) 0 = Disables Velocity Register Update (VEL_INT)

Status Register

Table 23 Interrupt Status Register

PADDR[5:0]	Register Name	Type	Width	Reset Value	Description
0x14	QEI_SR	R/W	16	0x0000	Status Register

Table 24 Interrupt Status Register Bit Definition

Bits	Name	Type	Description
15.5	–	–	Reserved
4	ERROR	R	QEI error bit 1 = Position counter overflow or underflow 0 = No overflow or underflow
3	UP/DOWN	R	Direction of Rotation Status bit 1 = Forward 0 = Reverse
2	DIR_INT	R/W	Direction of Rotation Interrupt (DIR_INT) 1 = Direction of rotation has changed. Must be cleared by writing a 1. 0 = Direction of rotation has not changed.
1	POS_INT	R/W	Position Counter Interrupt (POS_INT) 1 = The QEI position counter has reached the MAXCNT value or the index pulse, INDX, has been detected. Depends on the QEI operating mode enabled. Must be cleared by writing a '1'. 0 = The QEI position counter has not reached the MAXCNT value or the index pulse has not been detected.
0	VEL_INT	R/W	Velocity Register Update (VEL_INT) 1 = Velocity register updated. Must be cleared by writing a '1'. 0 = Velocity register not updated.

Timer Load Register

Table 25 Timer Load Register

PADDR[5:0]	Register Name	Type	Width	Reset Value	Description
0x18	QEI_TIMER_LOAD	R/W	16	0x0000	Timer Load Register. Load the time interval value for velocity.

APB Interface Timing

The APB interface is compliant with the AMBA specification. Figure 3 and Figure 4 depict typical write cycle and read cycle timing relationships relative to the system clock, PCLK.

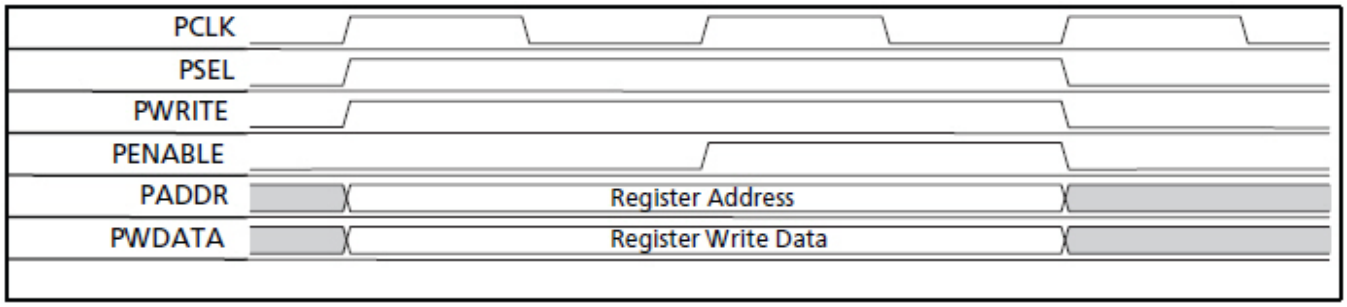

Figure 3 APB Data Write Cycle

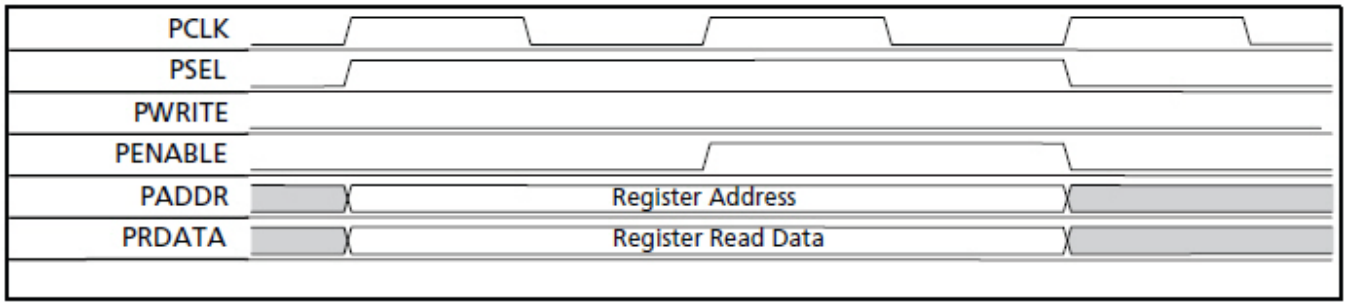

Figure 4 APB Data Read Cycle

QEI Internal Timing Diagram

Figure 5 shows that the x4 measurement mode provides for finer resolution data (more position counts) to determine the encoder position. Every rising and falling edge of the QEA and QEB signal generates a count_clk pulse and causes the position counter to increment or decrement.

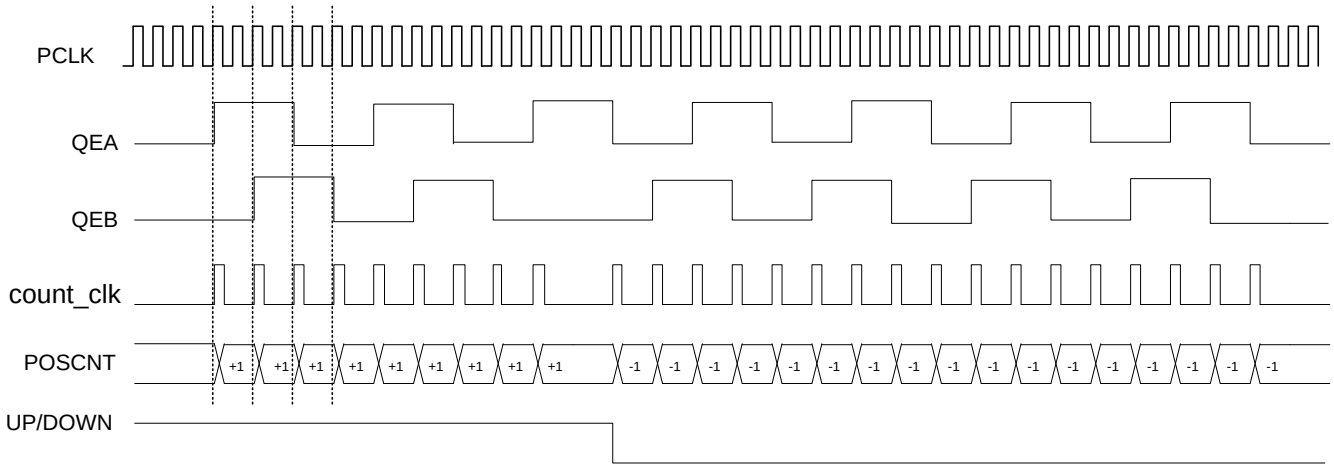

Figure 5 Quadrature Encoder Signals in x4 mode

Figure 6 shows that every rising and falling edge of the QEA signal generates a count_clk pulse and causes the position counter to increment or decrement in x2 mode. The QEB signal is still used to determine the counter direction, similar to the x4 measurement mode.

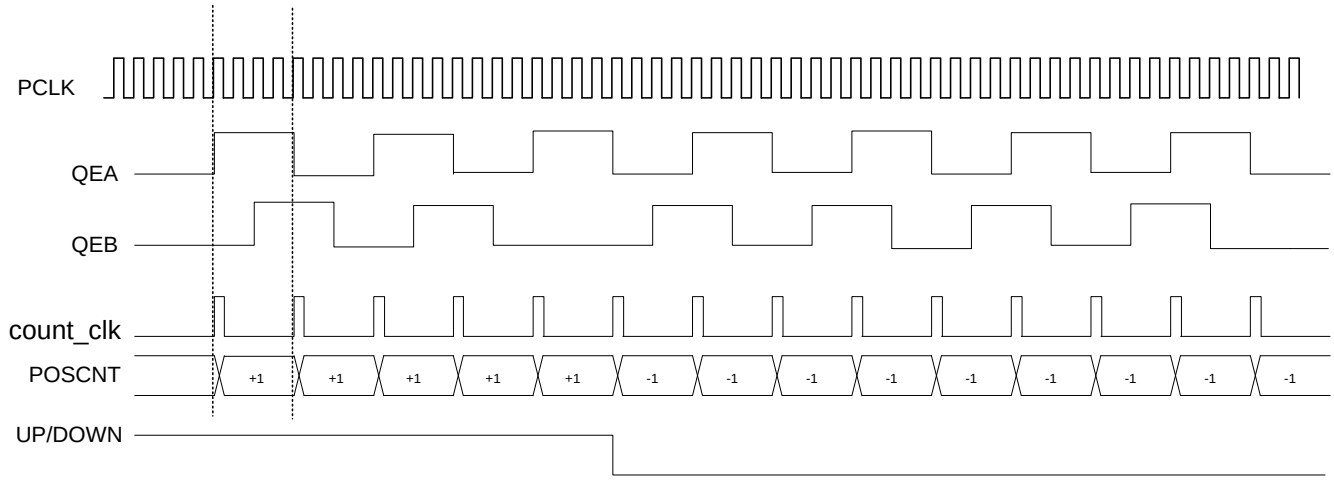

Figure 6 Quadrature Encoder Signals in x2 mode

Figure 7 shows the relationship between the incoming signal and the filtered output signal, where three consecutive clock pulses validate the input signal value. This example is the same for QEB and INDX signals.

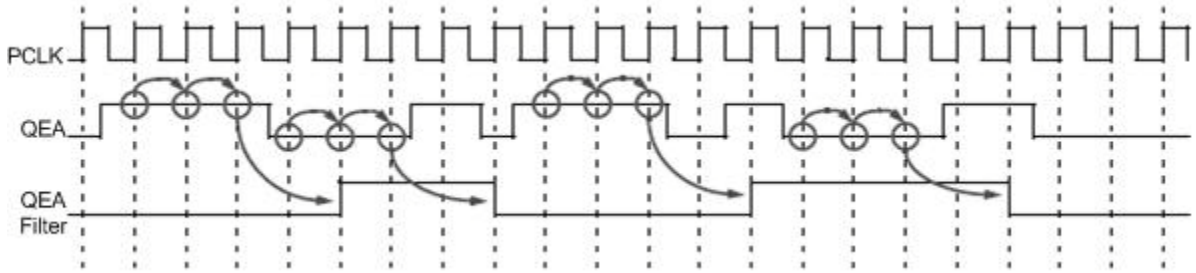

Figure 7 Input Signal Propagation through the Filter

Tool Flows

Licensing

CoreQEI is licensed in two ways – Obfuscated and RTL. Depending on your license tool flow, functionality may be limited.

Obfuscated

Complete RTL code is provided for the core, allowing the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed within Libero® Integrated Design Environment (IDE). The RTL code for the core is obfuscated[1] and some of the testbench source files are not provided; they are precompiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

SmartDesign

CoreQEI (Figure 8 on page 21) is preinstalled in the SmartDesign IP Deployment design environment. The core can be configured using the configuration GUI within SmartDesign (Figure 9 on page 22). For more information on using SmartDesign to instantiate and generate cores, refer to the *Using DirectCore in Libero IDE User's Guide*.

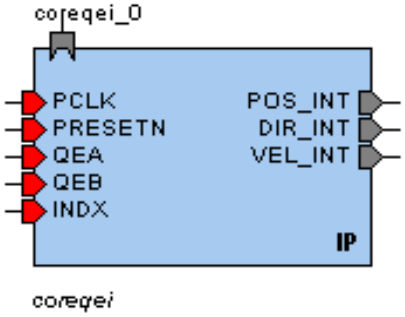

Figure 8 CoreQEI Full I/O View

[1] *Obfuscated means the RTL source files have had formatting and comments removed, and all instance and net names have been replaced with random character sequences.*

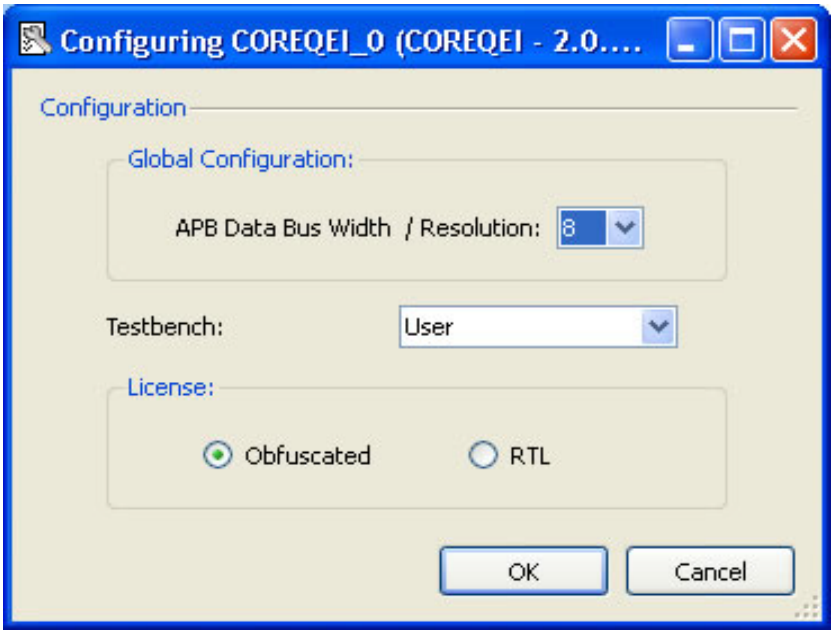

Figure 9 CoreQEI SmartDesign Configuration

Simulation Flows

The User Testbench for CoreQEI is included in all releases.

To run simulations, select the **User Testbench** flow within SmartDesign CoreQEI configuration GUI, right-click the canvas, and select **Generate Design**.

When SmartDesign generates the Libero IDE project, it installs the user testbench files.

To run the user testbench, set the design root to the CoreQEI instantiation in the Libero IDE design hierarchy pane and click the Simulation icon in the Libero IDE Design Flow window. This invokes ModelSim® and automatically runs the simulation.

User Testbench

A simplified block diagram of the User Testbench is shown in Figure 10. The user testbench instantiates the CoreQEI macro and provides a Register Write Stimulus process, Register Read process, and a QEI Output Check process.

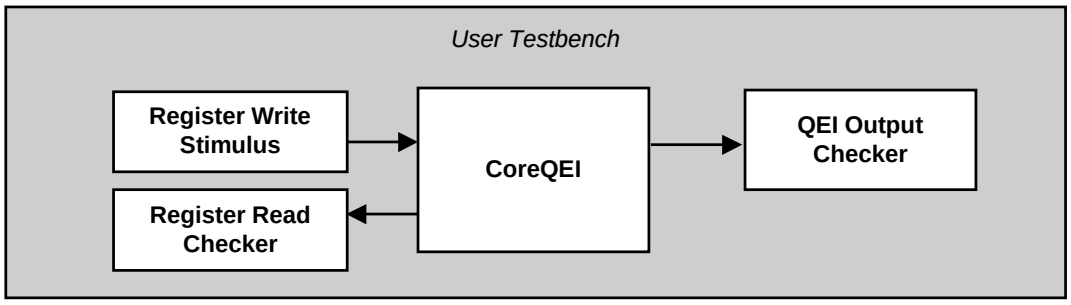

Figure 10 CoreQEI User Testbench

Synthesis in Libero IDE

After setting the design route appropriately for your design, click the **Synthesis** icon in Libero IDE. The Synthesis window appears, displaying the Synplify® project. Set Synplify to use the Verilog 2001 standard if Verilog is being used. To run Synthesis, select the **Run** icon.

Place-and-Route in Libero IDE

After setting the design route appropriately for your design, and running Synthesis, click the **Layout** icon in the Libero IDE to invoke the Designer. CoreQEI requires no special place-and-route settings.

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650. 318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (http://www.actel.com/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at http://www.actel.com/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure

to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/company/contact/default.aspx.

Actel is the leader in low power FPGAs and mixed signal FPGAs and offers the most comprehensive portfolio of system and power management solutions. Power Matters. Learn more at http://www.actel.com.

Actel Corporation *• 2061 Stierlin Court • Mountain View, CA 94043 • USA*
Phone 650.318.4200 • Fax 650.318.4600 • Customer Service: 650.318.1010 • Customer Applications Center: 800.262.1060

Actel Europe Ltd*. • River Court, Meadows Business Park • Station Approach, Blackwater • Camberley Surrey GU17 9AB • United Kingdom*
Phone +44 (0) 1276 609 300 • Fax +44 (0) 1276 607 540

Actel Japan *• EXOS Ebisu Building 4F • 1-24-14 Ebisu Shibuya-ku • Tokyo 150 • Japan*
Phone +81.03.3445.7671 • Fax +81.03.3445.7668 • http://jp.actel.com

Actel Hong Kong *• Room 2107, China Resources Building • 26 Harbour Road • Wanchai • Hong Kong*
Phone +852 2185 6460 • Fax +852 2185 6488 • www.actel.com.cn

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