

**RN0087**

**CoreQDR v3.3 Release Notes**



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a  **MICROCHIP** company



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# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 6.0

Updated changes related to CoreQDR v3.3.

## 1.2 Revision 5.0

Updated changes related to CoreQDR v3.2.

## 1.3 Revision 4.0

Updated changes related to CoreQDR v3.1.

## 1.4 Revision 3.0

Updated changes related to CoreQDR v3.0.

## 1.5 Revision 2.0

Updated changes related to CoreQDR v2.1.

## 1.6 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreQDR v2.0.

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## 2 CoreQDR v3.3 Release Notes

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### 2.1 Overview

These release notes accompany the production release of CoreQDR v3.3. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

### 2.2 Features

CoreQDR is a configurable memory controller for QDR static random access memory (SRAM) devices and has the following features:

- Supports QDR II Interface
  - Up to 666 MHz double data rate (333 MHz clock)
  - Separate read and write channels D (input) and Q (output), supporting concurrent transactions
  - Single address channel A
  - Burst of 2 and burst of 4 support (configurable)
- Configurable clock cycle latency
- Configurable QDR data width D/Q (8, 9, 18, and 36 bits)
- Two phase-locked loops (PLLs):
  - One to generate true write clock (K and K<sub>n</sub>)
  - One to generate 90 degree phase shifted clock from Echo (read) clock
- Two-Port FIFO's for clock synchronization / pipelining
  - Write Data Path
  - Read Data Path
  - Write Address Path
  - Read Address Path
- Configurable use of QVLD signal
  - When enabled, QVLD signal is used and there is no write-read clock crossing
  - When disabled (for QDR I / QDR II devices not supporting QVLD), CoreQDR generates an internal data valid signal

### 2.3 Delivery Types

CoreQDR requires a register transfer level (RTL) license to be used and instantiated. Complete source code is provided for the core.

### 2.4 Supported Families

- RTG4™
- SmartFusion®2

### 2.5 Supported Tool Flows

CoreQDR v3.3 requires Libero® System-on-Chip (SoC) v11.5 or later.

### 2.6 Installation Instructions

For the RTL version of the core, the FlexLM® license must be installed before the core can be exported. Consult Libero SoC online help for the instructions on core installation and licensing.

Refer to the [Libero SoC Online Help](#) for further instructions on core installation, licensing, and general use.

## 2.7 Documentation

This release contains a copy of the *CoreQDR Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Liberio SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

<http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>.

## 2.8 Supported Test Environments

- Verilog user testbench

## 2.9 Resolved History

Table 1 lists the release history for CoreQDR.

**Table 1 • Release History**

| Version | Date         | Changes  |
|---------|--------------|--|
| 3.3     | March 2019   | <ul style="list-style-type: none"> <li>• Added support for x36 mode</li> <li>• Packaging port size fixes (address bus size, remove SYSCLK)</li> <li>• Handbook updates (remove WSTRB functionality, remove SYSCLK, Q_EDGE descriptor)</li> </ul>   |
| 3.2     | April 2017   | <ul style="list-style-type: none"> <li>• License Lock feature included</li> </ul>  |
| 3.1     | June 2015    | <ul style="list-style-type: none"> <li>• Added RTG4 Support</li> <li>• Regenerated and added CoreFIFO with RTG4 support</li> <li>• Added synchronous reset</li> <li>• Updated Handbook with additional information about CLK_READY signal, as well as RTG4 utilization data</li> </ul>   |
| 3.0     | October 2014 | <ul style="list-style-type: none"> <li>• Removed CL parameter, replacing it with Q_EDGE and LAT_SEL[2:0] configuration ports</li> <li>• Removed TX CCC from CoreQDR, added input ports for external clocks instead</li> <li>• Added support for QVLD, with a top-level parameter USE_QVALID that enables / disables its operation</li> <li>• Modified read data path by doubling Read FIFO write port clock frequency, simplifying timing closure</li> </ul> |
| 2.1     | August 2013  | Pipelining for improved performance, bug fixes related to clock conditioning circuit (CCC) functional model in ModelSim, read data CCC no longer uses dedicated differential PAD input (uses fabric input)   |
| 2.0     | March 2013   | Initial release.   |

## 2.9.1 Resolved Issues in the v3.3 Release

**Table 2 • Resolved Issues in the v3.3 Release**

| SAR Number | Changes                                       |
|------------|---|
| 101506     | Add support for x36.                          |
| 65026      | Ported one register from async to sync reset. |
| 66156      | Removed SYSCLK.                               |
| 72775      | Updated Q_EDGE description in Handbook.       |
| 80593      | Removed WSTRB from Handbook.                  |
| 85426      | Added packaging width to address bus.         |

## 2.9.2 Resolved Issues in the v3.2 Release

**Table 3 • Resolved Issues in the v3.2 Release**

| SAR Number | Changes  |
|------------|--|
| 87624      | CoreQDR: License Lock update as per marketing requirement. |

## 2.9.3 Resolved Issues in the v2.1 Release

**Table 4 • Resolved Issues in the v2.1 Release**

| SAR Number              | Changes  |
|-------------------------|--|
| 43637                   | User interface timing is incorrect.  |
| 43638<br>43960<br>43961 | Read data packing into user clock domain is out of order.                          |
| 46185                   | (Enhancement) Add 2.5 clock latency option to CL parameter.                        |
| 47091                   | (Enhancement) Add pipeline stage after address incrementer to improve performance. |
| 47209                   | (Enhancement) Add pipeline stage after address mux to improve performance.         |
| 46249                   | Fix incorrect phase setting for read data CCC (PLL).                               |

## 2.10 Discontinued Features and Devices

There are no discontinued features and devices in CoreQDR v3.3.

## 2.11 Known Limitations and Workarounds

Following are the known limitations.

- Timing closure is difficult to achieve for QDR II+ devices operating at clock rates higher than 333 MHz.
- Timing closure is difficult to achieve for QDR II/II+ devices operating higher than 200 MHz in RTG4.
- This IP does not support x36 mode for SmartFusion2.