RN0061
Release Notes
CoreMemCtrl v2.2

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 8.0

Added support for PolarFire SoC and PolarFire.

1.2 Revision 7.0

Added support for IGLOO2, SmartFusion2, and RTG4.

1.3 Revision 6.0

The following is a summary of the changes made in this revision.

- Changed from using two AHB slave interfaces (with a shared set of AHB inputs) to only using a single AHB slave interface. CoreMemCtrl v2.0 only consumes a single slave slot on CoreAHB or CoreAHBLite, as opposed to the two slots used by previous versions of the core.
- Two new configurable options have been added to provide control over the address bus connections to external memory devices. The corresponding RTL parameters/generics for these options are FLASH_ADDR_SEL and SRAM_ADDR_SEL.
- A new REMAP input port has been added. When REMAP is asserted High, the locations of flash and SRAM are swapped in the address space.

Note: CoreMemCtrl v2.0 is not pin compatible with previous versions of CoreMemCtrl.

1.4 Revision 5.0

Read data path simplified to ensure that (falling edge clocked) multi-cycle paths are not treated as half cycle paths when analyzing timing using SmartTime.Depending on system configuration, an increase in the maximum operating frequency may also be observed.

1.5 Revision 4.0

Added support for IGLOO and IGLOOe devices.

1.6 Revision 3.0

Added FLOW_THROUGH parameter. This parameter is only applicable to synchronous SRAM and allows CoreMemCtrl to control SSRAM devices which are configured to operate in flow-through or pipeline mode.

1.7 Revision 2.0

Added SHARED_RW parameter, which is set to 1 when the common read and write signals (MemReadN and MemWriteN) are connected to the external SRAM and flash devices.

1.8 Revision 1.0

First production release.

Contents

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2 CoreMemCtrl v2.2

This is the production release for the CoreMemCtrl IP core. These release notes describe the features and enhancements for CoreMemCtrl v2.2. These release notes also contain known information about system requirements, supported families, implementations, and known issues and workarounds.

2.1 Intended Use

CoreMemCtrl provides an advanced microcontroller bus architecture (AMBA) advanced high-performance bus (AHB) interface to external SRAM and flash memory devices. CoreMemCtrl v2.2 has only a single AHB interface. The core has several configuration parameters, which allow different types of memories to be supported. For example, CoreMemCtrl can interface to either synchronous or asynchronous SRAM devices.

2.2 Key Features

The following are the key features of CoreMemCtrl:

- Provides an AHB slave interface to external memory devices.
- Configurable external memory interface, up to 4 chip select for sync/async SRAM.
- Interfaces to external flash and either synchronous or asynchronous external SRAM.
- Supports 32-bit word, 16-bit halfword, and 8-bit byte accesses to SRAM.
- Supports 32-bit word, 16-bit halfword, and 8-bit byte accesses to flash.
- The locations of flash and SRAM in the address space can be swapped by asserting the REMAP input.

2.3 Supported Interface

CoreMemCtrl has an AMBA AHB slave interface for connection to AHB or AHB-Lite systems. Typically, the AHB slave interface of CoreMemCtrl will be connected to one of the slave slots of CoreAHB or CoreAHBLite. The ports of CoreMemCtrl that connect to external flash and SRAM together make up the external memory interface.

2.4 Delivery Types

CoreMemCtrl is delivered with unobfuscated RTL.

2.4.1 RTL

Complete Verilog and VHDL RTL source code is provided for the core and testbenches.

2.5 Supported Families

The following families are supported in this version:

- PolarFire® SoC
- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2
- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3E
- ProASIC3L
- SmartFusion
- ProASICPLUS®
- Fusion
- RTAX-S
- RTSX-S
- EX
- AX

2.6 Supported Tool Flows

- CoreMemCtrl v2.2 requires the Libero® software v8.6 or later.
- Supports Windows® and Linux operating systems.

2.7 Installation Instructions

The CoreMemCtrl CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project. Refer to the *Libero SoC Online Help* for instructions on core installation, licensing, and general use.

To know how to create SmartDesign project using the IP cores, refer to the *SmartDesign User guide.*

2.8 Documentation

This release contains a copy of the *CoreMemCtrl Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also suggests implementation changes. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.9 Resolved Issues in the v2.2 Release

Table 1 shows SARs resolved in the v2.2 release of CoreMemCtrl.

Table 1 • **Resolved SARs in CoreMemCtrl v2.2**

SAR Number	Description
14387	Added mux logic to the Address output for flash device.
64652	Fixed MEMADDR generation issue for write transaction to 16bit FLASH device followed by a transaction to SRAM.
66664	Added minimum Libero version support to 8.6.

Table 1 • **Resolved SARs in CoreMemCtrl v2.2**

SAR Number	Description
68813	Fixed AHB Byte write transaction to Flash.

2.10 Resolved Issues in the v2.1 Release

Table 2 shows SARs resolved in the v2.1 release of CoreMemCtrl.

Table 2 • **Resolved SARs in CoreMemCtrl v2.1**

SAR Number	Description
57873	Added wait states to extend wait capability.
18144	Fixed SPIRIT description to allow for Memory Map generation.

2.11 Resolved Issues in the v2.0 Release

Table 3 shows SARs resolved in the v2.0 release of CoreMemCtrl.

Table 3 • **Resolved SARs in CoreMemCtrl v2.0**

SAR Number	Description
14249	CoreMemCtrl is now suitable for use in multi-master systems. This is made possible by the use of a single AHB slave interface. Previous versions of the core that used two AHB slave slots assumed that only a single master would address both slots.
14250	Configurability of external address bus connections is now provided. This provides more flexibility when interfacing to external memories and is of particular use when connecting to flash memory. Flash devices from different manufacturers use different approaches to addressing.

2.12 Resolved Issues in the v1.5 Release

Table 4 shows SARs resolved in the v1.5 release of CoreMemCtrl.

Table 4 • **Resolved SARs in CoreMemCtrl v1.5**

SAR Number	Description
13511	Read data path has been simplified to improve reported system performance.

Note: There are no specific bug fixes in the v1.5 release. CoreMemCtrl v1.5 improves on v1.4 by simplifying the path for read data from the core to the bus and ultimately to the processor. This simplification means that any CoreMemCtrl related timing paths identified by SmartTime should be easier to understand and may also give an increase in the maximum system frequency, depending on the system configuration.

2.13 Known Limitations and Workarounds

There are no known limitations or workarounds in the CoreMemCtrl v2.2 release.