CoreMACFilter v2.0

Handbook

Microsemi

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Introduction

Core Overview

CoreMACFilter provides a solution for SmartFusion®2 and IGLOO®2 integrated media access control (MAC) address filtering. The core provides the external filtering mechanism based on unicast (UCAD) / multicast (MCAD) / broadcast (BCAD) flags. It implements the desired mechanism to pass the frames to upper layer, so that, upper layer determines to reject or accept the frames. In case of the CoreMACFilter usage ten-bit interface (TBI) to external physical coding sublayer (EPCS) core need not to be used.

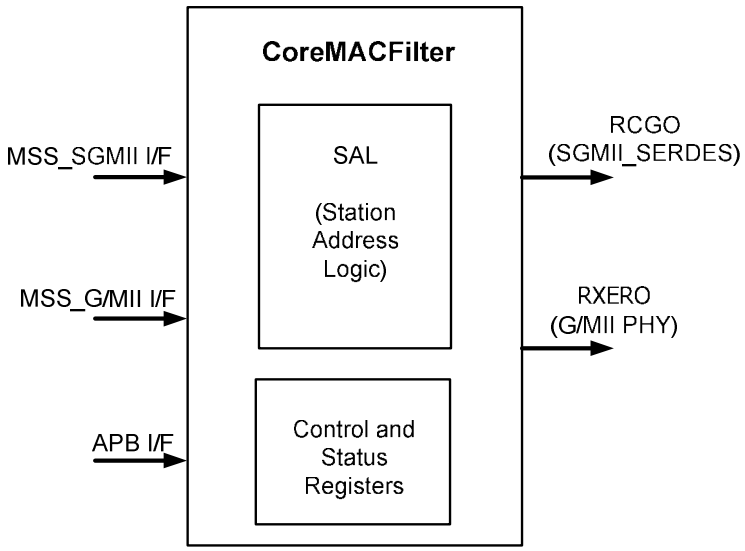

Figure 1 · Top-Functional Block Diagram

Core Version

This handbook applies to CoreMACFilter version 2.0.

Supported Families

- SmartFusion2
- IGLOO2

Key Features

The following key features are supported in CoreMAC Filter module:

- Provides advanced peripheral bus (APB) interface for control and status register access
- Supports unicast, multicast, and broadcast type of packets
- Supports hash based address filtering for unicast and multicast packets
- Provides mechanism to the upper layer to reject or accept the frames

Utilization and Performance

Table 1 summarizes the CoreMACFilter device utilization.

Table 1 CoreMACFilter Device Utilization

FPGA Family and Device	Parameter	Logic Elements			Utilization %
	GMII_SGMII	Comb	Sequential	Total	
SmartFusion2 M2S150T	1	1,779	788	2,567	1.7%
SmartFusion2 M2S150T	0	761	399	1,160	0.7%
IGLOO2 M2GL050T	1	1,800	788	2,588	4.6%
IGLOO2 M2GL050T	0	759	399	1,158	2%

Functional Description

Functional Overview

CoreMACFilter provides a mechanism to filter the frames based on the filtering configuration provided in Table 2.

The CoreMACFilter performs filtering out frames (unwanted frames) based on a combination of local base station MAC address, multicast, broadcast, hash-unicast, hash-multicast of filter operating modes. A 128-bit hash table is used for hash-unicast and hash-multicast frame filtering. The frame filtering is performed on the destination MAC address of the received frame. CoreMACFilter has an APB interface to allow address filtering configurations and other MAC configurations.

Table 2 CoreMACFilter Register Map

ADDR	Register
40h	Frame pass controls
44h	Hash Table Register0
48h	Hash Table Register1
4Ch	Hash Table Register2
50h	Hash Table Register3
54h	Misc Control register
58h	Frame drop counter.
5Ch	Station Address Lower Register
60h	Station Address Higher Register

Register Descriptions

Table 3 Register Descriptions

Address[9:0]	Function
0x40	**Frame pass controls – Default 0x0000_003F** [31:6] Reserved [5] (W/R) pass the frame if the hash table entry matches for Multicast-DA [4] (W/R) pass the frame if hash table entry matches for Unicast-DA [3] (W/R) Promiscuous mode. Allow all the frames to pass [2] (W/R) pass the frame if it is Unicast-DA matches the configured-DA [1] Pass all multicast frames [0] Pass all broadcast frames
0x44	**Hash Table Register0: Hash Entries-[31:0] - Default 0x0000**
0x48	**Hash Table Register1: Hash Entries-[63:32] - Default 0x0000**

Address[9:0]	Function
0x4C	**Hash Table Register2: Hash Entries-[95:64] - Default 0x0000**
0x50	**Hash Table Register3: Hash Entries-[127:96] - Default 0x0000**
0x54	**Misc Control register** [31:11] Reserved [10:3] (R/W) MINIMUM IFG ENFORCEMENT: Default 0x50 This programmable field represents the minimum size of inter-frame gap (IFG) to enforce between frames (expressed in bit times). A frame whose IFG is less than that programmed is dropped. The default setting of 0x50 (80d) represents half of the nominal minimum IFG which is 160 bits. *Note: Value of this field must be same as the value of minimum IFG field (bit 15:8) of IFG / interpacket gap (IPG) register of MAC core* [2] (W/R) FULL-DUPLEX: Default 1 Setting this bit configures the MAC to operate in Full-Duplex mode. Clearing this bit configures the MAC to operate in Half-Duplex mode. *Note: Value of this field must be same as the value of FULL-DUPLEX field (bit 0) of MAC Configuration #2 register]* [1:0] (W/R) INTERFACE MODE: Default 0x 10 This field determines the type of interface the MAC is connected to and accordingly behaves at PHY interface 2'b00: MAC Tx/Rx represents media independent interface (MII) 10 Mbps interface (Nibble Mode) 2'b01: MAC Tx/Rx represents MII 100 Mbps interface (Nibble Mode) 2'b10: MAC Tx/Rx represents gigabit MII (G/MII) 1000 Mbps interface (Byte Mode) 2'b11: Reserved ***Note:*** *Value of this field must be same as the value of INTERFACE MODE field (bit 9:8) of MAC Configuration #2 register of MAC core*
0x58	**Frame drop counter.** This is 32-bit roll over counter, incremented for each frame dropped by this filter logic.
0x5C	**Station Address Lower Register - Default 0x3C88_8888** [31:24] (W/R) First octet of the DA in the frame: Station Address[7:0] [23:16] (W/R) Second octet of the DA in the frame: Station Address[15:8] [15: 8] (W/R) Third octet of the DA in the frame: Station Address[23:16] [7: 0] (W/R) Fourth octet of the DA in the frame: Station Address[31:24]
0x60	**Station Address Higher Register Default 0xC0B1_0000** [31:24] (W/R) Fifth octet of the DA in the frame: Station Address[39:32] [23:16] (W/R) Sixth octet of the DA in the frame: Station Address[47:40] [15:0] Reserved

Tool Flows

Licenses

CoreMACFilter requires a register transfer level (RTL) license to be used and instantiated. Microsemi® provides the complete source code for the core.

SmartDesign

CoreMACFilter is available for download in the Libero® System-on-Chip (SoC) IP catalog through the web repository. Once it is listed in the catalog, the core can be instantiated using the SmartDesign flow. For information on using SmartDesign to configure, connect, and generate cores, refer to the Libero online help. Figure 2 shows an example instantiated view.

The CoreMACFilter can be instantiated as a component of a larger design. CoreMACFilter is compatible with both Libero integrated design environment (IDE) and Libero SoC. Unless specified otherwise this document uses the common name Libero to identify Libero IDE and Libero SoC.

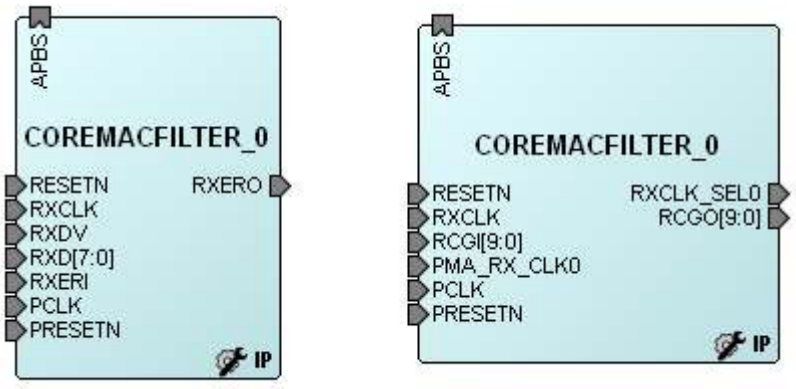

Figure 2 SmartDesign CoreMACFilter Instance View

Simulation Flows

Unit level simulation is not supported for CoreMACFilter.

Synthesis in Libero

To run synthesis on the CoreMACFilter, set the design root to the IP component instance and run the synthesis tool from the Libero design flow pane.

Place-and-Route in Libero

After the design is synthesized, run the compilation and then place-and-route the tools. CoreMACFilter requires no special place-and-route settings.

Interface Descriptions

Ports

The port signals for CoreMACFilter are described in Table 4 on page 9 and shown in Figure 3.

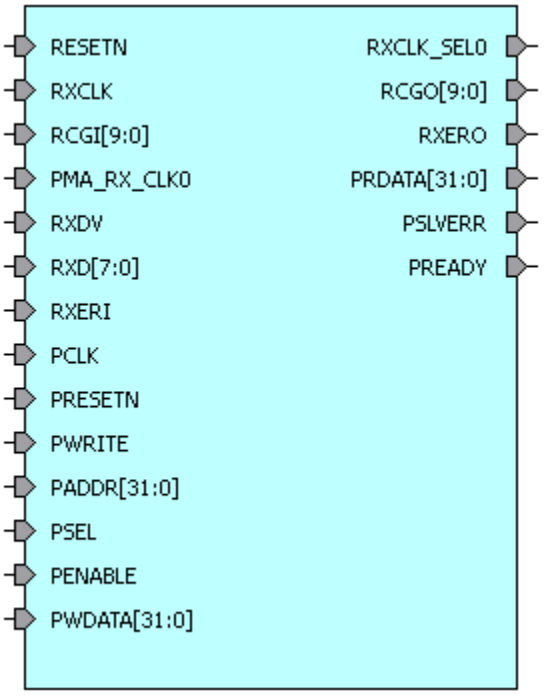

Figure 3 CoreMACFilter I/O Signals

Table 4 · I/O Signal Description

Signal	Direction	Description
Clock-reset		
RESETN	Input	Active Low reset
RXCLK	Input	G/MII Mode – 125/25/2.5 MHz clock for 1000/100/10 respectively SGMII Mode – 125 MHZ for 1000 mbps and 25 MHZ clock for 100/10 mbps
G/MII interface		
RXD[7:0]	Input	G/MII Receive data
RXDV	Input	G/MII Receive data valid
RXERI	Input	G/MII Receive Error input
RXERO	Output	G/MII Receive Error output (After address based filtering)
SGMII Interface		
RCGI[9:0]	Input	TBI Receive code group input
RCGO[9:0]	Output	TBI Receive code group output (After address based filtering)
PMA_RX_CLK0	Input	PMA Receive Clock phase-0 @ 62.5 MHz
APB Interface		
PCLK	Input	APB System Clock: reference clock for all internal logic
PRESETN	Input	APB active-low asynchronous reset
PADDR[31:0]	Input	APB address bus
PSEL	Input	APB Slave Select
PENABLE	Input	APB Enable
PWRITE	Input	0: APB Read 1: APB Write
PWDATA[31:0]	Input	APB write data
PRDATA[31:0]	Output	APB read data
PSLVERR	Output	APB error signal to indicate the failure of transfer
PREADY	Output	APB ready signal to indicate completion of transfer
Other Interface Signals		
RXCLK_SEL0	Output	Clock Selection (INTERFACE MODE bit field of Misc register, 54h)

Configuration Parameters

CoreMACFilter generates the RTL code based on parameters set by the user. CoreMACFilter supports below configurable parameters specified in Table 5. Figure 4 shows the **Configuration** window of the CoreMACFilter.

Table 5 · CoreMACFilter Configuration Parameters

Name	Valid Values	Description
GMII_SGMII	0/1	0: G/MII mode of operation 1: SGMII mode of operation

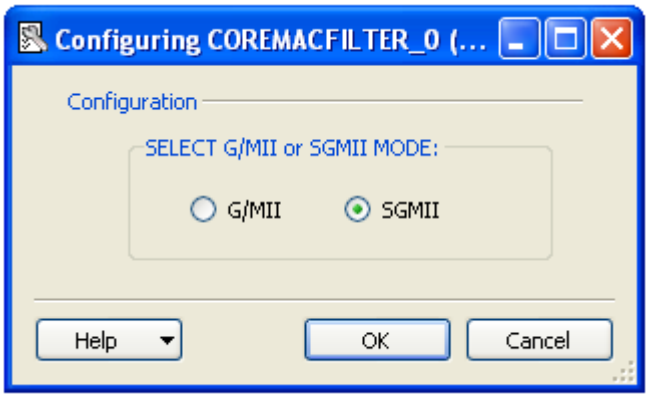

Figure 4 CoreMACFilter Configuration Window

Test-bench Operation and Modification

CoreMACFilter is not packaged with unit level test bench. CoreMACFilter is a workaround solution for integrated MAC address filtering issue and functionality is validated on SmartFusion2 development board.

System Operation

This section provides hints to ease the integration of CoreMACFilter.

The SmartFusion2 microcontroller subsystem (MSS) has an instance of the triple speed MAC (SmartFusion2 MSS MAC). CoreMACFilter hardware soft IP core is to be used with the SmartFusion2 MSS MAC. To create a design using MSS, SmartDesign should be used. CoreMACFilter must be used in the receive data path of the SmartFusion2 MSS MAC.

The SmartFusion2 MSS MAC can be connected to SGMII PHY interface by configuring it for the TBI operation. The TBI is routed through the FPGA fabric onto the SERDES I/Os. The SERDES SGMII interface will in turn communicate with the SGMII PHY. CoreMACFilter is integrated between the TSEMAC TBI interface and SERDES. For more information on the SmartFusion2 MSS MAC TBI interface, refer to the *SmartFusion2 Microcontroller Subsystem User Guide*.

Figure 5 shows the SmartFusion2 MSS MAC design with integrated CoreMACFilter and SERDES which interacts with the onboard SGMII PHY.

Transmit data path:

TBI_TCGF[9:0] (MSS Ethernet MAC) to SGMII_TX_DATA[9:0] (SERDES)

Receive data path:

SGMII_RX_DATA [9:0] (SERDES) to RCGI [9:0] (CoreMACFilter)

RCGO[9:0] (CoreMACFilter) To TBI_RCGF[9:0] (MSS Ethernet MAC)

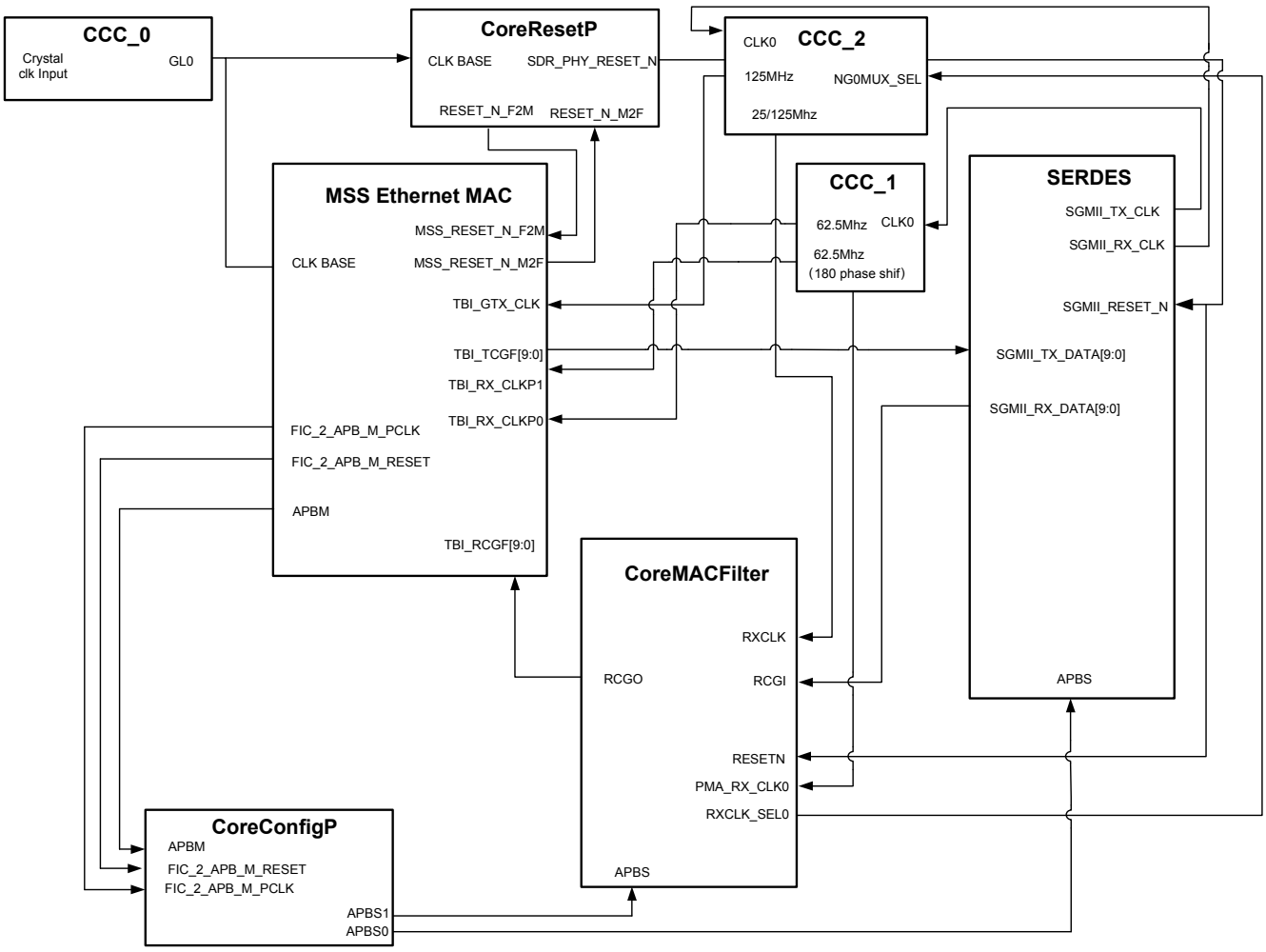

Figure 5 System Level integration example of CoreMACFilter in SGMII Mode

Figure 6 shows that the SmartFusion2 MSS MAC can be connected to GMII PHY interface by configuring it for the GMII interface operation. CoreMACFilter is integrated between the TSEMAC G/MII interface and the G/MII PHY.

Transmit data path: MAC_GMII_TXD [7:0] (MSS Ethernet MAC) to Ethernet PHY

Receive data path: Ethernet PHY to MAC_GMII_RXD [7:0] (MSS Ethernet MAC)

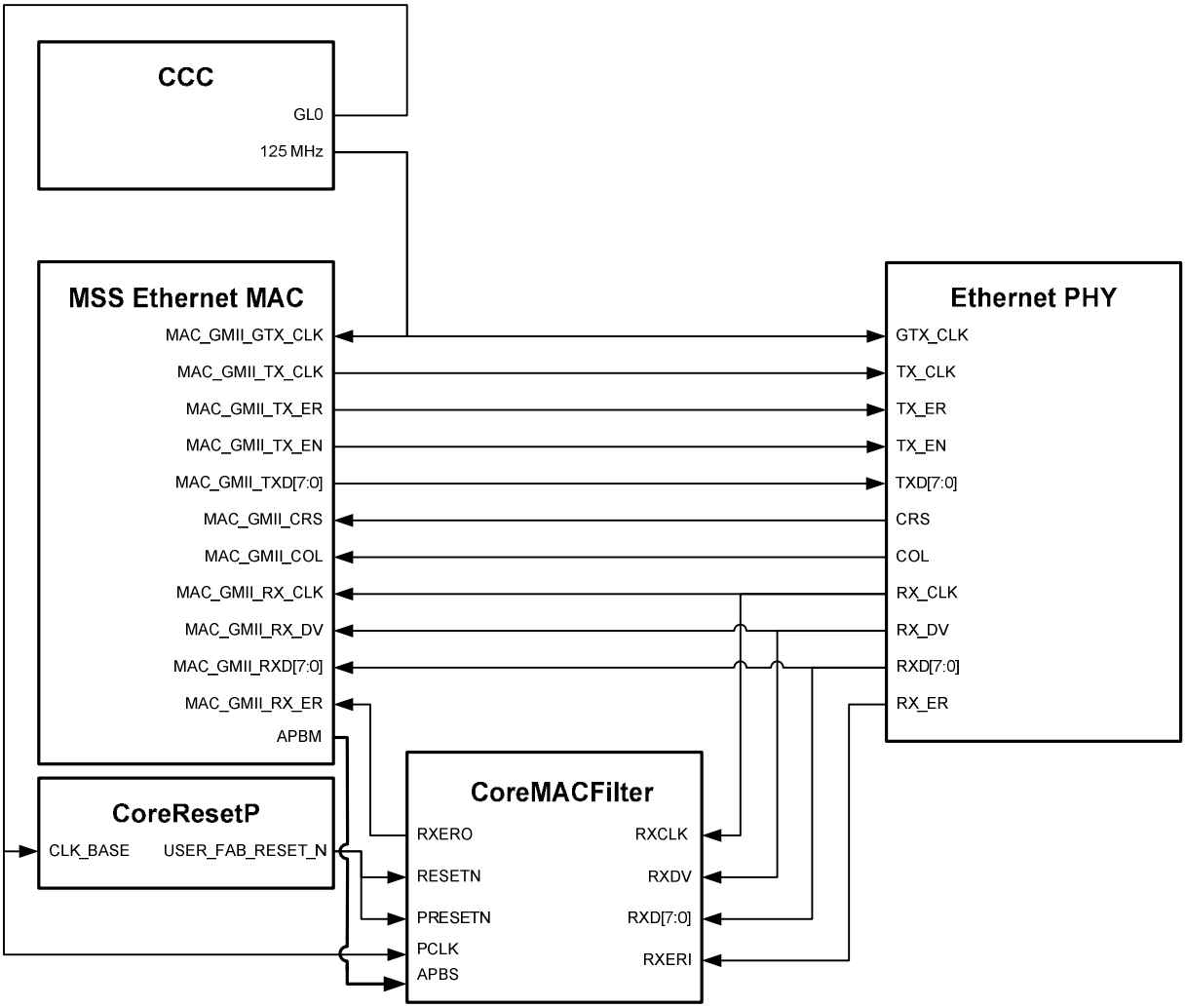

Figure 6 System Level integration example of CoreMACFilter (G/MII Mode)

Ordering Information

Ordering Codes

CoreMACFilter can be ordered through the local sales representatives by using the following number scheme: CoreMACFilter-XX, where XX is listed in Table 6.

Table 6 · Ordering Codes

XX	Description
RM	RTL for RTL source — multi-use license

List of Changes

The following table lists the critical changes that were made in each revision of the document.

Date	Change	Page
July 2014	Initial Release	N/A

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Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

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Website

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