CoreLPC v3.2 Release Notes

This is the production release for CoreLPC. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

Intended Use

CoreLPC is a low pin count (LPC) peripheral APB component which accepts LPC host-side system interface commands to the APB-slave side keyboard control style (KCS) interface. Alternatively, LPC traffic can be sent directly to/from other APB peripherals via an APB Master interface. Serial interrupt request (SERIRQ) logic can be utilized to aggregate interrupts onto a single line.

Key Features

- Support for LPC interface as governed by the LPC specification revision 1.1
- I/O read/write LPC cycle types
- Support for the KCS protocol over the LPC interface, as described in the IPMI specification v2.0
- Programmable SERIRQ slot interface
- LPC controller enabling/disabling by software
- Configurable base address for KCS registers
- Configurable base address and range for master port peripherals
- APB3 compliant

Supported Interfaces

CoreLPC is available with the following interfaces:

- LPC peripheral to host-side
- Serial interrupt request interface
- APB Slave interface
- APB Master port interface

Delivery Types

CoreLPC is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero® Integrated Design Environment (IDE). The RTL code for the core is obfuscated, and some of the testbench source files are not provided. They are precompiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3E
- ProASIC3L
- SmartFusion™
- Fusion
- ProASICPLUS®
- Axcelerator®
- RTAX-S

Supported Tool Flows

CoreLPC requires SmartDesign and Microsemi Libero IDE v8.6 or later.

Installation Instructions

The CoreLPC CCZ file must be installed into Libero IDE. This is done automatically via the Catalog update function in Libero IDE or the CCZ file can be manually added using the **Add Core catalog** feature.

Once installed in the Libero IDE Catalog, the core can be instantiated and configured. For RTL and obfuscated versions of the core, the FlexLM license must be installed before the core is exported.

Refer to the Libero IDE online help for further instructions on core installation, licensing, and general use.

Documentation

The release contains a copy of the CoreLPC Handbook. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, as well as implementation suggestions. For updates and additional information about the software, devices, and hardware visit the Intellectual Property pages on the Microsemi website at http://www.microsemi.com.

Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

Discontinued Features and Devices

KCS SerIRQ slot selection was soft-programmable and is now configured via parameters.

New Features and Devices

- Added APB master port interface.

Known Limitations and Workarounds

There are no known limitations or workarounds with the CoreLPC v3.2 release.

Release History

Version	Date	Changes
3.2	March 2012	Various issues resolved as listed below.
3.1	June 2010	Various issues resolved as listed below.
3.0	April 2010	Various issues resolved as listed below.
2.0	August 2009	First production release

Resolved Issues in the v3.2 Release

Table 1 Resolved SARs in CoreLPC v3.2 Release

SAR	Description
36585	Erratic clearing of KOBF flag
35066	Core LPC: Synthesis failed for VHDL flow

Resolved Issues in the v3.1 Release

Table 2 Resolved SARs in CoreLPC v3.1 Release

SAR	Description
26495	Parameter typo in GUI configurator for the "Enable Master Port IRQ" setting

Resolved Issues in the v3.0 Release

Table 3 Resolved SARs in CoreLPC v3.0 Release

SAR	Description
21909	Allow LPC host direct access to peripherals via Master APB Port.