CoreLPC v3.2

Handbook

Microsemi

Table of Contents

Introduction

CoreLPC is a low pin count (LPC) peripheral APB component which accepts LPC host-side system interface commands to the APB-slave side keyboard control style (KCS) interface. Alternatively, LPC traffic can be sent directly to/from other APB peripherals via an APB Master Interface. Serial interrupt request (SERIRQ) logic may be utilized to aggregate interrupts onto a single line.

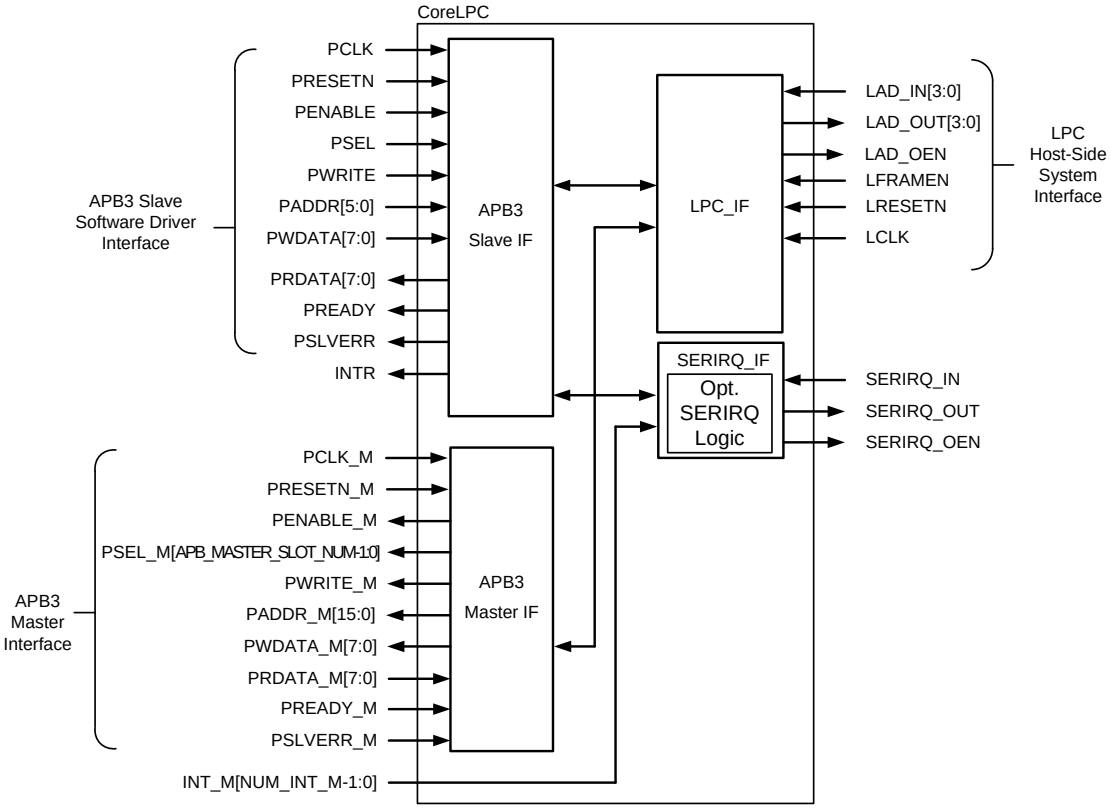


Figure 1 CoreLPC I/O Signal Diagram

CoreLPC example application is shown in Figure 2. CoreLPC is configured from the APB Slave bus controller (for example, Cortex™ -M1). The LPC FSM directs transactions from the LPC-side interface to either the KCS interface or the APB Master Interface that contains two Core16550s. All interrupts are mapped to the SERIRQ interface. Resynchronization occurs between the APB slave clock domain (PCLK) and the LPC clock domain (LCLK), as well as between APB master clock domain (PCLK_M) and the LPC clock domain (LCLK).

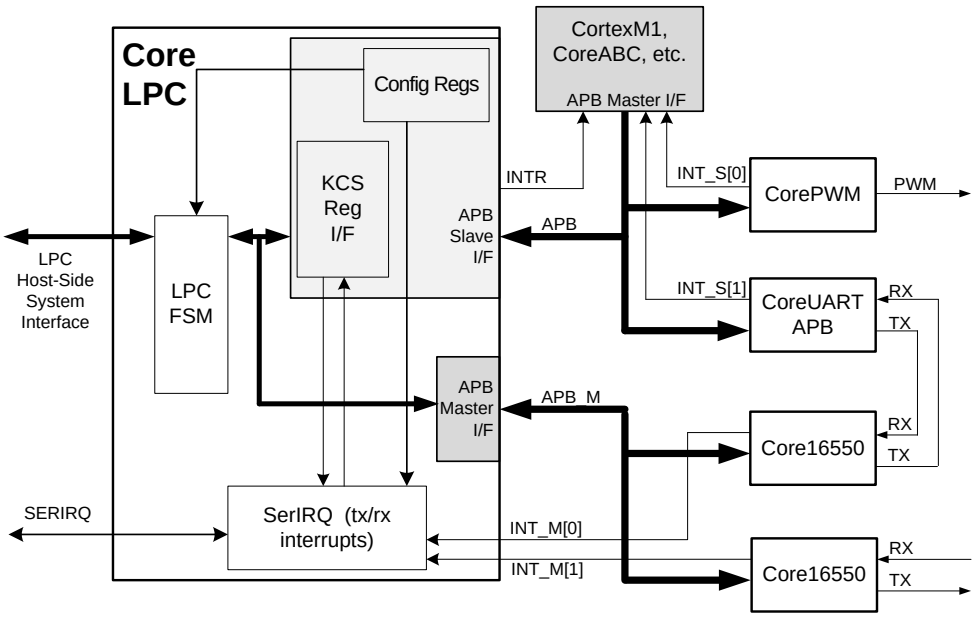


Figure 2 CoreLPC Example Application

Key Features

- Support for LPC interface as governed by the Intel® Low Pin Count Interface Specification Revision 1.1 (Microsemi is an Intel LPC adopter)
- I/O read/write LPC cycle types
- Support for the KCS protocol over the LPC interface, as described in the IPMI specification v2.0
- Programmable SERIRQ slot interface
- LPC controller enabling/disabling by software
- Configurable base address for KCS registers
- Configurable base address and range for master port peripherals
- APB3 compliant

Core Version

This handbook supports CoreLPC version 3.2.

Supported Interfaces

CoreLPC is available with the following interfaces:

- LPC peripheral to host-side
- SERIRQ interface
- APB Slave Interface
- APB Master port Interface

Supported Families

- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3E
- ProASIC3L
- SmartFusion™
- Fusion
- ProASICPLUS®
- Axcelerator®
- RTAX-S

Utilization and Performance

All Microsemi families and devices are supported. CoreLPC has been implemented in several Microsemi device families using standard speed grades. A summary of various implementation data is listed in Table 1 through Table 3.

Table 1 CoreLPC Device Utilization and Performance (KCS enabled with SERIRQ Interface Disabled Configuration)

Family	Tiles			Utilization		Performance, PCLK MHz	
	Sequential	Combinatorial	Total	Device	Total %	PCLK	LCLK
Fusion/SmartFusion™	77	248	325	AFS600	2.3	>100	98
IGLOO®/e	77	248	325	AGLE600V2	2.3	>100	41
ProASIC®3/E	77	248	325	M1A3P250	5.2	>100	>100
ProASIC PLUS®	78	247	325	APA075	10.6	>100	58
Axcelerator®	82	107	189	AX250	4.5	>100	>100
RTAX-S	82	107	189	RTAX250S	4.5	>100	>100

Note: Data in this table was achieved using typical synthesis and layout settings. Top-level parameters/generics were left at their default values.

Table 2 CoreLPC Device Utilization and Performance (KCS enabled with SERIRQ Interface Enabled Configuration)

Family	Tiles			Utilization		Performance, PCLK MHz	
	Sequential	Combinatorial	Total	Device	Total %	PCLK	LCLK
Fusion/SmartFusion	92	269	361	AFS600	2.6	>100	>100
IGLOO/e	92	269	361	AGLE600V2	2.6	>100	41
ProASIC3/E	92	269	361	M1A3P250	5.9	>100	>100
ProASIC PLUS	94	307	401	APA075	13.1	>100	63
Axcelerator	101	150	251	AX250	5.9	>100	>100
RTAX-S	101	150	251	RTAX250S	5.9	>100	>100

Note: Data in this table was achieved using typical synthesis and layout settings. Top-level parameters/generics were changed from their default value as follows: SERIRQ_EN = 1, SER_KIRQ_EN = 1, SER_KIRQ_SEL = 3.

Table 3 CoreLPC Device Utilization and Performance (KCS, SERIRQ, and 2 Master Port slots Enabled Configuration)

Family	Tiles			Utilization		Performance, PCLK MHz		
	Sequential	Combinatorial	Total	Device	Total %	PCLK	PCLK_M	LCLK
Fusion/SmartFusion	170	482	652	AFS600	4.7	>100	>100	83
IGLOO/e	170	482	652	AGLE600V2	4.7	>100	51	33
ProASIC3/E	170	482	652	M1A3P250	10.6	>100	>100	76
ProASIC^{PLUS}	171	546	717	APA075	23.3	>100	55	53
Axcelerator	276	180	456	AX250	10.8	>100	>100	>100
RTAX-S	276	180	456	RTAX250S	10.8	>100	95	94

Note: Data in this table was achieved using typical synthesis and layout settings. Top-level parameters/generics were changed from their default value as follows: SERIRQ_EN = 1, SER_KIRQ_EN = 1, SER_INT_MIRQ_EN =1, INT_M_NUM = 2, SER_INT_M0_IRQ_SEL = 1, SER_INT_M1_IRQ_SEL = 15, APB_MASTER_PORT_EN = 1, APB_MASTER_SLOT_NUM = 2, APB_MASTER_SLOT1_BASE = 16, APB_MASTER_SLOT1_RANGE = 256, APB_MASTER_SLOT2_BASE = 1024, APB_MASTER_SLOT2_RANGE = 512.

Design Description

Verilog/VHDL Parameters

CoreLPC has parameters (Verilog) or generics (VHDL) for configuring the RTL code (Table 4). All parameters and generics are integer types.

Table 4 CoreLPC Parameters/Generics Descriptions

Parameter Name	Valid Range	Default	Description
SERIRQ_EN	0, 1	0	0: Do not include SERIRQ interface logic. 1: Include SERIRQ interface logic.
SER_KIRQ_EN	0,1	0	0: Do not include KCS SERIRQ logic. 1: Include KCS SERIRQ logic.
SER_KIRQ_SEL	0 to 15	0	Integer SERIRQ slot select for KCS interrupt.
SER_INT_MIRQ_EN	0,1	0	0: Do not include master port INT_M IRQ logic. 1: Include master port INT_M IRQ logic.
INT_M_NUM	1 to 16	1	Integer number of master port INT_M interrupts.
SER_INT_M0_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M0 interrupt.
SER_INT_M1_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M1 interrupt.
SER_INT_M2_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M2 interrupt.
SER_INT_M3_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M3 interrupt.
SER_INT_M4_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M4 interrupt.
SER_INT_M5_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M5 interrupt.
SER_INT_M6_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M6 interrupt.
SER_INT_M7_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M7 interrupt.
SER_INT_M8_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M8 interrupt.
SER_INT_M9_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M9 interrupt.

Parameter Name	Valid Range	Default	Description
SER_INT_M10_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M10 interrupt.
SER_INT_M11_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M11 interrupt.
SER_INT_M12_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M12 interrupt.
SER_INT_M13_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M13 interrupt.
SER_INT_M14_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M14 interrupt.
SER_INT_M15_IRQ_SEL	0 to 15	0	Integer SERIRQ slot select for INT_M15 interrupt.
APB_MASTER_PORT_EN	0,1	0	0: Do not include APB master port 1: Include APB master port
SYNC	0,1	0	0: Use LPC short wait SYNC value of 0b0101 during master port transactions 1: Use LPC long wait SYNC value of 0b0110 during master port transactions
APB_MASTER_SLOT_NUM	1 to 16	1	Integer number of PSEL decode slots on APB master port.
APB_MASTER_SLOT1_BASE	0 to 65535	0	Slot1 base address.
APB_MASTER_SLOT1_RANGE	0 to 65535	0	Slot1 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.
APB_MASTER_SLOT2_BASE	0 to 65535	0	Slot2 base address.
APB_MASTER_SLOT2_RANGE	0 to 65535	0	Slot2 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.
APB_MASTER_SLOT3_BASE	0 to 65535	0	Slot3 base address.
APB_MASTER_SLOT3_RANGE	0 to 65535	0	Slot3 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.
APB_MASTER_SLOT4_BASE	0 to 65535	0	Slot4 base address.
APB_MASTER_SLOT4_RANGE	0 to 65535	0	Slot4 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.

Parameter Name	Valid Range	Default	Description
APB_MASTER_SLOT5_BASE	0 to 65535	0	Slot5 base address.
APB_MASTER_SLOT5_RANGE	0 to 65535	0	Slot5 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.
APB_MASTER_SLOT6_BASE	0 to 65535	0	Slot6 base address.
APB_MASTER_SLOT6_RANGE	0 to 65535	0	Slot6 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.
APB_MASTER_SLOT7_BASE	0 to 65535	0	Slot7 base address.
APB_MASTER_SLOT7_RANGE	0 to 65535	0	Slot7 maximum address range. A max address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.
APB_MASTER_SLOT8_BASE	0 to 65535	0	Slot8 base address.
APB_MASTER_SLOT8_RANGE	0 to 65535	0	Slot8 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.
APB_MASTER_SLOT9_BASE	0 to 65535	0	Slot9 base address.
APB_MASTER_SLOT9_RANGE	0 to 65535	0	Slot9 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.
APB_MASTER_SLOT10_BASE	0 to 65535	0	Slot10 base address.
APB_MASTER_SLOT10_RANGE	0 to 65535	0	Slot10 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.
APB_MASTER_SLOT11_BASE	0 to 65535	0	Slot11 base address.
APB_MASTER_SLOT11_RANGE	0 to 65535	0	Slot11 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.
APB_MASTER_SLOT12_BASE	0 to 65535	0	Slot12 base address.
APB_MASTER_SLOT12_RANGE	0 to 65535	0	Slot12 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.

Parameter Name	Valid Range	Default	Description
APB_MASTER_SLOT13_BASE	0 to 65535	0	Slot13 base address.
APB_MASTER_SLOT13_RANGE	0 to 65535	0	Slot13 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.
APB_MASTER_SLOT14_BASE	0 to 65535	0	Slot14 base address.
APB_MASTER_SLOT14_RANGE	0 to 65535	0	Slot14 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.
APB_MASTER_SLOT15_BASE	0 to 65535	0	Slot15 base address.
APB_MASTER_SLOT15_RANGE	0 to 65535	0	Slot15 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.
APB_MASTER_SLOT16_BASE	0 to 65535	0	Slot16 base address.
APB_MASTER_SLOT16_RANGE	0 to 65535	0	Slot16 maximum address range. A maximum address range value of 0x0000 implies a single memory map location equal to the base address + 0x0000.

I/O Signals

The port signals for the CoreLPC macro are illustrated in Figure 1 and defined in Table 5.

Table 5 CoreLPC I/O Signal Descriptions

Port Name	Type	Description
APB Slave Interface		
PCLK	In	APB system clock; reference clock for all internal logic.
PRESETN	In	APB Active Low asynchronous reset.
PADDR[6:0]	In	APB address bus; address internal registers.
PSEL	In	APB slave select; select signal for register reads or writes.
PENABLE	In	APB strobe. This signal indicates the second cycle of an APB transfer.
PWRITE	In	APB write/read. If High, a write occurs when an APB transfer takes place. If Low, a read takes place.
PWDATA[7:0]	In	APB write data.
PRDATA[7:0]	Out	APB read data.

Port Name	Type	Description
PREADY	Out	APB ready. Used to insert wait states. Not used in CoreLPC, but part of APB3 Interface. Tied High (always ready).
PSLVERR	Out	APB error. Not used in CoreLPC, but part of APB3 Interface. Tied Low.
APB Master Interface		
PCLK_M	In	Master I/F APB system clock; reference clock for all internal logic.
PRESETN_M	In	Master I/F APB Active Low asynchronous reset.
PADDR_M[15:0]	Out	Master I/F APB address bus output.
PSEL_M[APB_MASTER_SLOT_NUM-1:0]	Out	Master I/F APB slave select output. Number of PSEL bits based on APB_MASTER_SLOT_NUM parameter. Maximum of 16 PSEL slots for 16 peripherals.
PENABLE_M	Out	Master I/F APB strobe output. This signal indicates the second cycle of an APB transfer.
PWRITE_M	Out	Master I/F APB write/read output. If High, a write occurs when an APB transfer takes place. If Low, a read takes place.
PWDATA_M[7:0]	Out	Master I/F APB write data output.
PRDATA_M[7:0]	In	Master I/F APB read data input.
PREADY_M	In	Master I/F APB ready input.
PSLVERR_M	In	Master I/F APB error input.
Interrupts		
INTR	Out	APB slave KCS interrupt output. This Active High output is the KCS Interface's interrupt output signal from CoreLPC.
INT_M[INT_M_NUM-1:0]	In	APB master port's interrupt input array. These Active High inputs are the APB master port interrupts to CoreLPC. The array bits can be programmed to go into a SERIRQ slot, which are then forwarded to the LPC host device.
Low Pin Count (LPC) Interface		
LAD_IN[3:0]	In	LPC address/data out: multiplexed command, address, and data input.
LAD_OUT[3:0]	Out	LPC address/data out: multiplexed command, address, and data output.

Port Name	Type	Description
LFRAMEN	In	LPC frame: Indicates start of a new cycle, termination of broken cycle. Active Low.
LAD_OEN	Out	Output enable signal used in push/pull LAD buffer configurations. Active Low.
LRESETN	In	LPC reset: Same as PCI reset on the host. Active Low.
LCLK	In	LPC clock: Same 33 MHz clock as PCI clock on the LPC host. Same clock phase with typical PCI skew.
SerIRQ Interface		
SERIRQ_OUT	Out	Serialized IRQ out.
SERIRQ_IN	In	Serialized IRQ in.
SERIRQ_OEN	Out	Output enable signal used in push/pull SERIRQ buffer configurations. Active Low.

Note: All signals are Active High (logic 1) unless otherwise noted.

Register Map and Descriptions

Register Summary

Values shown in the below tables are in hexadecimal format; type designations: R = read only; W = write only; R/W = read/write.

Table 6 CoreLPC Internal Register Address Map

Address	Register Name	Type	Width	Reset Value	Description
0x00	GCFG	R/W	8	0x40	General core configuration register.
0x04	STS	R/W	8	0x00	Status register. Bits 0-3 and 6-7 designed for KCS use, but can be used for any LPC-to-APB application.
0x08	KIRQ	R/W	8	0x00	KCS IRQ configuration register. Used to configure the SERIRQ port for KCS use.
0x10	KOBR	R/W	8	0x00	KCS output buffer register.
0x14	KIBR	R	8	0x00	KCS input buffer register; read only.
0x18	KADRL	R/W	8	0x00	KCS base address low register.
0x1C	KADRH	R/W	8	0x00	KCS base address High register.
0x34	MIRQ	R/W	8	0x00	APB master port IRQ configuration register. Used to enable the SERIRQ port for each interrupt coming from the APB master port.

General Configuration Register

Table 7 General Configuration Register

PADDR[6:0]	Register Name	Type	Width	Reset Value	Description
0x00	GCFG	R/W	8	0x40	General core configuration register.

Table 8 General Configuration Register Bit Definitions

Bits	Name	Type	Description
7	–	–	Reserved
6	IRQ_MDE	R	0: Quiet IRQ mode. Any device can initiate a SERIRQ transaction. 1: Continuous mode. Only the host initiates SERIRQ transactions (RESET VALUE). The IRQ_MDE value is decoded from the STOP length of each SERIRQ frame. The STOP length is 2 for Quiet mode, 3 for Continuous mode.
5	IRQ_EN	R/W	0: Disable SERIRQ port. 1: Enable SERIRQ port.
4:2	–	–	Reserved
1	EINTR	R/W	0: Disable interrupt, INTR. 1: Enable IBF as interrupt, INTR.
0	ELPC	R/W	0: Disable LPC port. 1: Enable LPC port.

Status Register

Table 9 describes the status register.

Table 9 Status Register

PADDR[6:0]	Register Name	Type	Width	Reset Value	Brief Description
0x04	STS	R/W	8	0x00	Status register. Bits 0-3 and 6-7 designed for KCS use, but can be used for any LPC-to-APB application.

Table 10 Status Register Bit Definitions

Bits	Name	Type	Description
7	S1	R/W	State bit 1. Bits 7 and 6 can be used to indicate the current state of the APB-side software driver. These bits are written by the driver. System software on the LPC-side could examine these bits to verify synchronization with the APB-side driver. See the description for bit 6.
6	S0	R/W	State bit 0. See bit 7 and the state table below. S1 S0 State 0 0 IDLE_STATE. Interface is idle. 0 1 READ_STATE. The APB-side driver is transferring a packet to LPC-side system software. LPC-idle system software should be in the “Read Message” state. 1 0 WRITE_STATE. The APB-side driver is receiving a packet from LPC-side system software. The LPC-side system software should be writing a command to CoreLPC. 1 1 ERROR_STATE. The APB-side driver has detected a protocol violation at the interface level, or the transfer has been aborted. LPC-side system software can either use the Get_Status control code to request the nature of the error, or retry the command.
5	OEM2	R/W	OEM2 read/write bit – reserved for CoreLPC implementer / system integrator definition.
4	OEM1	R/W	OEM1 read/write bit – reserved for CoreLPC implementer / system integrator definition.

Bits	Name	Type	Description
3	C_DN	R	Specifies whether the last write was to the command cegister or the Data_In register (1 = command, 0 = data). The default base address of an I/O mapped KCS-SMS interface is 0xCA2. According to the IPMI specification for KCS, the command register is located at the base address + 1. As such, bit 0 of the incoming KCS I/O address is written into this bit, as it signifies a command write to the IBR. Otherwise it is a data write to the IBR.
2	SMS_ATN	R/W	Set to 1 when the APB master has one or more messages in the receive message queue, or when a watchdog timer pre-timeout or event message buffer full condition exists. Refer to the IPMI specification for further information on the use and requirements for the SMS_ATN bit.
1	KIBF	R	KCS input buffer register flag. Automatically set to 1 when either the associated command or Data_In byte has been written by the LPC-side system software to the IBR register. Cleared when the IBR has been read by the APB master.
0	KOBF	R	KCS output buffer register flag. Set to 1 when the associated Data_Out register (OBR) has been written by the APB master. Cleared when the OBR has been read by the LPC-side system software.

KCS IRQ Configuration Register

Table 11 KCS IRQ Configuration Register

PADDR[6:0]	Register Name	Type	Width	Reset Value	Brief Description
0x08	KIRQ	R/W	8	0x00	KCS IRQ configuration register. Used to configure the SERIRQ port for KCS use.

Table 12 KCS IRQ Configuration Register Bit Definitions

Bits	Name	Type	Description
7:1	–	–	Reserved
0	KIRQ_EN	R/W	0: Disable parameter-configured KIRQ slot of SERIRQ port. 1: Enable parameter-configured KIRQ slot of SERIRQ port.

KCS Output Buffer Register

Table 13 KCS Output Buffer Register

PADDR[6:0]	Register Name	Type	Width	Reset Value	Brief Description
0x10	KOBR	R/W	8	0x00	KCS output buffer register.

KCS Input Buffer Register

Table 14 KCS Input Buffer Register

PADDR[6:0]	Register Name	Type	Width	Reset Value	Brief Description
0x14	KIBR	R	8	0x00	KCS input buffer register; read only.

KCS Base Address Low Register

Table 15 KCS Base Address Low Register

PADDR[6:0]	Register Name	Type	Width	Reset Value	Brief Description
0x18	KADRL	R/W	8	0x00	KCS base address low register.

Table 16 KCS Base Address Low Register Bit Definitions

Bits	Name	Type	Description
7:1	KADRL	R/W	KCS base address low register bits Contains the LSB of the 16-bit base address. For an I/O mapped KCS SMS interface base address of 0x0CA2, LADRL must be set to 0xA2.
0	-	-	Reserved. Not used. Bit 0 is not used as address; it is an LPC-side system software control bit that gets mapped to the C_DN bit in the status register during LPC-side writes. During LPC reads, the incoming bit 0 value determines if the read request is for status or data

KCS Base Address High Register

Table 17 KCS Base Address High Register

PADDR[6:0]	Register Name	Type	Width	Reset Value	Brief Description
0x1C	KADRH	R/W	8	0x00	KCS base address High register.

Table 18 KCS Base Address High Register Bit Definitions

Bits	Name	Type	Description
7:0	LADRH	R/W	KCS base address High register bits. Contains the MSB of the 16-bit base address. For an I/O mapped KCS SMS interface base address of 0x0CA2, LADRH must be set to 0x0C.

APB Master Port IRQ Configuration Register

Table 19 APB Master Port IRQ Configuration Register

PADDR[6:0]	Register Name	Type	Width	Reset Value	Brief Description
0x34	MIRQ	R/W	8	0x00	APB master port IRQ configuration register. Used to enable the SERIRQ port for each interrupt coming from the APB master port.

Table 20 APB Master Port IRQ Config1 Register Bit Definitions

Bits	Name	Type	Description
7:4	INT_M_IRQ_SEL	R/W	APB master port interrupt number index to associate with its parameter configured SERIRQ slot enable, INT_M_IRQ_SEL_EN. 16 interrupts can be brought in from the APB master port if the KCS is not used; otherwise only 15 interrupts can be brought in from the APB master port , in addition to the one KCS interrupt.
0	INT_M_IRQ_SEL_EN	R/W	0: Disable parameter-configured MIRQ slot of SERIRQ port. 1: Enable parameter-configured MIRQ slot of SERIRQ port.

Design Details

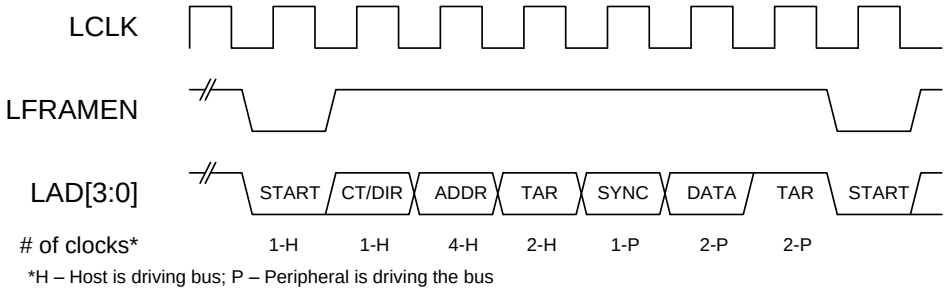
LPC Supported Cycle Types

CoreLPC supports I/O read/write cycle types.

I/O Read/Write Cycle Types

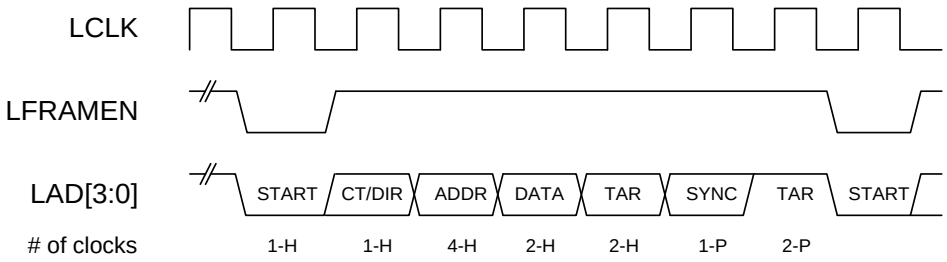
A typical read transaction is shown in Figure 3 and a write transaction is shown in Figure 4. The first clock is the start field followed by the cycle type and direction field, CT/DIR. The ADDR field is 4 clocks wide for I/O cycle writes/reads and includes the 16-bit base address for the incoming or outgoing data. If the transaction is a read, CoreLPC supplies the DATA field. If the transaction is a write, the host supplies the DATA to CoreLPC.

Refer to the LPC specification for further cycle definition details.



*H – Host is driving bus; P – Peripheral is driving the bus

Figure 3 LPC I/O Read Example Transaction



*H – Host is driving bus; P – Peripheral is driving the bus

Figure 4 LPC I/O Write Example Transaction

LPC FSM

I/O Read/Write FSM

For I/O reads and writes the FSM works by collecting the transaction type initially and proceeding accordingly as shown in Figure 5.

In KCS Mode:

The KADRL and KADRH registers are written only by the APB side and map to a specific ADDR base address from the system-side. When an incoming ADDR value matches the KADRL[7:1] and KADRH registers, then CoreLPC “addresses” and proceeds with a transaction based on the cycle type and direction. The APB master reacts to these LPC-side system KCS read/write commands. For example, if a READ command arrives from the LPC-side, the APB-based driver gets an IBF interrupt, read the IBR register’s READ command, and proceed with fetching read data and placing it in the OBR register, which generates the OBF flag. If using SERIRQ, the OBF flag propagates through the SERIRQ line, alerting the LPC-side system software that the OBR register is ready. As an alternative to the SERIRQ channel, the LPC-side system software could poll the status register for the OBF bit.

In APB Master Port Mode:

The PSLVERR and PREADY signals of the APB3 master port are translated to the LPC interface in the SYNC field. If PSLVERR is active for a given addressed peripheral, the SYNC field is assigned the error condition value of 0b1010 and has priority over other SYNC field values. If PREADY is active for a given addressed peripheral, the SYNC field is assigned either the short wait value of 0b0101, or the long wait value of 0b0110 based on the parameter SYNC.

Once PREADY has reasserted (or was never deasserted during a transaction), the SYNC field is assigned the ready value of 0b0000.

Note: When the short wait SYNC value is used, peripheral wait times must be equal to or less than the LPC host’s short wait timeout abort mechanism. If the APB master port clock rate is equal or close to the LPC clock rate, the short wait time of a standard peripheral will be within the default value of 8 LPC clock cycles, according to the LPC specification. However, if the master port clock rate is much slower than the LPC clock rate or a peripheral has long wait times, then the LPC host’s timeout abort mechanism must be duly compensated or the long wait SYNC value must be used. If the long wait value is used, the LPC host will not timeout the transactions and thus an external timer must be used to reset the master port via PRESET_M in order to time-out hung up peripherals.

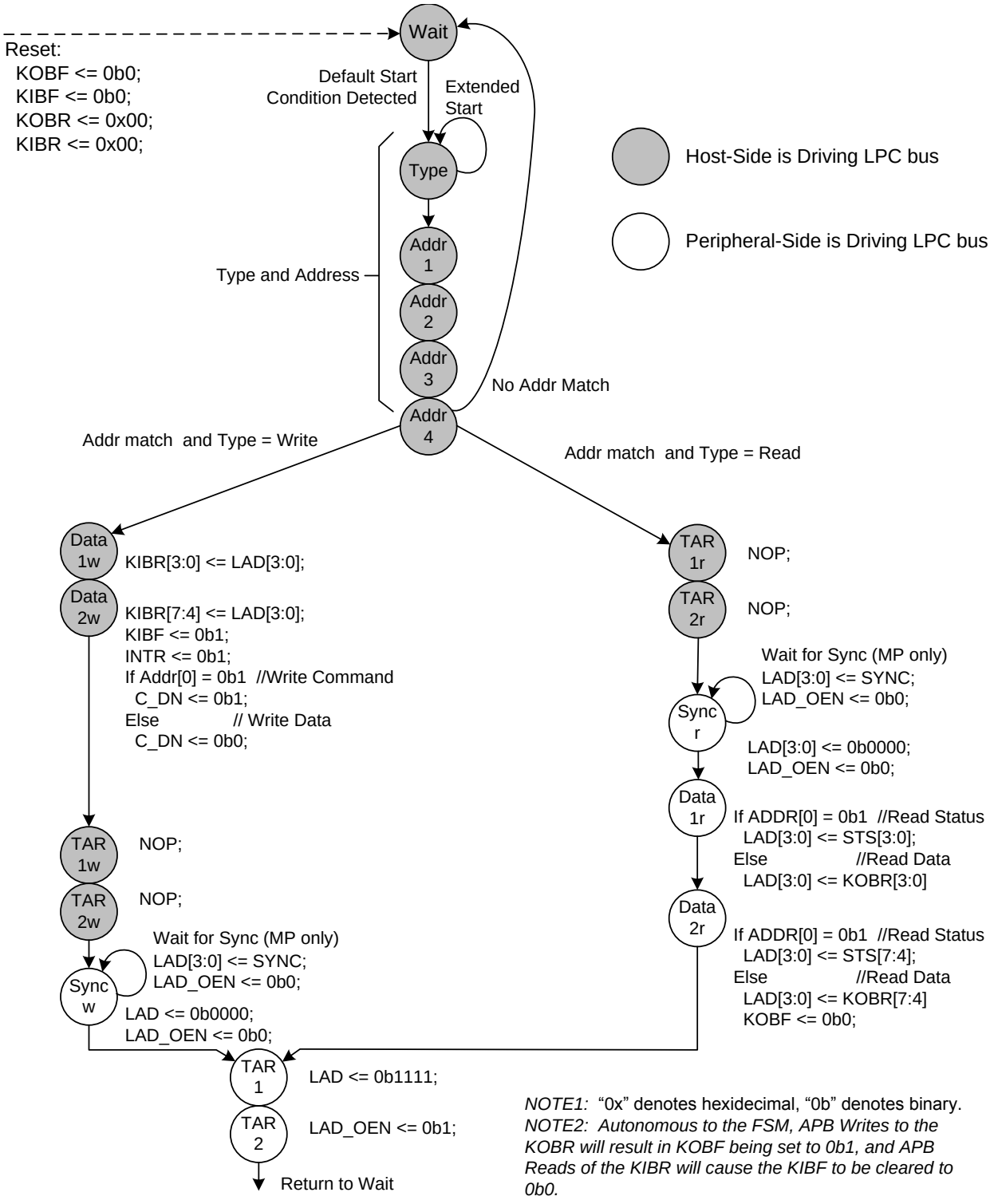


Figure 5 FSM for LPC-Side I/O Writes and Reads (KCS protocol shown, APB master port writes/reads go directly to master port peripherals, with APB PREADY_M and PSLVERR_M status relayed during the SYNC states)

APB Slave Port Support via KCS Protocol

The KCS interface definition and protocol follows the LPC I/O cycle specification, adding register definitions and flag conditions to avoid register access contention between the APB slave port and the external LPC-side system software (refer to Figure 4 and Table 10). Additionally, refer to the KCS protocol section of the IPMI Specification for further details.

APB Master Port Support

CoreLPC provides an APB master port, directly accessible and driven by the LPC host. Each master port peripheral's APB PSEL line is decoded based on the configurable base address and range parameters.

Refer to the I/O Read/Write FSM section for further details on LPC-APB master port transactions.

Serial Interrupt Request (SERIRQ) FSM

CoreLPC allows for interrupts to be handled through the SERIRQ interface. The SERIRQ interface is a serial line interface, which uses time slots to send multiple interrupts across a line.

The following outgoing interrupts may be channeled through SERIRQ:

- CoreLPC's KCS OBF interrupt
- Up to 16 APB master port peripherals

All slot locations are parameter-based and must be known before programming the FPGA. Slot locations are not soft-programmable. The SERIRQ FSM, shown in Figure 6, asserts (Quiet mode) or detects (Continuous mode) a start condition and begins a counter which generates interrupts at the programmed IRQx time slots (refer to the three separate IRQ configuration registers for more information). Note that in Quiet mode, the start condition (SERIRQ Low) is asserted by CoreLPC for one clock cycle when an outgoing and configured-for-SERIRQ interrupt is asserted; the host completes the start condition by continuing with 3 to 7 more clock cycles of SERIRQ Low. If the SERIRQ is not idle when an outgoing interrupt is asserted, the SERIRQ logic waits until idle before sending off its SERIRQ start condition.

Figure 6, Figure 7, and Figure 8 show the internal CoreLPC SERIRQ FSM and the start, IRQ, and stop timing of the SERIRQ line. Refer to the Serialized IRQ Support for PCI Systems, Version 6.0 Specification, for further information on the SERIRQ protocol.

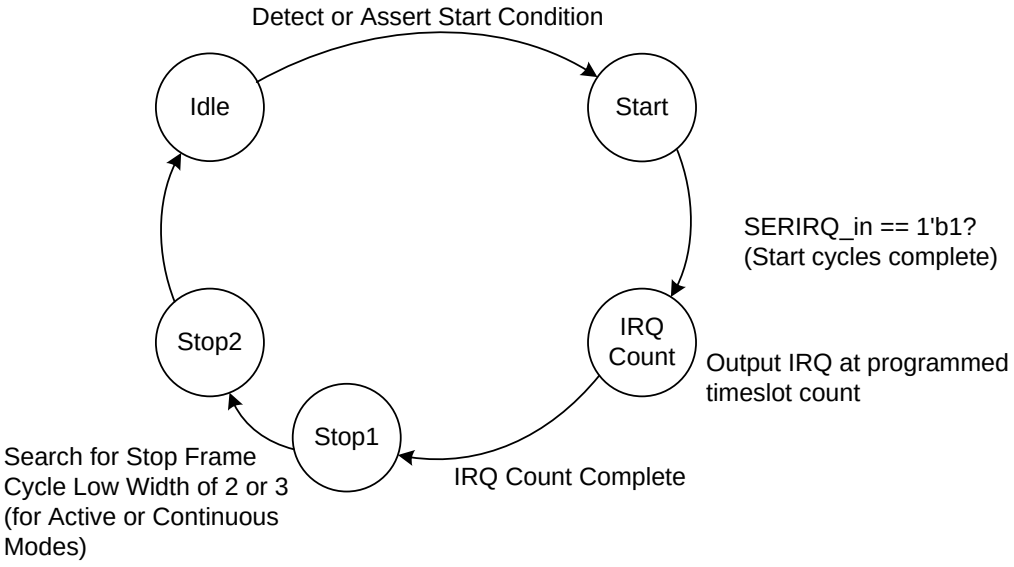
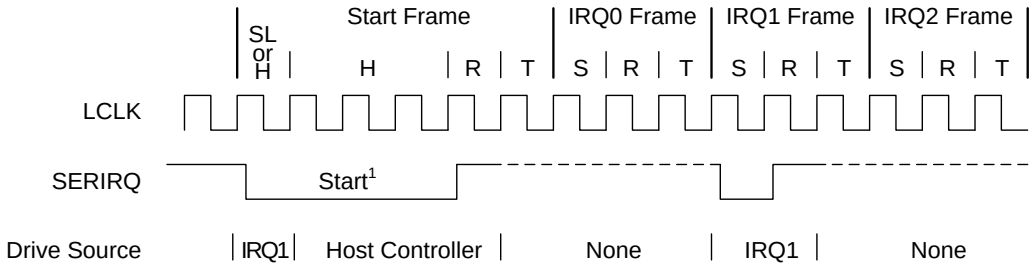


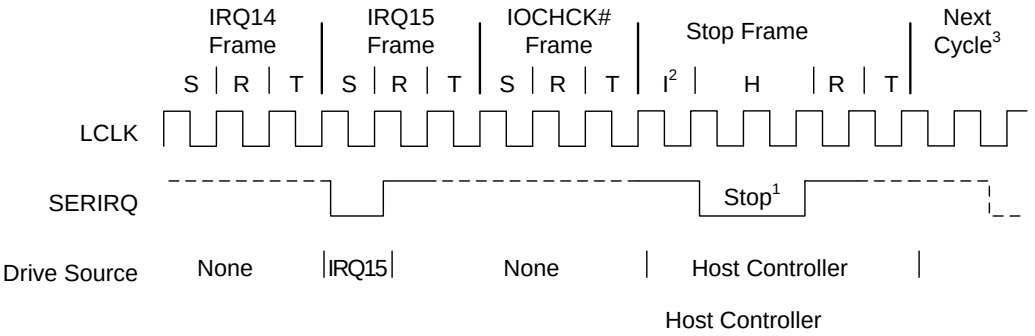
Figure 6 SERIRQ FSM



H = Host Control, SL = Slave Control, S = Sample, R = Recovery, T = Turn-around

1. Start Frame pulse can be 4-8 clocks wide.

Figure 7 SERIRQ Start Frame with IRQ1 Assertion Timing



H = Host Control, S = Sample, R = Recovery, T = Turn-around, I = Idle

1. Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
2. There may be none, one or more Idle states during the Stop Frame.
3. The next SERIRQ cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

Figure 8 SERIRQ Start Frame with IRQ15 Assertion and Stop Frame Timing

APB Interface

Both slave and master port APB interfaces adhere to the AMBA peripheral bus, version 3 specification. Typical timing waveforms are shown below. Refer to the AMBA specification for further timing/waveform information.

APB Interface Timing

Figure 9 and Figure 10 show typical write cycle and read cycle timing relationships relative to the system clock, PCLK.

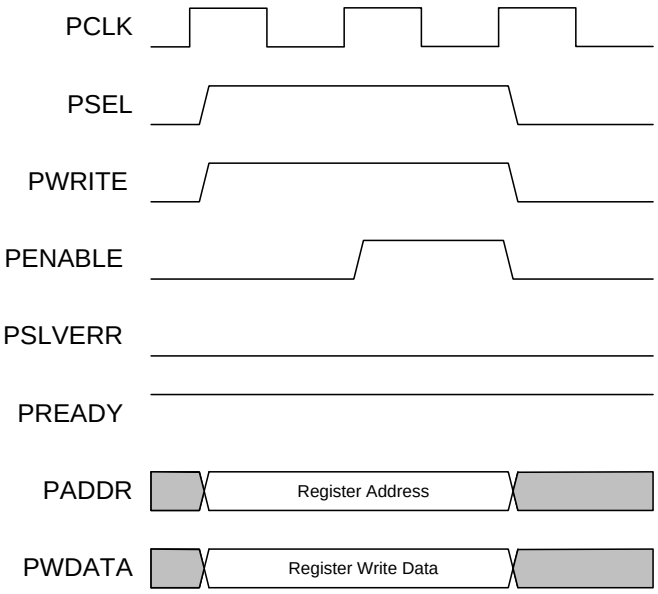


Figure 9 APB Data Write Cycle

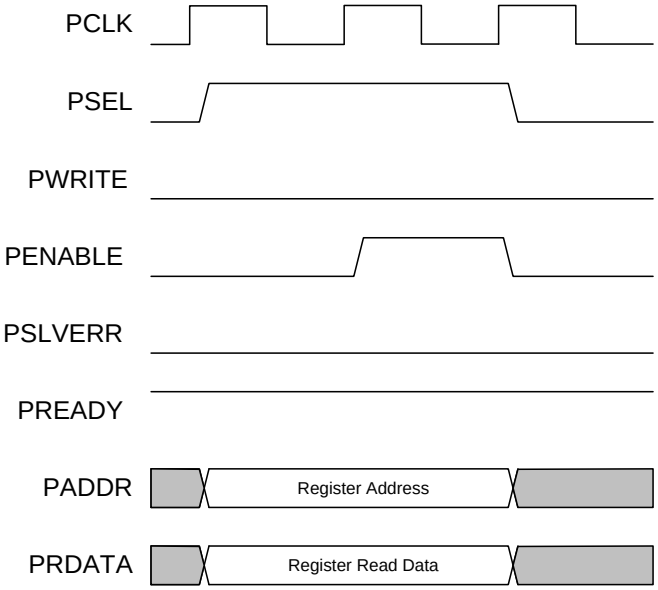


Figure 10 APB Data Read Cycle

Clock Domains

As shown in Figure 11, CoreLPC consists of three clock domains: PCLK for the APB slave I/F, PCLK_M for the APB master I/F and LCLK for all other logic.

The PRESETN resets the APB slave I/F block, PRESETN_M resets the APB master I/F block and LRESETN resets the LPC I/F and the SerIRQ I/F blocks.

Note the following clock and reset implications based on application specific design requirements:

- You can connect PCLK_M to the LCLK input pin and PRESET_M to the LRESETN input pin. For this scenario, the APB peripherals connected to the CoreLPC APB master I/F would be clocked by LCLK (33 MHz) and reset by LRESETN. However, in some systems the host cannot continuously drive LCLK. Confirm the host operation during idle states before relying on LCLK as a continuous clock source.
- You can also connect PRESETN_M to the LRESETN signal, if LRESETN is synchronized to PCLK_M prior to using the PRESETN_M I/F signal of the CoreLPC APB master. This allows the host to reset the APB peripherals while the master APB operates from a clock independent of LCLK.

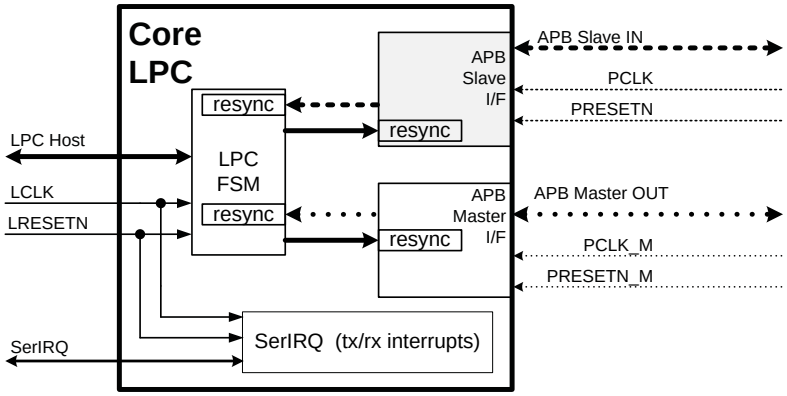


Figure 11 LPC and APB Slave In Clock Domains

Tool Flows

Licensing

CoreLPC is licensed in two ways. Depending on your license tool flow, functionality may be limited.

Obfuscated

Complete RTL code is provided for the core, allowing the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed within Libero® Integrated Design Environment (IDE). The RTL code for the core is obfuscated[1] and some of the testbench source files are not provided; they are precompiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

SmartDesign

CoreLPC is preinstalled in the SmartDesign IP deployment design environment. Figure 12 shows an example of the instantiated view. The core can be configured using the configuration GUI within SmartDesign, as shown in Figure 13.

For more information on using SmartDesign to instantiate and generate cores, refer to the Using DirectCore in Libero® IDE User's Guide.

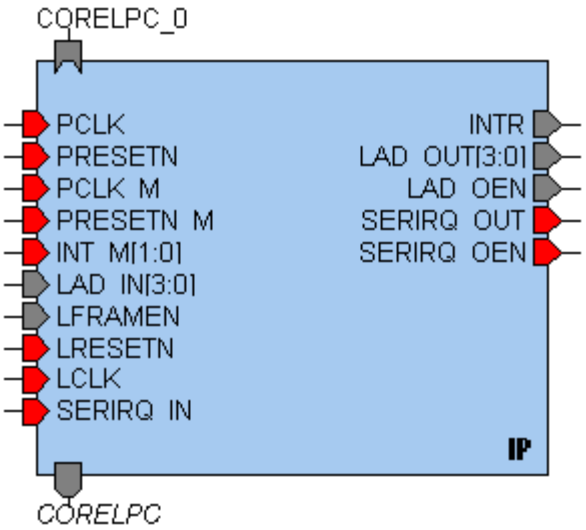


Figure 12 CoreLPC Full I/O View[1]

[1] *Obfuscated means the RTL source files have had formatting and comments removed, and all instance and net names have been replaced with random character sequences.*

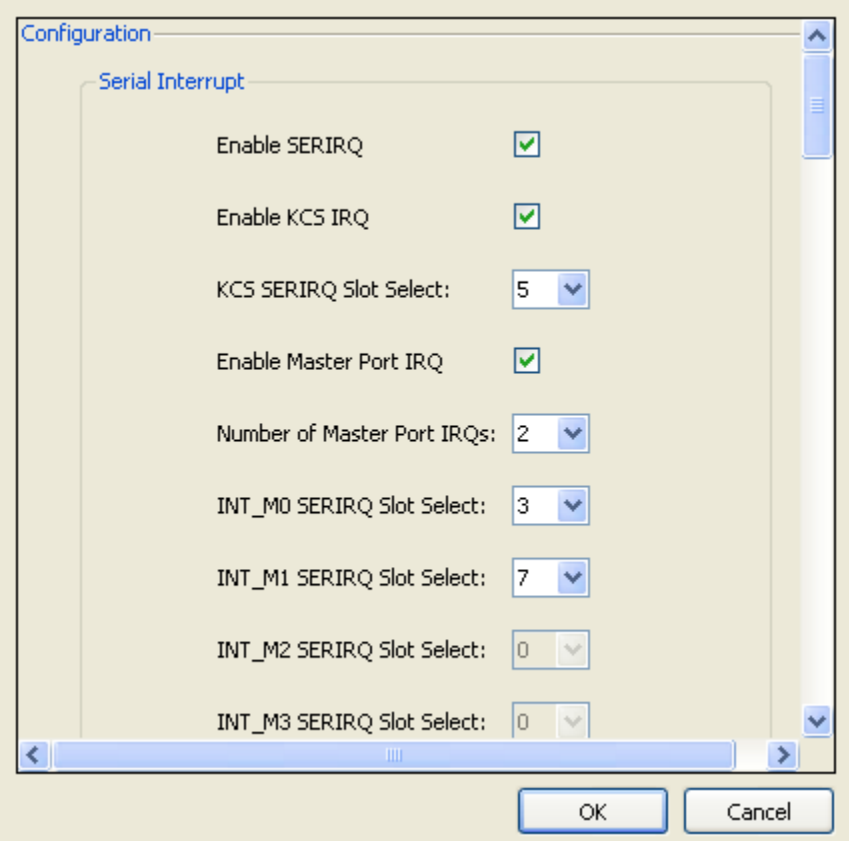


Figure 13 CoreLPC Parameter Configuration

Simulation Flows

The user testbench for CoreLPC is included in all releases.

To run simulations, select the user testbench flow within SmartDesign and click **Save & Generate** on the **Generate** pane. The user testbench is selected through the Core Testbench Configuration GUI.

When SmartDesign generates the Libero IDE project, it will install the user testbench files.

To run the user testbench, set the design root to the CoreLPC instantiation in the Libero IDE Design Hierarchy pane and click the **Simulation** icon in the Libero IDE Design Flow window. This will invoke ModelSim® and automatically run the simulation.

User Testbench

The simulation testbench shown in Figure 14 includes: an instantiation of the CoreLPC macro, APB and LPC function calls, a SERIRQ checker, and an APB peripheral model. The top-level testbench (tb_user_corelpc) includes the necessary open drain connections. The testbench utilizes simple APB read/write function calls to initialize each module and sends example LPC host-side I/O write and read transactions to the KCS interface or to an APB peripheral on the APB master port interface. Checks are performed at all interfaces.

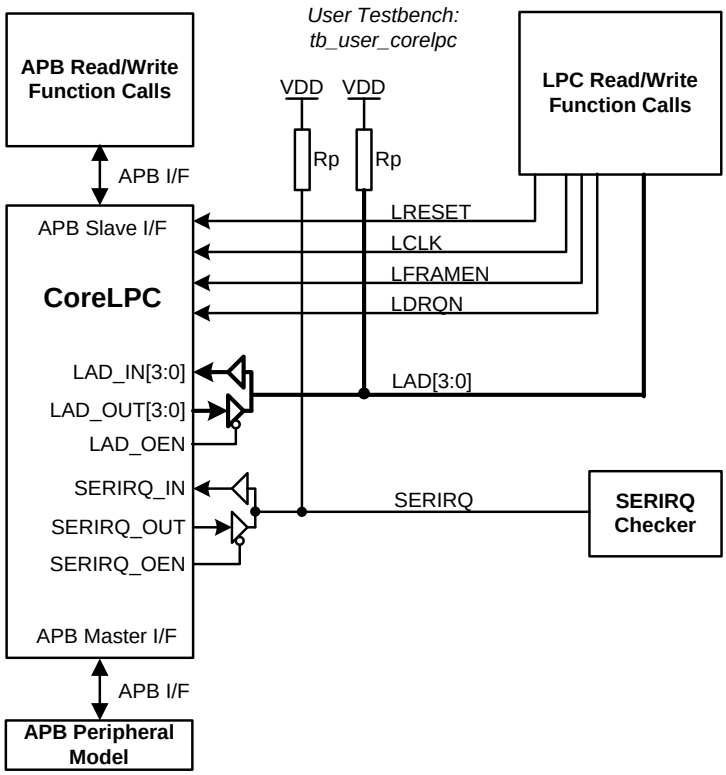


Figure 14 CoreLPC User Testbench

Synthesis in Libero IDE

Click the **Synthesis** icon in Libero IDE. The Synthesis window appears, displaying the Synplicity® project. Set Synplicity to use the Verilog 2001 standard if Verilog is being used. To run Synthesis, click the **Run** icon.

Note: Implementing CoreLPC in a design may require Synthesis constraints for design optimization. Refer to the Application Hints section for more details.

Place-and-Route in Libero IDE

Click the Layout icon in Libero IDE to invoke Designer.

Note: Implementing CoreLPC in a design may require Place and Route constraints for design optimization. Refer to the Application Hints section for more details

Application Hints

This chapter provides various hints to ease the process of implementation and integration of CoreLPC into your design.

Connecting the Master Port in SmartDesign

Figure 15 shows an example system design using CoreLPC's master APB port. Because CoreLPC controls the PSEL of each peripheral, CoreAPB is used to connect the peripherals to CoreLPC as it passes all PSEL signals generated by CoreLPC through to each peripheral. Using CoreAPB will tie PREADY and PSLVERR signals to their inactive states. A future version of CoreAPB3 will likely support PREADY and PSLVERR functionality for applications like CoreLPC, where PSEL decode control is required by the master.

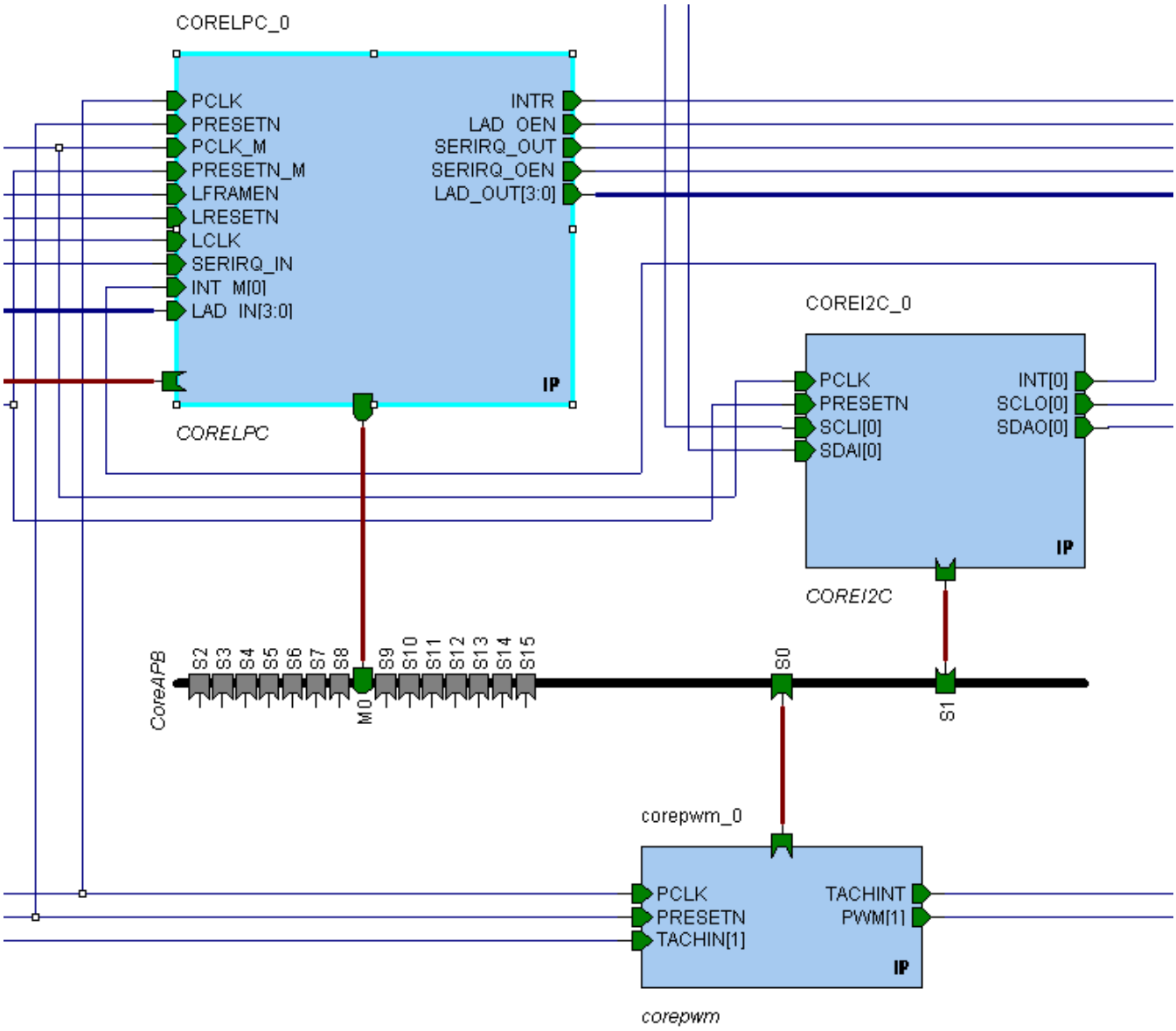


Figure 15 CoreLPC System Example using CoreAPB

Setting Synthesis and Place-and-Route Constraints

The Synplicity FPGA Implementation tools can read native Synopsys Design Compiler (SDC) constraint files for a supported set of clock definition, I/O delay, and timing exception constraints.

For CoreLPC in a typical design, the following top-level example constraints may be referenced for internal false paths and LPC-side I/Os.

Clock Domain Crossing False Path Constraints:

False path constraints require clock definitions; the example below defines the LPC clock at 33 MHz, PCLK at 100 MHz, and PCLK_M at 50 MHz.

Create Clock

```
create_clock -name { Clock_LPC }  -period 30.000 -waveform {0.000 15.000} { LCLK  }
create_clock -name { Clock_PCLK }  -period 10.000 -waveform {0.000  5.000} { PCLK  }
create_clock -name { Clock_PCLK_M } -period 20.000 -waveform {0.000  1.000} { PCLK_M }
```

False Path Constraints between clock domains

```
set_false_path -from [all_registers -clock_pins -clock { Clock_PCLK }]  -to [all_registers -data_pins -clock { Clock_LPC }]
set_false_path -from [all_registers -clock_pins -clock { Clock_LPC }]  -to [all_registers -data_pins -clock { Clock_PCLK }]
set_false_path -from [all_registers -clock_pins -clock { Clock_PCLK_M }] -to [all_registers -data_pins -clock { Clock_LPC }]
set_false_path -from [all_registers -clock_pins -clock { Clock_LPC }]  -to [all_registers -data_pins -clock { Clock_PCLK_M }]
```

LPC and SerIRQ Top-Level I/O Constraints:

LPC-side I/O requirements are based on Version 2.3 of the PCI Specification.

Note: The top-level signal names listed below could be different per design.

Input Delay Constraints FOR TOP LEVEL LPC and SERIRQ signal

```
set_input_delay -max 22.500 -clock { Clock_LPC } [get_ports { LAD3 LAD2 LAD1 LAD0 LFRAMEN SERIRQ }]
set_input_delay -min 0.000 -clock { Clock_LPC } [get_ports { LAD3 LAD2 LAD1 LAD0 LFRAMEN SERIRQ }]
```

Output Delay Constraints FOR TOP LEVEL LPC and SERIRQ signals

```
set_output_delay -max 10.500 -clock { Clock_LPC } [get_ports { LAD3 LAD2 LAD1 LAD0 SERIRQ }]
set_output_delay -min -2.000 -clock { Clock_LPC } [get_ports { LAD3 LAD2 LAD1 LAD0 SERIRQ }]
```

Hints on Configuring Bidirectional Buffers in RTL

For an example on how to connect the bidirectional LAD and SERIRQ outputs in a design, refer to the user testbench in Figure 14, and either the verilog tb_user_CoreLPC.v and/or the VHDL tb_user_CoreLPC.vhd RTL files.

Firmware Driver Location

Drivers for CoreLPC are available via the Firmware Catalog tool provided with Libero IDE. For more information on the Firmware Catalog, refer to the Microsemi web site: http://www.microsemi.com/soc/products/software/firmwarecat/default.aspx.

List of Changes

The following table lists critical changes that were made in each revision of the document.

Date	Change	Page
March 2012	Updated the document for v3.2.	N/A
	Added the Supported Families section.	7

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Microsemi SoC Products Group Customer Support website for more information and support (http://www.microsemi.com/soc/support/search/default.aspx). Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on website.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

50200175-2/03.12