CoreHPDMACtrl v2.1 Release Notes

This document accompanies the release of CoreHPDMACtrl v2.1 IP core. This document provides details about the features and enhancements, system requirements, supported families, implementations, and known limitations and workarounds of the core.

Key Features

CoreHPDMACtrl is a highly configurable core and has the following features:

- Provides four queuing high performance direct memory access (HPDMA) descriptors.
- Starts and resets the memory descriptor.
- Provides source and destination address for each descriptor.
- Provides size and direction of transfer for each descriptor.
- DMA transfer complete and error interrupts.
- Provides advanced high-performance bus (AHB)-Lite master interface to the fabric interface controller (FIC)
- Supports word-aligned data transfers

Delivery Types

CoreHPDMACtrl is provided as register transfer level (RTL).

RTL

Complete RTL source code is provided for the core.

Supported Families

- SmartFusion®2
- IGLOO®2

Supported Tool Flows

CoreHPDMACtrl v2.1 requires Libero® System-on-Chip (SoC) software v11.2 or later.

Installation Instructions

For the RTL version of the core, no license is required to be installed before the core can be exported.

Consult the Libero SoC online help for instructions on core installation and licensing.

New Features and Devices

The HPDMA source address, destination address, transfer size, and transfer direction have been changed from static parameter configuration to ports. Hence, the dynamic configuration is now allowed.

Documentation

This release contains a copy of the *CoreHPDMACtrl Handbook*, which describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also provides implementation suggestions.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi® web site at: www.microsemi.com/soc.

Supported Test Environments

- Verilog user testbench
- VHDL user testbench

Release History

Table 1 Release History

Version	Date	Changes
2.1	April 2014	As listed inTable 2.
2.0	November 2013	Initial release

Resolved Issues in the v2.1 Release

Table 2 Resolved SARs in CoreHPDMACtrl v2.1 Release

SAR	Description
53313	Dynamic address configuration of descriptors is required.
55533	Errors in simulations while loading libraries if both CoreHPDMACtrl and CoreSysServices are used in the same design.

Discontinued Features and Devices

No features have been discontinued in the CoreHPDMACtrl v2.1 release.

Known Limitations and Workarounds

There are no known issues for CoreHPDMACtrl v2.1.

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