
CoreFIR v8.6 Release Notes

These release notes accompany the production release of CoreFIR v8.6. This document provides details about the features and enhancements, system requirements, supported families, implementations, and known issues and workarounds.

Key Features

CoreFIR supports the following filter types:

- Fully Enumerated
- Folded
- Polyphase Interpolator
- Polyphase Decimator

The key features for each type are listed in [Table 1](#).

Table 1. Key Feature Support

Feature	Fully Enumerated	Folded	Interpolator	Decimator
Number of filter coefficients	2 to 2N, where N is a number of physically available MACs	4 to 1,024	2 – 1,024	2 – 1,024
Input data bit width	2 – 18	2 – 18	2 – 18	2 – 18
Coefficient bit width	2 – 18	2 – 18	2 – 18	2 – 18
Signed and unsigned data coefficients	Yes	Yes	Yes	Yes
Full precision output	Yes	Yes	Yes	Yes
Coefficient symmetry optimization	Yes	No	No	No
Constant coefficients and constant coefficient sets	Yes	Yes	Yes	Yes
Run-time reloadable coefficients	Yes	Yes	Yes	Yes
RAM-based coefficient storage	No	Yes	Yes	Yes
RAM-based data storage	No	Yes	Yes	Yes

Supported Interfaces

No standard interface available.

Delivery Types

CoreFIR is licensed for register transfer level (RTL). Complete HDL source code is provided for the core and testbenches.

Supported Families

- RTG4™
- SmartFusion®2
- IGLOO®2

Supported Tool Flows

- CoreFIR v8.6 requires Libero® SoC software v11.4 or later
- Supports only Windows and Linux operating systems

Installation Instructions

The CoreFIR CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero SoC, or the CPZ file can be manually added using the Add Core catalog feature. Once installed in the Libero SoC Catalog, the core can be instantiated and configured.

Refer to the [Libero SoC Online Help](#) for further instructions on core installation, licensing, and general use.

Documentation

The release contains a copy of the *CoreFIR Handbook*. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, as well as implementation suggestions. For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website at www.microsemi.com.

Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

Release History

Table 2 lists the release history for this core release version.

Table 2. Release History

Version	Date	Changes
8.6	March 2015	Support for RTG4 added
8.5	January 2014	Support for Linux OS added RTAX-D support moved to a separate IP
8.4	June 2013	Support for IGLOO2 added
8.3	March 2013	Support for SmartFusion2 added
7.0	March 2011	Decimation filter option added
6.0	December 2010	Folded single-rate and Polyphase Interpolation filter option added
4.1	July 2010	Improved filter throughput. The release supports RTAX-DSP family only
4.0	August 2009	Fully enumerated MAC-based FIR filter implementation. The release supports RTAX-DSP family only
3.0	May 2006	Constant coefficient algorithm implemented
2.0	January 2005	Initial release

Resolved Issues in the v8.6 Release

Table 3 shows SARs resolved in the v8.6 release of CoreFIR.

Table 3. Resolved SARs in CoreFIR v8.6

SAR No.	Description
26897	Prevent using unsigned coefficients in anti-symmetric filter
43880	Fix "Invalid die configuration" issue for all valid die types
54996	Indicate a correct uRAM depth range on Handbook
55935	Eliminate core generation failures caused by incorrect device identification
57820	Eliminate simulation failure for 97-tap fully enumerated filter
58567	Improve compatibility for multiple core instances
61779	Eliminate potential metastability when using asynchronous reset
62325	Add RTG4 support

Resolved Issues in the v8.5 Release

Linux OS support added.

Resolved Issues in the v8.4 Release

Table 3 shows SARs resolved in the v8.4 release of CoreFIR.

Table 4. Resolved SARs in CoreFIR v8.4

SAR No.	Description
48057	Support for IGLOO2 family

Resolved Issues in the v8.3 Release

Table 4 shows SARs resolved in the v8.3 release of CoreFIR.

Table 5. Resolved SARs in CoreFIR v8.3

SAR No.	Description
33218	Support for SmartFusion2 family
39038	Add support for interpolation filter signed data
39083	Fix user testbench to provide coverage for polyphase filter corner cases
40647	Eliminate unnecessary FIFO on polyphase designs
40679	Improve interpolation filter ease of use

Resolved Issues in the v7.0 Release

Table 6. Resolved SARs in CoreFIR v7.0 Release

SAR No.	Description
30457	Decimation architecture is not supported in CoreFIR 6.0.
30300	Minimum Libero version should be 9.1, however, it is specified to be 8.6.
30458	TGI-interpolation filter should be seen as 'Multi-rate'.

Resolved Issues in the v6.0 Release

Table 7. Resolved SARs in CoreFIR v6.0 Release

SAR No.	Description
28646	Implement semi-parallel (folding) filter type.
29750	CoreFIR v4.1 does not support up-sampling/interpolation architecture.

Resolved Issues in the v4.1 Release

Table 8. Resolved SARs in CoreFIR v4.1 Release

SAR No	Description
20214	Implement RTL licensing.
20420	Correct typos on the handbook.
26463	Eliminate extended datapath delays by inserting extra pipeline registers.
26466	Double register high fanout signals to support synthesis replication feature.

Resolved Issues in the v4.0 Release

No issues resolved. This was the first release of the MAC-based FIR filter.

Resolved Issues in the v3.0 Release

No issues resolved. The Constant Coefficient architecture was added.

Discontinued Features and Devices

CoreFIR discontinued support for RTAX-D devices. The support for RTAX-D devices moved to a separate IP compatible with Libero IDE design software.

Known Limitations and Workarounds

No known issues have been found in the CoreFIR v8.6 release.



Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

© 2015 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,400 employees globally. Learn more at www.microsemi.com.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.