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CoreFIFO v2.7 Release Notes

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 8.0

Updated changes related to CoreFIFO v2.7.

1.2 Revision 7.0

Updated changes related to CoreFIFO v2.6.

1.3 Revision 6.0

Updated changes related to CoreFIFO v2.5.

1.4 Revision 5.0

Updated changes related to CoreFIFO v2.4.

1.5 Revision 4.0

Updated changes related to CoreFIFO v2.3.

1.6 Revision 3.0

Updated changes related to CoreFIFO v2.2.

1.7 Revision 2.0

Updated changes related to CoreFIFO v2.1.

1.8 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreFIFO v2.0.

Contents

3 CoreFIFO v2.7 Release Notes

3.1 Overview

These release notes accompany the production release of CoreFIFO v2.7. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

3.2 Features

- Dual and single clock operation
- Clock edge - positive/negative
- Full/empty flag generation
- Almost full and almost empty flag generation
- Empty/full stop generation
- Write and read count
- Variable aspect ratio (depth/width)
- Error status generation with overflow and underflow
- Write acknowledge and read data valid generation
- Supports large RAM and micro RAM or controller only option
- Almost full and almost empty single threshold value for assertion
- Pipelining in the memory read data paths (controller with memory option)
- Pre-fetch mode option to provide read data in the same clock cycle
- FWFT (First-Word Fall-Through)
- ECC capability for RTG4 and PolarFire device family

3.3 Delivery Types

CoreFIFO is licensed as register transfer level (RTL). Complete RTL source code is provided for the core and testbenches.

3.4 Supported Families

- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

3.5 Supported Tool Flows

CoreFIFO v2.7 requires Libero® System-on-Chip (SoC) software v11.0 or later.

3.6 Installation Instructions

The CoreFIFO CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

3.7 Documentation

This release contains a copy of the *CoreFIFO Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

3.8 Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

3.9 Resolved History

Table 1, page 6 lists the release history for CoreFIFO.

Table 1 • **Release History**

Version	Date	Changes
2.7	July 2018	As listed in Table 2, page 7
2.6	February 2017	As listed in Table 3, page 7
2.5	March 2016	As listed in Table 4, page 7
2.4	April 2015	As listed in Table 5, page 7
2.3	December 2014	As listed in Table 6, page 8
2.2	July 2014	As listed in Table 7, page 8
2.1	November 2013	As listed in Table 8, page 8
2.0	March 2013	Initial Release. As listed in Table 9, page 9

3.10 Resolved Issues in the v2.7 Release

Table 2 • **Resolved Issues in the v2.7 Release**

SAR Number	Changes
91876	CoreFIFO should double sync the reset with write and read clock.
87120	Support for async reset option for RTG4.
93202	Overflow flag not getting asserted.
95499	CoreFIFO post configuration indicates ”controller only”.
94791	EMPTY flag behavior to be documented.
93440	EMPTY flag is mentioned as synchronous in HB where as in case of FWFT, it is combinational.
87688	Remove or modify incorrect entry “run run -all” in packager attributes.
98462	glitches on EMPTY and DVLD not getting asserted with PREFETCH or FWFT with single word in FIFO.
97984	PF CoreFIFO does not enable SB_CORRECT/ DB_DETET for valid configuration.

3.11 Resolved Issues in the v2.6 Release

Table 3 • **Resolved Issues in the v2.6 Release**

SAR Number	Changes
43498	Missing Modules in Libero Design Hierarchy.
80253	RTG4 uses sync reset, but the Handbook mentions async.
80609	Support for PolarFire.
80679	MEMWD and MEMRD are bypassed for controller mode.

3.12 Resolved Issues in the v2.5 Release

Table 4 • **Resolved Issues in the v2.5 Release**

SAR Number	Changes
68070	CoreFIFO address counter issue (not getting rolled off).
68113	ECC capability missing for RTG4.

3.13 Resolved Issues in the v2.4 Release

Table 5 • **Resolved Issues in the v2.4 Release**

SAR Number	Changes
66456	RTG4 DRC check failure.
65631	CoreFIFO HB: reset is shown as active-low, however it can be configured to active low/high in the GUI.

3.14 Resolved Issues in the v2.3 Release

Table 6 • **Resolved Issues in the v2.3 Release**

SAR Number	Changes
57411	Add support for RTG4.
60654	CoreFIFO with prefetch, single clk is not working.
60021	CoreFIFO behavior with gated clock.
60185	Timing diagrams and FWFT issue (simulation).

3.15 Resolved Issues in the v2.2 Release

Table 7 • **Resolved Issues in the v2.2 Release**

SAR Number	Changes
56536	FWFT (First Word Fall Through) FIFO implementation.
57411	Add support for RTG4.
54647	CoreFIFO does not retain data when RE is de-asserted.
55148	Data lost when data is read back after empty de-assertion.
56537	CoreFIFO issue when the pre-fetch option is checked.

3.16 Resolved Issues in the v2.1 Release

Table 8 • **Resolved Issues in the v2.1 Release**

SAR Number	Changes
51140	CoreFIFO FIFOs do not operate correctly when the prefetch option is checked.
50808	CoreFIFO simulation errors when "vhdl2008" is checked in the Libero GUI.
49361	Data output is zero from RAM when read/write enable are configured as active low.
49133	Issue with CoreFIFO during compile stage when multiple corefifos are used along with MSS in VHDL.
48624	CoreFIFO prompts error for duplicate instances in VHDL.
48300	SmartFusion2 CoreFIFO simulation is not correct.
48299	CoreFIFO 2.0.101 issue in SF2.
43498	Missing modules in Libero Design Hierarchy > Components view.

3.17 Resolved Issues in the v2.0 Release

Table 9 • **Resolved Issues in the v2.0 Release**

SAR Number	Changes
46695	One word is missing (read extra after read en de-assertion) in prefetch mode on de-asserting the rd_en and asserting it back.

3.18 Discontinued Features and Devices

There are no discontinued features for this release of CoreFIFO v2.7.

3.19 Known Limitations and Workarounds

The user testbench in CoreFIFO v2.7 release provides support for single fixed parameter configuration only.