CoreConfigP v7.1 Release Notes

These release notes accompany the production release of CoreConfigP v7.1. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

Features

Facilitates advanced peripheral bus (APB) based configuration of peripheral blocks in a SmartFusion®2 or IGLOO®2 device. The relevant peripheral blocks are the double data rate (DDR) controllers and the high speed serial interface (SERDESIF) blocks.

Interfaces

CoreConfigP has one mirrored master APB interface and several mirrored slave APB interfaces. The mirrored master interface can be connected to the microcontroller subsystem (MSS) component in the case of SmartFusion2, or the high performance memory subsystem (HPMS) component in the case of IGLOO2. The mirrored slave interfaces can be connected to the MDDR, FDDR, and SERDESIF blocks.

If the System Builder tool is used within Libero® System-on-Chip (SoC) to construct a design targeted at a SmartFusion2 or IGLOO2 device, CoreConfigP will be automatically instantiated and connected within the design if required.

Delivery Types

CoreConfigP is delivered as register transfer level (RTL) code. The core is freely available and unlicensed.

Supported Families

- SmartFusion2
- IGLOO2

Supported Tool Flows

Use Libero v11.4 software or later with CoreConfigP v7.1 release.

Installation Instructions

CoreConfigP is available through the Libero SoC IP Catalog. The core can be downloaded from a remote web-based repository to the local vault. Once installed in Libero SoC, the core can be instantiated, configured, connected, and generated using the SmartDesign tool. The System Builder tool automatically instantiates and connects CoreConfigP when constructing a design.

Known Issues and Workarounds

There are no known issues in this release.

Release History

Table 1 provides the release history of CoreConfigP.

Table 1. Release History of CoreConfigP

Version	Date	Changes
7.1	April 2016	Minor change to Configuration GUI: “090” replaced with “060 or 090”.
7.0	June 2014	Removed CLR_INIT_DONE output and Control Register 2. Removed SOFT_FAB_RESET and SOFT_USER_FAB_RESET outputs. Added SOFT_SDIF0_0_CORE_RESET and SOFT_SDIF0_1_CORE_RESET outputs. Renamed CONFIG_DONE output to CONFIG1_DONE. Added CONFIG2_DONE output. Added SDIF_RELEASED input. Added Version Register.
5.0	January 2014	Added DEVICE_090 parameter which should be set to 1 when targeting a 090 device. The SERDESIF block in a 090 device contains two PCIe controllers and setting DEVICE_090 to 1 ensures that sufficient address space is allocated to the SERDESIF_0 interface to allow both PCIe controllers to be accessed.
4.0	September 2013	Added new parameters to indicate if a particular SERDESIF block is used for PCIe. If so, additional ports appear for connection to CoreResetP. These ports allow the APB read data bus from the SERDESIF block to be monitored in CoreResetP. This provides a means to track the Link Training and Status State Machine within the SERDESIF block when in PCIe mode. A read only status register has been added to indicate which peripheral blocks (DDR controllers and SERDESIF blocks) are in use. A new control register can be optionally included to provide software control over the reset outputs from CoreResetP. When this soft reset register is included, SOFT_* outputs from CoreConfigP are available for connection to CoreResetP.
3.0	June 2013	First production release.

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