CoreConfigP v7.1

Handbook

Microsemi

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Introduction

Core Overview

CoreConfigP facilitates the configuration of peripheral blocks in a SmartFusion®2 or IGLOO®2 device. The blocks of interest are the double data rate (DDR) memory controllers and the high speed serial interface blocks (SERDESIF). CoreConfigP has a mirrored master advanced peripheral bus (APB) port and several mirrored slave APB ports. The mirrored master APB port should be connected to the FIC_2_APB_MASTER master port of the microcontroller subsystem (MSS) in the case of SmartFusion2, or the high performance memory subsystem (HPMS) in the case of IGLOO2. The mirrored slave APB ports should be connected to the APB slave ports of the blocks that need to be configured.

If the System Builder tool is used within Libero® System-on-Chip (SoC) to construct a design targeted at a SmartFusion2 or IGLOO2 device, CoreConfigP will be automatically instantiated and connected within the design if required.

Key Features

- Facilitates APB based configuration of DDR and SERDESIF peripheral blocks in a SmartFusion2 or IGLOO2 device.

Supported FPGA Families

CoreConfigP supports the following families:

- SmartFusion2
- IGLOO2

Core Version

This handbook supports CoreConfigP v7.1.

Interface Description

Parameters

The parameters present on CoreConfigP are listed in Table 1.

Table 1 CoreConfigP Parameters

Parameter	Description
MDDR_IN_USE	Set to 1 when the MDDR block is in use.
FDDR_IN_USE	Set to 1 when the FDDR block is in use.
SDIF0_IN_USE	Set to 1 when the SERDESIF_0 block is in use.
SDIF1_IN_USE	Set to 1 when the SERDESIF_1 block is in use.
SDIF2_IN_USE	Set to 1 when the SERDESIF_2 block is in use.
SDIF3_IN_USE	Set to 1 when the SERDESIF_3 block is in use.
SDIF0_PCIE	Set to 1 when the SERDESIF_0 block is used for PCIe.
SDIF1_PCIE	Set to 1 when the SERDESIF_1 block is used for PCIe.
SDIF2_PCIE	Set to 1 when the SERDESIF_2 block is used for PCIe.
SDIF3_PCIE	Set to 1 when the SERDESIF_3 block is used for PCIe.
ENABLE_SOFT_RESETS	Set to 1 to enable the SOFT_* outputs and the Soft Reset Control register. The SOFT_* outputs are intended for connection to CoreResetP where they can be used to control the assertion of various reset outputs from CoreResetP.
DEVICE_090	Set to 1 when a 060 or 090 sized device is being targeted. When DEVICE_090 = 1, the amount of address space allocated to the APB interface to the SERDESIF_0 block is increased so that the two PCIe controllers that reside in the SERDESIF_0 block on the 060 or 090 device can be accessed.

Ports

The ports present on CoreConfigP are listed in Table 2.

Table 2 CoreConfigP Ports

Port Name	Type	Description
Mirrored Master Port (connect to FIC_2_APB_MASTER interface of MSS/HPMS)		
FIC_2_APB_M_PRESET_N	Input	Active low reset
FIC_2_APB_M_PCLK	Input	Clock
FIC_2_APB_M_PSEL	Input	Select
FIC_2_APB_M_PENABLE	Input	Enable
FIC_2_APB_M_PWRITE	Input	Write/read indication

Port Name	Type	Description
FIC_2_APB_M_PADDR[16:2]	Input	Address
FIC_2_APB_M_PWDATA[31:0]	Input	Write data
FIC_2_APB_M_PRDATA[31:0]	Output	Read data
FIC_2_APB_M_PREADY	Output	Ready
FIC_2_APB_M_PSLVERR	Output	Slave error
Slave Clock and Reset (connect to peripheral blocks)		
APB_S_PCLK	Output	Clock signal to all peripheral APB interfaces
APB_S_PRESET_N	Output	Active low reset signal to all peripheral APB interfaces
Mirrored Slave Port (connect to MDDR_APB_SLAVE port of MSS/HPMS)		
MDDR_PSEL	Output	Select
MDDR_PENABLE	Output	Enable
MDDR_PWRITE	Output	Write/read indication
MDDR_PADDR[15:2]	Output	Address
MDDR_PWDATA[31:0]	Output	Write data
MDDR_PRDATA[31:0]	Input	Read data
MDDR_PREADY	Input	Ready
MDDR_PSLVERR	Input	Slave error
Mirrored Slave Port (connect to FDDR APB slave port)		
FDDR_PSEL	Output	Select
FDDR_PENABLE	Output	Enable
FDDR_PWRITE	Output	Write/read indication
FDDR_PADDR[15:2]	Output	Address
FDDR_PWDATA[31:0]	Output	Write data
FDDR_PRDATA[31:0]	Input	Read data
FDDR_PREADY	Input	Ready
FDDR_PSLVERR	Input	Slave error
Mirrored Slave Port (connect to SERDESIF_0 APB slave port)		
SDIF0_PSEL	Output	Select
SDIF0_PENABLE	Output	Enable
SDIF0_PWRITE	Output	Write/read indication
SDIF0_PADDR[15:2]	Output	Address
SDIF0_PWDATA[31:0]	Output	Write data
SDIF0_PRDATA[31:0]	Input	Read data
SDIF0_PREADY	Input	Ready
SDIF0_PSLVERR	Input	Slave error

Port Name	Type	Description
Mirrored Slave port (connect to SERDESIF_1 APB slave port)		
SDIF1_PSEL	Output	Select
SDIF1_PENABLE	Output	Enable
SDIF1_PWRITE	Output	Write/read indication
SDIF1_PADDR[15:2]	Output	Address
SDIF1_PWDATA[31:0]	Output	Write data
SDIF1_PRDATA[31:0]	Input	Read data
SDIF1_PREADY	Input	Ready
SDIF1_PSLVERR	Input	Slave error
Mirrored Slave Port (connect to SERDESIF_2 APB slave port)		
SDIF2_PSEL	Output	Select
SDIF2_PENABLE	Output	Enable
SDIF2_PWRITE	Output	Write/read indication
SDIF2_PADDR[15:2]	Output	Address
SDIF2_PWDATA[31:0]	Output	Write data
SDIF2_PRDATA[31:0]	Input	Read data
SDIF2_PREADY	Input	Ready
SDIF2_PSLVERR	Input	Slave error
Mirrored Slave port (connect to SERDESIF_3 APB slave port)		
SDIF3_PSEL	Output	Select
SDIF3_PENABLE	Output	Enable
SDIF3_PWRITE	Output	Write/read indication
SDIF3_PADDR[15:2]	Output	Address
SDIF3_PWDATA[31:0]	Output	Write data
SDIF3_PRDATA[31:0]	Input	Read data
SDIF3_PREADY	Input	Ready
SDIF3_PSLVERR	Input	Slave error
Signals (connect to CoreResetP)		
CONFIG1_DONE	Output	Indicates the completion of the first stage of configuration to CoreResetP.
CONFIG2_DONE	Output	Indicates the completion of the second stage of configuration to CoreResetP
SDIF_RELEASED	Input	Indication from CoreResetP that SERDESIF blocks have been released from reset.
INIT_DONE	Input	Indicates the completion of initialization from CoreResetP.
SOFT_EXT_RESET_OUT	Output	This signal is controlled by bit 0 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its EXT_RESET_OUT output.

Port Name	Type	Description
SOFT_RESET_F2M	Output	This signal is controlled by bit 1 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its RESET_N_F2M output.
SOFT_M3_RESET	Output	This signal is controlled by bit 2 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its M3_RESET_N output.
SOFT_MDDR_DDR_AXI_S_CORE_RESET	Output	This signal is controlled by bit 3 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its MDDR_DDR_AXI_S_CORE_RESET_N output.
SOFT_FDDR_CORE_RESET	Output	This signal is controlled by bit 6 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its FDDR_CORE_RESET_N output.
SOFT_SDIF0_PHY_RESET	Output	This signal is controlled by bit 7 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its SDIF0_PHY_RESET_N output.
SOFT_SDIF0_CORE_RESET	Output	This signal is controlled by bit 8 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its SDIF0_CORE_RESET_N output.
SOFT_SDIF1_PHY_RESET	Output	This signal is controlled by bit 9 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its SDIF1_PHY_RESET_N output.
SOFT_SDIF1_CORE_RESET	Output	This signal is controlled by bit 10 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its SDIF1_CORE_RESET_N output.
SOFT_SDIF2_PHY_RESET	Output	This signal is controlled by bit 11 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its SDIF2_PHY_RESET_N output.
SOFT_SDIF2_CORE_RESET	Output	This signal is controlled by bit 12 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its SDIF2_CORE_RESET_N output.
SOFT_SDIF3_PHY_RESET	Output	This signal is controlled by bit 13 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its SDIF3_PHY_RESET_N output.
SOFT_SDIF3_CORE_RESET	Output	This signal is controlled by bit 14 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its SDIF3_CORE_RESET_N output.
SOFT_SDIF0_0_CORE_RESET	Output	This signal is controlled by bit 15 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its SDIF0_0_CORE_RESET_N output.
SOFT_SDIF0_1_CORE_RESET	Output	This signal is controlled by bit 16 of the Soft Reset Control register and is intended for connection to CoreResetP to allow software control over its SDIF0_1_CORE_RESET_N output.

Note: All signals in this table are active high unless otherwise stated.

Tool Flows

SmartDesign

Figure 1 shows how the CoreConfigP is typically connected in a SmartDesign design.

Note: The mirrored slave ports of CoreConfigP are peripheral specific; that is, each port should be connected to a particular peripheral block as indicated by port names. In SmartDesign, hovering over the mirrored slave ports (labeled S) on the CoreConfigP symbol with the mouse pointer shows the names of signals. For example, the port with signal names matching MDDR_* should be connected to the MDDR APB configuration port (labeled MDDR_APB_SLAVE on the MSS symbol for SmartFusion2 and HPMS symbol for IGLOO2).

If the System Builder tool is used within Libero® System-on-Chip (SoC) to construct a design targeted at the SmartFusion2 or IGLOO2 device, CoreConfigP will be automatically instantiated and connected within the design if required.

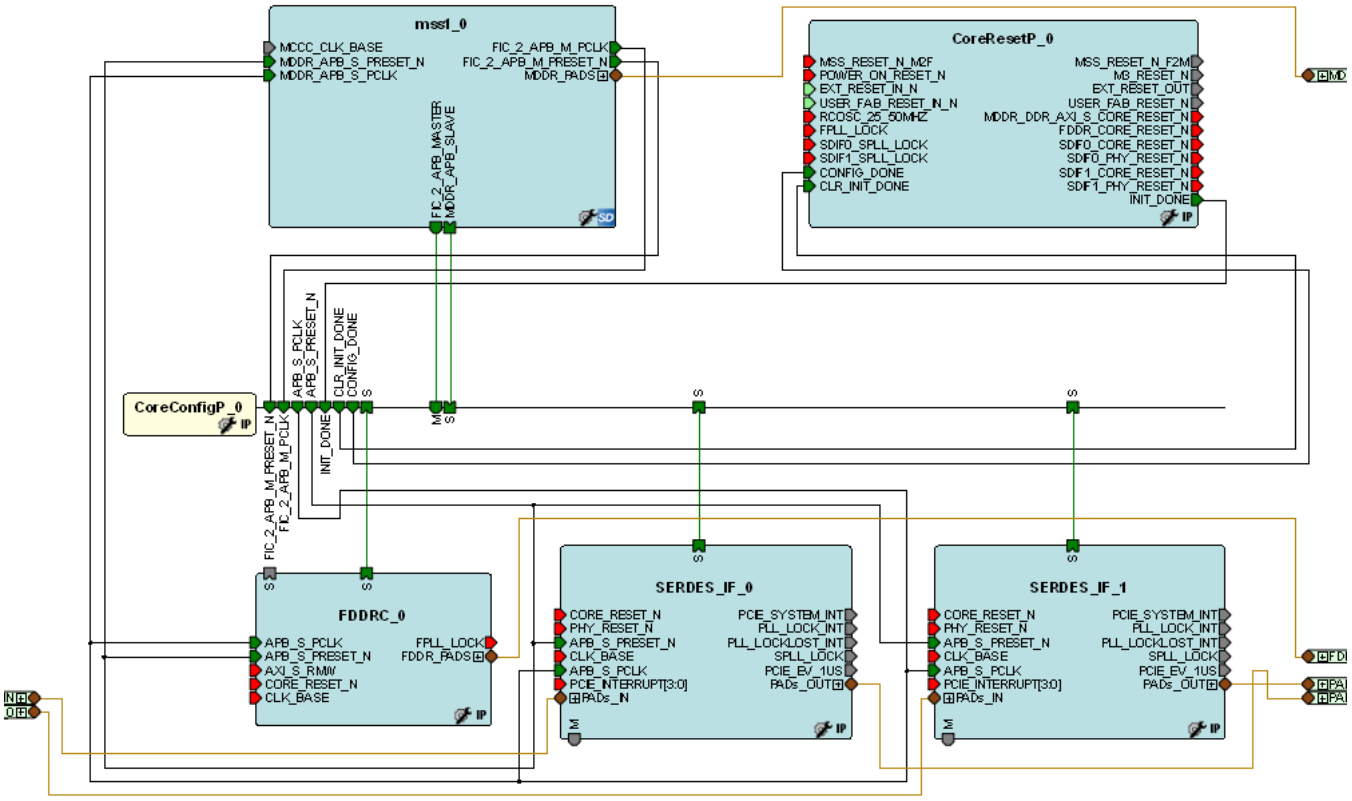

Figure 1 Connecting CoreConfigP in SmartDesign

Configuring CoreConfigP in SmartDesign

The CoreConfigP GUI is shown in Figure 2. Check boxes allow selection of peripheral blocks that will be in use. If a peripheral block is not in use, the ports related to that block do not appear for connection on the CoreConfigP symbol.

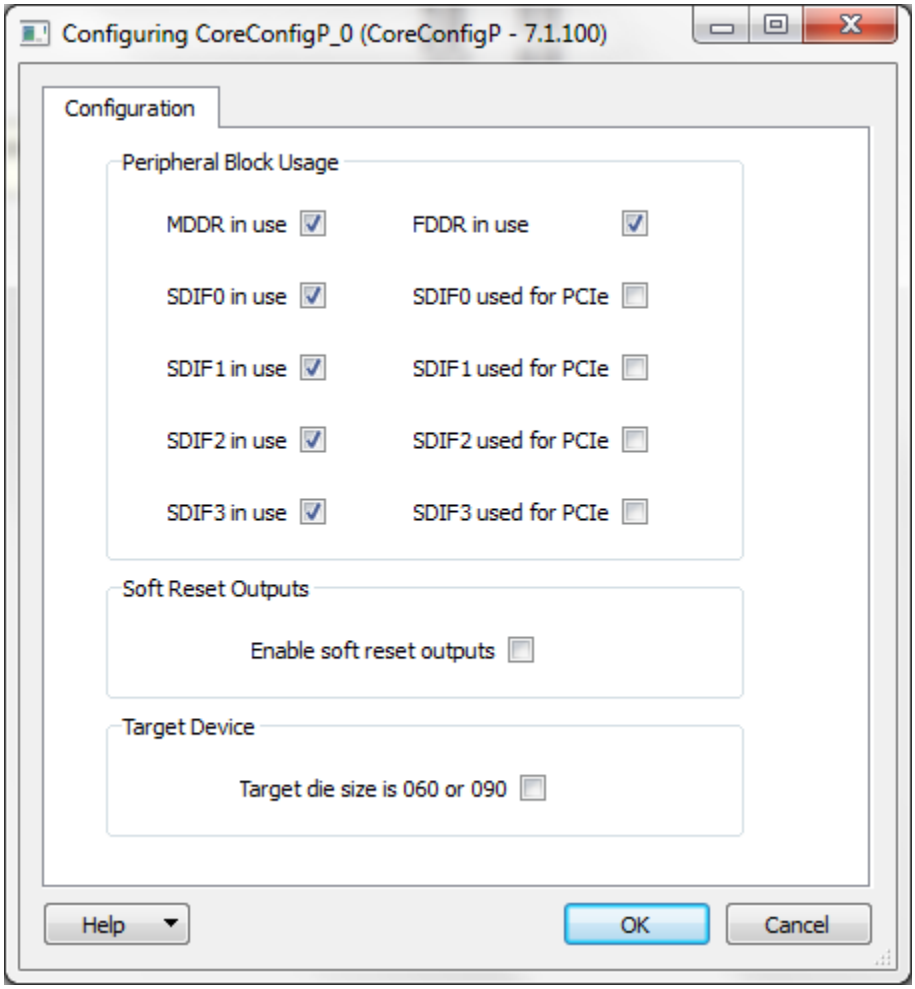

Figure 2 CoreConfigP Configuration GUI

Memory Map

In the SmartFusion2 microcontroller subsystem (MSS) or IGLOO2 high performance memory subsystem (HPMS) memory map, accesses in the address range 0x40020800 to 0x4002FFFF are propagated to the FIC_2_APB_MASTER interface of the MSS or HPMS. Table 3 shows the address ranges for the peripheral blocks when CoreConfigP is mastered by the FIC_2_APB_MASTER interface.

In a 060 or 090 sized device, the DEVICE_090 parameter should be set to 1. This has the effect of increasing the address space allocated to the SERDESIF_0 interface, allowing the two PCIe controllers that exist in the SERDESIF block of a 060 or 090 device to be addressed through the SERDESIF_0 interface.

Table 3 CoreConfigP Address Map

DEVICE_090 Parameter	Address Range	Description
0	0x40020800 – 0x40020FFF	MDDR
	0x40021000 – 0x400217FF	FDDR
	0x40022000 – 0x40023FFF	Internal control and status registers, described under Control and Status Registers section
	0x40024000 – 0x40027FFF	Reserved
	0x40028000 – 0x4002A3FF	SERDESIF_0
	0x4002C000 – 0x4002E3FF	SERDESIF_1
	0x40030000 – 0x400323FF	SERDESIF_2
	0x40034000 – 0x400363FF	SERDESIF_3
1	0x40020800 – 0x40020FFF	MDDR
	0x40021000 – 0x400217FF	FDDR
	0x40022000 – 0x40023FFF	Internal control and status registers, described under Control and Status Registers section
	0x40024000 – 0x40027FFF	Reserved
	0x40028000 – 0x4002E3FF	SERDESIF_0

Control and Status Registers

Control Register 1

Address : 0x40022000
Access : Read/write
Reset state : 0x00000000

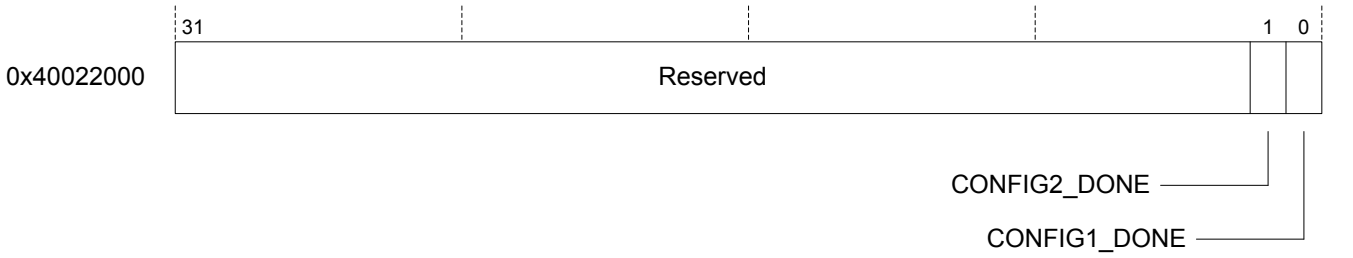

Figure 3 Control Register 1

Table 4 describes the fields of Control Register 1.

Table 4 Control Register 1 Bit Assignments

Bits	Field	Function
[31:2]	-	Reserved
[1]	CONFIG2_DONE	Controls the CONFIG2_DONE output of the core.
[0]	CONFIG1_DONE	Controls the CONFIG1_DONE output of the core.

Status Register

Address : 0x40022004
Access : Read only
Reset state : 0x00000000

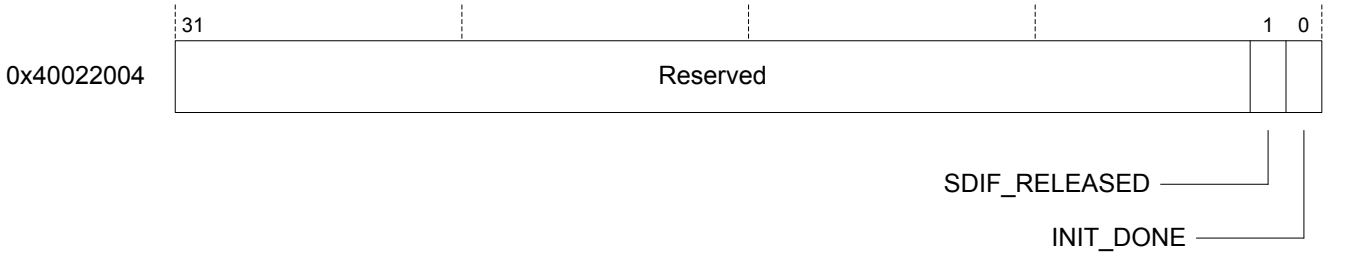

Figure 4 Status Register

Table 5 describes the fields of the Status Register.

Table 5 Status Register Bit Definitions

Bits	Field	Function
[31:2]	-	Reserved
[1]	SDIF_RELEASED	Indicates the logic level on the SDIF_RELEASED input to the core. Normally, this input is connected to the SDIF_RELEASED output of CoreResetP.
[0]	INIT_DONE	Indicates the logic level on the INIT_DONE input to the core. Normally, this input is connected to the INIT_DONE output of CoreResetP.

Configuration Status Register

Address : 0x4002200C
Access : Read Only
Reset state : Depends on the settings for parameters mentioned in Table 6.

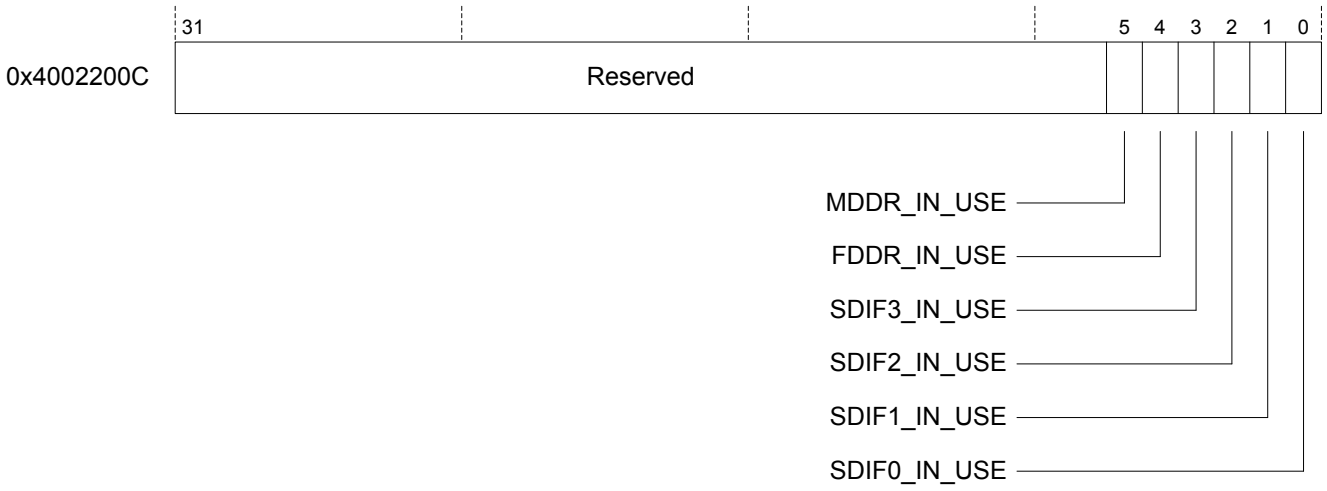

Figure 5 Configuration Status Register

Table 6 describes the fields of the Configuration Status Register.

Table 6 Configuration Status Register Bit Definitions

Bits	Field	Function
[31:6]	-	Reserved
[5]	MDDR_IN_USE	This bit reads as 1 when the MDDR_IN_USE parameter is set to 1, indicating that the MDDR block is in use.
[4]	FDDR_IN_USE	This bit reads as 1 when the FDDR_IN_USE parameter is set to 1, indicating that the FDDR block is in use.
[3]	SDIF3_IN_USE	This bit reads as 1 when the SDIF3_IN_USE parameter is set to 1, indicating that the SERDESIF_3 block is in use.
[2]	SDIF2_IN_USE	This bit reads as 1 when the SDIF2_IN_USE parameter is set to 1, indicating that the SERDESIF_2 block is in use.
[1]	SDIF1_IN_USE	This bit reads as 1 when the SDIF1_IN_USE parameter is set to 1, indicating that the SERDESIF_1 block is in use.
[0]	SDIF0_IN_USE	This bit reads as 1 when the SDIF0_IN_USE parameter is set to 1, indicating that the SERDESIF_0 block is in use.

Soft Reset Control Register

Address : 0x40022010
Access : Read/write
Reset state : 0x00000000

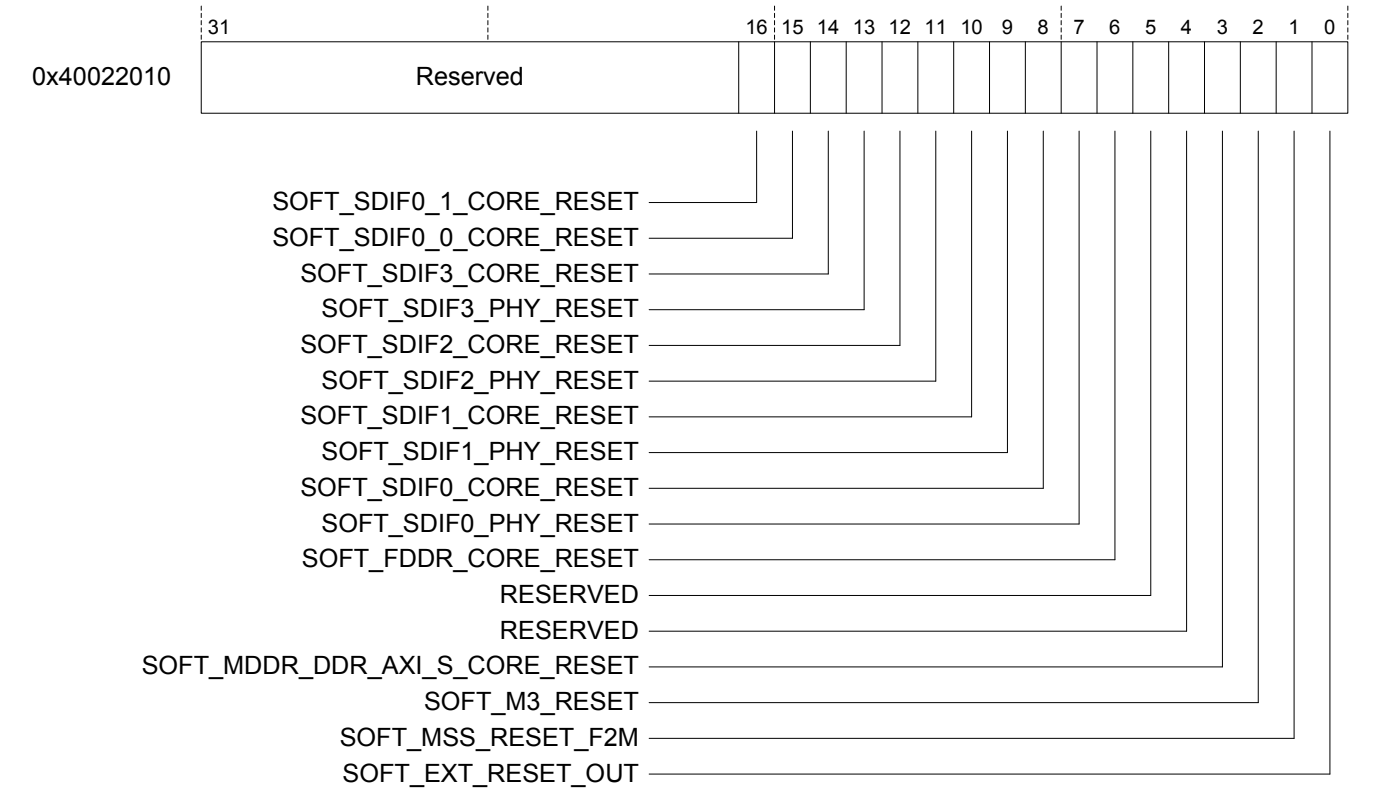

Figure 6 Soft Reset Control Register

Table 7 describes the fields of the Soft Reset Control Register.

Table 7 Soft Reset Control Register Bit Definitions

Bits	Field	Function
[31:17]	-	Reserved
[16]	SOFT_SDIF0_1_CORE_RESET	This bit controls the SOFT_SDIF0_1_CORE_RESET output.
[15]	SOFT_SDIF0_0_CORE_RESET	This bit controls the SOFT_SDIF0_0_CORE_RESET output.
[14]	SOFT_SDIF3_CORE_RESET	This bit controls the SOFT_SDIF3_CORE_RESET output.
[13]	SOFT_SDIF3_PHY_RESET	This bit controls the SOFT_SDIF3_PHY_RESET output.
[12]	SOFT_SDIF2_CORE_RESET	This bit controls the SOFT_SDIF2_CORE_RESET output.
[11]	SOFT_SDIF2_PHY_RESET	This bit controls the SOFT_SDIF2_PHY_RESET output.
[10]	SOFT_SDIF1_CORE_RESET	This bit controls the SOFT_SDIF1_CORE_RESET output.
[9]	SOFT_SDIF1_PHY_RESET	This bit controls the SOFT_SDIF1_PHY_RESET output.
[8]	SOFT_SDIF0_CORE_RESET	This bit controls the SOFT_SDIF0_CORE_RESET output.
[7]	SOFT_SDIF0_PHY_RESET	This bit controls the SOFT_SDIF0_PHY_RESET output.
[6]	SOFT_FDDR_CORE_RESET	This bit controls the SOFT_FDDR_CORE_RESET output.
[5]	-	Reserved
[4]	-	Reserved
[3]	SOFT_MDDR_DDR_AXI_S_CORE_RESET	This bit controls the SOFT_MDDR_DDR_AXI_S_CORE_RESET output.
[2]	SOFT_M3_RESET	This bit controls the SOFT_M3_RESET output.
[1]	SOFT_RESET_F2M	This bit controls the SOFT_RESET_F2M output.
[0]	SOFT_EXT_RESET_OUT	This bit controls the SOFT_EXT_RESET_OUT output.

Version Register

Address : 0x40022014
Access : Read only
Reset state : 0x00070000

Figure 7 Version Register

Table 8 Version Register Bit Definitions

Bits	Field	Function
[31:16]	Major version number	Major version number of core.
[15:0]	Minor version number	Minor version number of core.

List of Changes

The following table shows the important changes made in this document for each revision.

Date	Change	Page
April 2016	CoreConfigP v7.1 release.	N/A
June 2014	CoreConfigP v7.0 release.	N/A
January 2014	CoreConfigP v5.0 release.	N/A
June 2013	CoreConfigP v3.0 release.	N/A

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