

CoreConfigMaster v2.1 Release Notes

These release notes accompany the production release of CoreConfigMaster v2.1. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

Features

CoreConfigMaster can be used to drive the configuration of peripheral blocks in a SmartFusion[®]2 or IGLOO[®]2 device. The peripheral blocks of interest are the double data rate (DDR) controllers, and the high speed serial interface (SERDESIF) blocks.

CoreConfigMaster fetches information stored in the embedded nonvolatile memory (eNVM), processes this information, and writes configuration data to the relevant blocks.

Interfaces

CoreConfigMaster masters the configuration process using an advanced high-performance bus (AHB)-Lite master interface. This interface should be connected via CoreAHBLite to the fabric interface controller 0 (FIC_0) interface of the microcontroller subsystem (MSS) in a SmartFusion2 device, or high performance memory system (HPMS) in an IGLOO2 device.

If the System Builder tool is used within Libero[®] System-on-Chip (SoC) to construct a design targeted at a SmartFusion2 or IGLOO2 device, CoreConfigMaster will be automatically instantiated, configured and connected within the design if required.

Supported Families

- SmartFusion2
- IGLOO2

Supported Tool Flows

Use Libero v11.4 software or later with CoreConfigMaster v2.1 release.

Installation Instructions

CoreConfigMaster is available through the Libero SoC IP Catalog. The core can be downloaded from a remote web-based repository to the local vault. Once installed in Libero SoC, the core can be instantiated, configured, connected, and generated using the SmartDesign tool. The System Builder tool automatically instantiates, configures and connects CoreConfigMaster when constructing a design.

Known Issues and Workarounds

There are no known issues in this release.



Release History

Table 1 provides the release history of CoreConfigMaster.

Version	Date	Changes
2.1	June 2014	Some additional processing capabilities have been added to the core to support setting and clearing of register bits. Libero v11.4 or later is required for this version of the core.
2.0	June 2013	First production release



Microsemi Corporate Headquarters One Enterprise, Aliso Viejo CA 92656 USA Within the USA: +1(949) 380-6100 Sales: +1 (949) 380-6136 Fax: +1 (949) 215-4996 E-mail: sales.support@microsemi.com Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense and security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices, and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,400 employees globally. Learn more at **www.microsemi.com**.

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