CoreConfigMaster v2.1

Handbook

Microsemi

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Introduction

Core Overview

CoreConfigMaster can be used to drive the configuration of peripheral blocks in a SmartFusion®2 or IGLOO®2 device. The peripheral blocks of interest are the double data rate (DDR) controllers, and the high speed serial interface (SERDESIF) blocks.

CoreConfigMaster masters the configuration process using an advanced high-performance bus (AHB)-Lite master interface. This interface should be connected through CoreAHBLite to the fabric interface controller 0 (FIC_0) interface of the microcontroller subsystem (MSS) in a SmartFusion2 device, or high performance memory system (HPMS) in an IGLOO2 device. CoreConfigMaster fetches information stored in the embedded nonvolatile memory (eNVM), processes this information, and writes configuration data to the relevant blocks. The peripheral blocks are accessed through the MSS or HPMS component. That is, CoreConfigMaster writes configuration data to the FIC_2_APB_MASTER interface of the MSS or HPMS through the FIC_0 interface. A CoreConfigP instance connected to the FIC_2_APB_MASTER interface takes care of routing the configuration data to the peripherals. Figure 1 shows how the various cores are connected. The System Builder tool will automatically instantiate, configure and connect CoreConfigMaster when it is required in a system.

Key Features

- Masters configuration of DDR and SERDESIF peripheral blocks in a SmartFusion2 or IGLOO2 device.

Supported Microsemi® FPGA Families

CoreConfigMaster supports the following families:

- SmartFusion2
- IGLOO2

Core Version

This handbook supports CoreConfigMaster v2.1.

Interface Description

Ports

The ports present on CoreConfigMaster are listed in Table 1.

Table 1 CoreConfigMaster Ports

Port Name	Type	Description
HRESETN	Input	Active low reset
HCLK	Input	Clock
HADDR[31:0]	Output	Address
HSIZE[2:0]	Output	Size of transfer
HTRANS[1:0]	Output	Transfer type
HWRITE	Output	Write indication
HWDATA[31:0]	Output	Write data
HMASTLOCK	Output	Lock indication
HBURST[2:0]	Output	Burst type
HPROT[3:0]	Output	Protection control signals
HRDATA[31:0]	Input	Read data
HREADY	Input	Ready indication

Note: All signals in this table are active high unless otherwise stated.

SmartDesign

Figure 1 shows CoreConfigMaster is typically connected in a SmartDesign design. When System Builder is used to construct a design, it will automatically instantiate, configure and connect CoreConfigMaster when it is required.

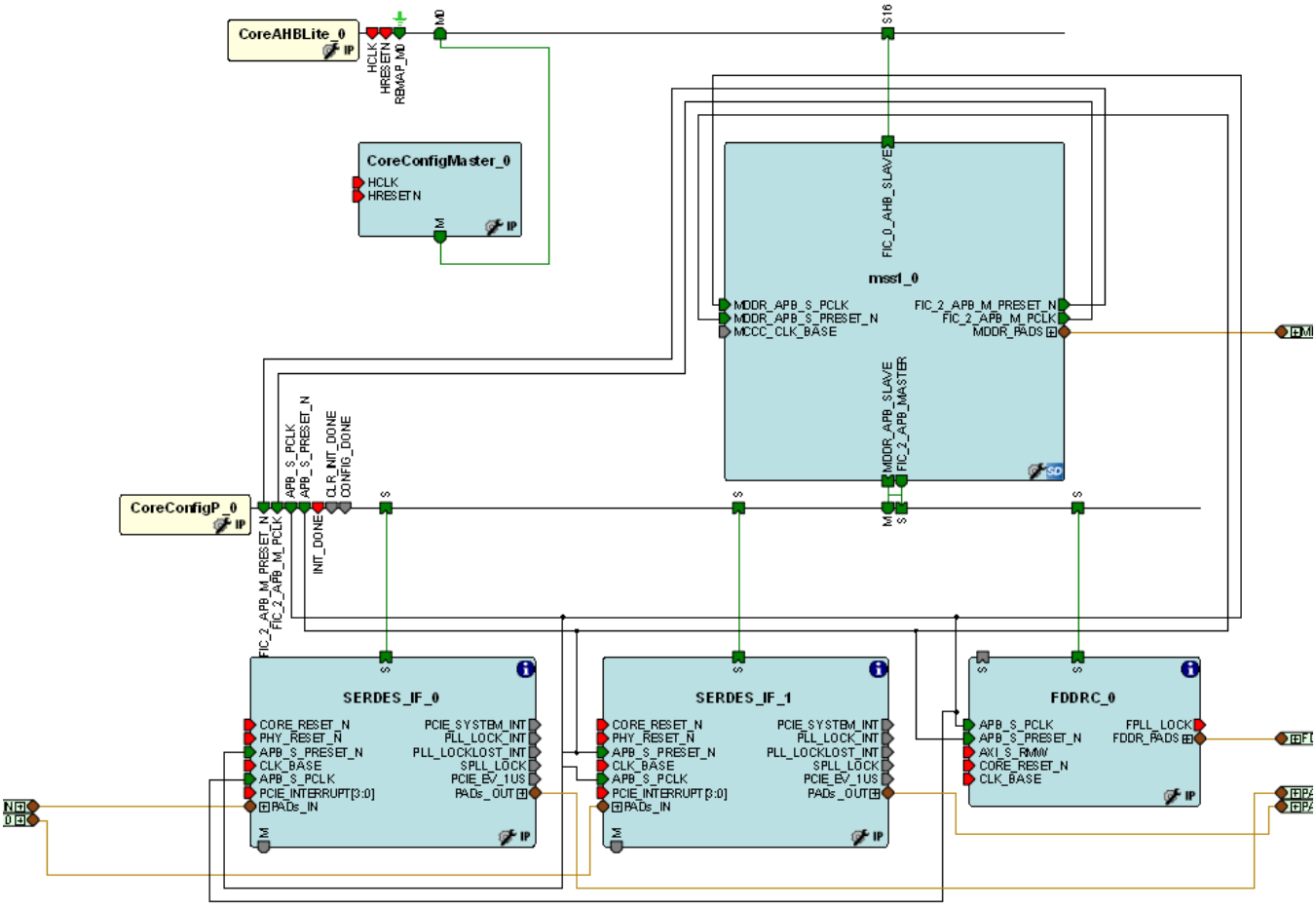

Figure 1 Connecting CoreConfigMaster in SmartDesign

Configuring CoreConfigMaster in SmartDesign

The CoreConfigMaster configuration GUI is shown in Figure 2. The only information required by the core is the location in the address space where the configuration data begins. This should be entered as a decimal integer. CoreConfigMaster begins fetching data from the value entered.

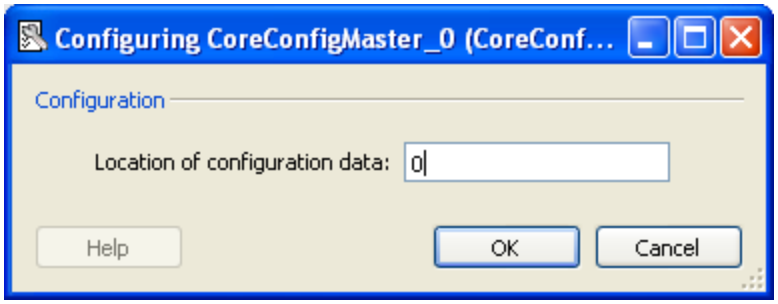

Figure 2 CoreConfigMaster Configuration GUI

List of Changes

Figure 3 The following table lists critical changes that were made in each revision of the document.

Date	Change	Page
June 2014	CoreConfigMaster v2.1 release.	N/A
June 2013	CoreConfigMaster v2.0 release.	N/A

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