CoreAXI v3.2 Release Notes

This is the production release for CoreAXI v3.2 IP core. This release notes provides details about the features, supported families, system requirements, implementations, and known limitations and workarounds.

Key Features

Following are the CoreAXI v3.2 features

- Multi-master AXI interconnect with support up to four AXI masters
- All masters support connectivity to all 16 slaves
- Supports additional 17th slave when the huge slave or combined region is in use
- Provides 256 bytes to 256 MB of address space for each slave (Huge slave occupies 2 GB address space)
- Supports allocation of slave slots to a combined region slave interface
- AXI interface address width of 32-bits and data bus width of 64-/128-/256-bits
- Supports increment and wrap type bursts
- Round-robin arbitration scheme
- FEED_THROUGH mode for single slave and single master configuration
- Configurable register pipelining at the input and/or output stage
- Supports Outstanding write transactions:
  - Support for ID fields to provide additional information on the ordering requirements during write transactions. Transaction ordering rules must be followed.
  - Configurable Write transaction acceptance limits. Supports maximum of four multiple outstanding write transactions
  - Supports write response re-ordering
- The following v2.0 features are retained in v3.2:
  - Support for ID fields to provide additional information on the ordering requirements during read transactions
  - Support for Out-of-Order completion for read transaction. Transaction ordering rules must be followed.
  - Support maximum of four multiple outstanding read transactions to the same slave

Delivery Types

CoreAXI is licensed as a register transfer level (RTL).

RTL

Only Verilog RTL source code is provided for the core and test benches.

Supported Families

- RTG4™
- SmartFusion®2
- IGLOO®2

Supported Tool Flows

Libero System-on-Chip (SoC) software v11.5 or later supports the CoreAXI release.

Installation Instructions

For the RTL version of the core, the license is not required before the core can be exported.

Consult the *Libero SoC online help* for instructions on core installation and licensing.

Documentation

This release contains a copy of the *CoreAXI handbook*, which describes the core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and provides implementation suggestions.

For more information about Intellectual Property, visit: http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores. For updates and additional information about software, FPGAs, and hardware, visit: www.microsemi.com.

Supported Test Environments

- Verilog user testbench

Release History

There are resolved issues in the v3.2 release.

Table 1 Release History

Version	Date	Changes
3.2	December 2015	As listed in Table 2
3.1	April 2015	As listed in Table 3
3.0	May 2014	As listed in Table 4
2.1	September 2013	As listed in Table 5
2.0	January 2013	Initial release

Resolved Issues in the v3.2 Release

Table 2 Resolved SARs in CoreAXI v3.2 Release

SAR	Description
67448	Enhancement Request: RN should include dependencies to use the core
62204	Testbench should have relative path for the coreparamater
68165	Min Libero Version should not be 11.5.5
68816	CoreAXI does not work when it is Single master single slave mode if FEEDTHROUGH is not selected
69878	CoreAXI: support for outstanding write transaction
70361	AXI master and slave code doesn't have similar behavior for Address

Resolved Issues in the v3.1 Release

Table 3 Resolved SARs in CoreAXI v3.1 Release

SAR	Description
66253	Add support for RTG4
63022	CoreAXI display name should arguably be "CoreAXI" and not "COREAXI"
57930	Typos in Temp grade metadata

Resolved Issues in the v3.0 Release

Table 4 Resolved SARs in CoreAXI v3.0 Release

SAR	Description
53137	Add support for 128-bit and 256-bit data widths
53138	Add multi-master support
53435	Slave address space needs to be increased above, 256 MB

Resolved Issues in the v2.1 Release

Table 5 Resolved SARs in CoreAXI v2.1 Release

SAR	Description
49706	Misc packaging issues for CoreAXI 2.0.104
50274	CoreAXI does not pass write data through write data channel
50407	CoreAXI version 2.0.104 does not work in either HDL sim or on hardware

Discontinued Features and Devices

The CoreAXI v3.2 release contains only Verilog non-obfuscated support.

Known Limitations and Workarounds

- Write data interleaving and write data out-of-order is not supported.
- The low power interface of AXI is not supported.
- CoreAXI does not support locked transactions.
- The CoreAXI expects AWREADY before WREADY. Slaves connected to CoreAXI must acknowledge acceptance of write addresses by asserting AWREADY before acknowledging acceptance of the related write data by asserting WREADY.
- Outstanding read transactions to different slave with same ID value are not supported.
- Only four ID values are available per master.

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