CoreAPBSRAM v2.0 Release Notes

This is the production release for CoreAPBSRAM v2.0. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

Intended Use

CoreAPBSRAM provides an advanced microcontroller bus architecture (AMBA) advanced peripheral bus (APB) interface to the embedded SRAM blocks within IGLOO®, ProASIC®3, and Fusion families of devices. APB masters read from and write to the memory resources of the SRAM blocks through the APB slave interface of CoreAPBSRAM.

Key Features

- Fully AMBA 2 APB compliant
- Compatible with AMBA 3 APB
- Ability to logically merge multiple SRAM blocks into one large area of SRAM
- Configurable 8-, 16-, 24- or 32-bit data width
- Size of SRAM is configurable from 512 locations to 8192 locations (for 32- or 24-bit data width), or 16384 locations (for 16-bit data width), or 32768 locations (for 8-bit data width)

Interfaces

CoreAPBSRAM contains an AMBA APB slave interface to connect to AMBA-based systems.

Delivery Types

CoreAPBSRAM is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero® Integrated Design Software (IDE). The RTL code for the core is obfuscated.

This core is licensed as part of the default Libero IDE license set and no additional license is required.

RTL

Complete RTL source code is provided for the core

Supported Families

- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3E
- ProASIC3L
- Fusion

Supported Tool Flows

This version of the core requires Libero IDE v8.4 SP1 or later.

Installation Instructions

The CoreAPBSRAM CCZ file must be installed into Libero IDE. Within Libero IDE, click the **Add Core** button in the Catalog to locate and install a local CCZ file, or use the automatic web update feature in Libero IDE. Once the CCZ file is installed in Libero IDE, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE project.

Refer to the Libero IDE online help for further instructions on core installation, licensing, and general use.

Documentation

This release contains a copy of the CoreAPBSRAM handbook. The CoreAPBSRAM handbook describes the core functionality and describes how to use the core.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Actel website at www.actel.com.

Release History

Table 1 provides the release history of CoreAPBSRAM.

Table 1 · Release History of CoreAPBSRAM

Version	Date	Changes
2.0	January 2009	First production release of the core

Known Issues and Workarounds

There are no known issues or workarounds with the CoreAPBSRAM v2.0 release

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