

CoreAPBSRAM v2.0

Handbook

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Introduction

Core Overview

CoreAPBSRAM enables advanced microcontroller bus architecture (AMBA) advanced peripheral bus (APB) access to the embedded SRAM blocks within the IGLOO[®] series, ProASIC[®]3 series, and Fusion devices. The core can logically group a number of SRAM blocks into a single large block of SRAM. The amount of SRAM can be configured to range from 512 bytes to 32,768 bytes. The number of SRAM blocks available, and therefore the maximum size of SRAM which can be configured, depends on the device being targeted. Refer to the device family datasheets available on the Actel website at www.actel.com for information on the amount of SRAM available on each device.

Figure 1 shows a block diagram of CoreAPBSRAM.

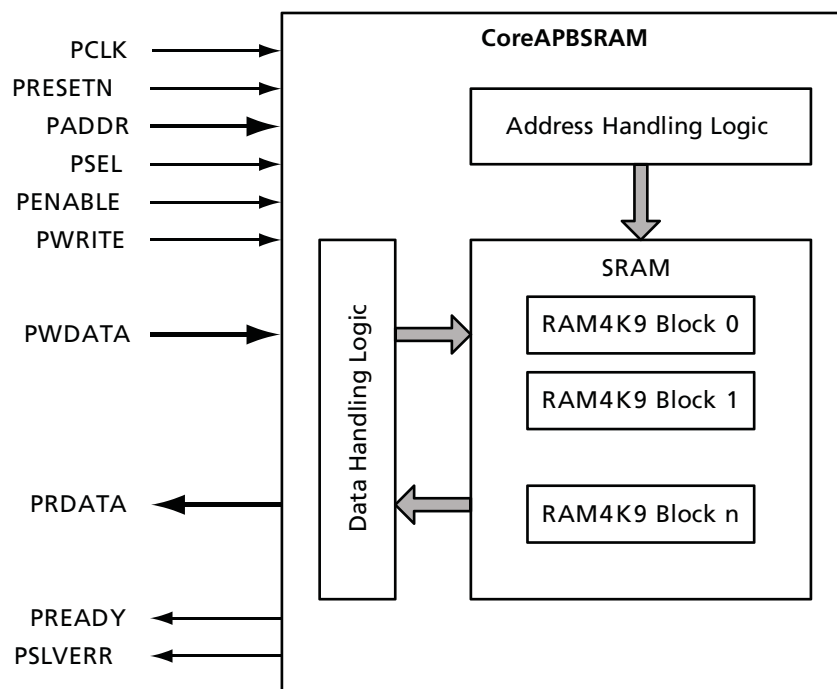


Figure 1 · CoreAPBSRAM Block Diagram

Key Features

- Fully AMBA 2 APB compliant
- Compatible with AMBA 3 APB
- Ability to logically merge multiple SRAM blocks into one large area of SRAM
- Configurable 8-, 16-, 24-, or 32-bit data width
- Size of SRAM is configurable from 512 locations to 8,192 locations for 32- or 24-bit data width, 16,384 locations for 16-bit data width, or 32,768 locations for 8-bit data width

Supported Families

The following device families are supported by CoreAPBSRAM:

- IGLOO
- IGLOOe
- IGLOO PLUS
- ProASIC3
- ProASIC3E
- ProASIC3L
- Fusion

Device Utilization and Performance

Table 1 lists tile counts and RAM block usage, as well as performance figures for various configurations of CoreAPBSRAM. Table 1 does not cover every possible configuration, but lists a range of configurations which should give a good indication of the expected resource usage and performance of the core.

Table 1 · CoreAPBSRAM Device Utilization and Performance

Configuration		Resource Usage and Performance		
APB_DWIDTH	Number of Locations	Number of RAM Blocks	Number of Tiles	Performance (MHz)
8	512	1	11	250
8	4,096	8	11	227
8	8,192	16	37	232
8	12,288	24	61	222
8	16,384	32	57	250
8	20,480	40	74	250
8	24,576	48	91	250
8	28,672	56	92	250
8	32,678	64	111	250
16	512	2	19	248
16	2,048	8	19	233
16	4,096	16	32	236
16	8,192	32	55	250
16	10,240	40	61	250
16	12,288	48	70	250
16	14,336	56	93	250
16	16,384	64	97	250

Table 1 · CoreAPBSRAM Device Utilization and Performance (continued)

Configuration		Resource Usage and Performance		
APB_DWIDTH	Number of Locations	Number of RAM Blocks	Number of Tiles	Performance (MHz)
24	512	3	2	249
24	1,024	6	2	239
24	2,048	12	2	224
24	3,072	18	46	219
24	4,096	24	28	215
24	5,120	30	52	250
24	6,144	36	55	250
24	7,168	42	84	250
24	8,192	48	61	250
32	512	4	2	239
32	1,024	8	2	227
32	2,048	16	14	229
32	3,072	24	65	250
32	4,096	32	19	250
32	5,120	40	70	250
32	6,144	48	75	250
32	7,168	56	111	250
32	8,192	64	81	250

Note: Data in this table were obtained for an A3PE3000 device, speed grade -2. The resource usage and performance figures are applicable for both ADDR_SCHEME = 0 (word aligned addressing) and ADDR_SCHEME = 1 (sequential addressing).

Supported Interfaces

CoreAPBSRAM has an AMBA 2 APB slave interface with PREADY and PSLVERR signals for AMBA 3 APB compatibility. [Figure 1-1](#) shows APB write transfers and [Figure 1-2](#) shows read transfers.

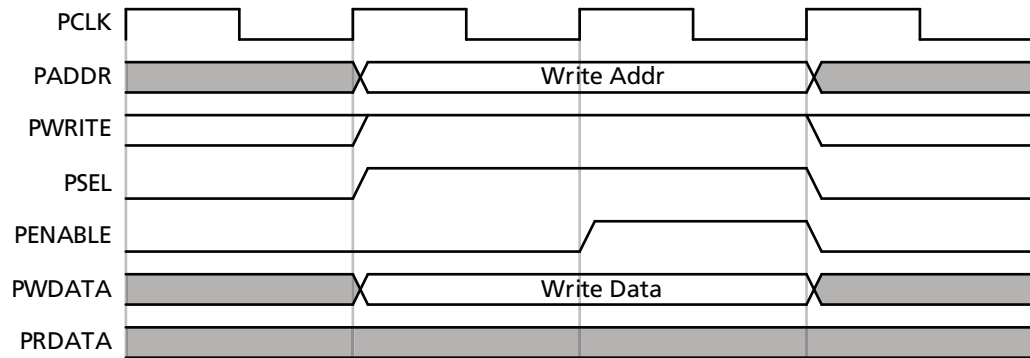


Figure 1-1 · APB Write Transfer

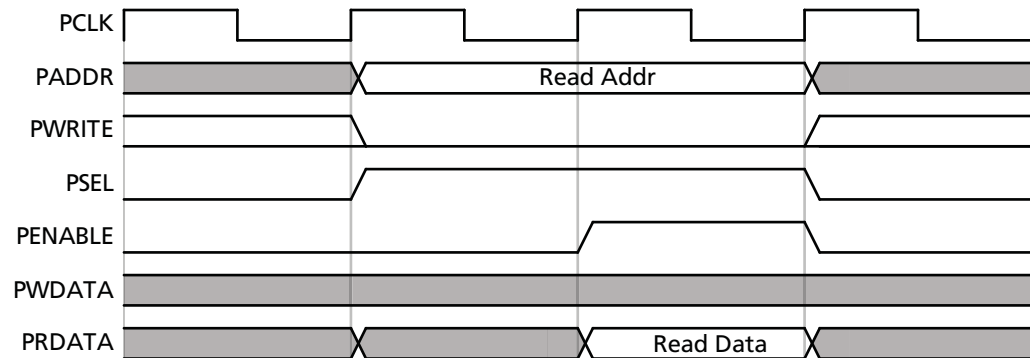


Figure 1-2 · APB Read Transfer

Tool Flows

SmartDesign

CoreAPBSRAM is available for download to the SmartDesign IP Catalog via the Libero® Integrated Design Environment (IDE) web repository. For information on using SmartDesign to instantiate, configure, connect, and generate cores, refer to the Libero IDE online help.

Figure 2-1 shows the CoreAPBSRAM configuration window, as well as cross references to the corresponding top-level parameters.

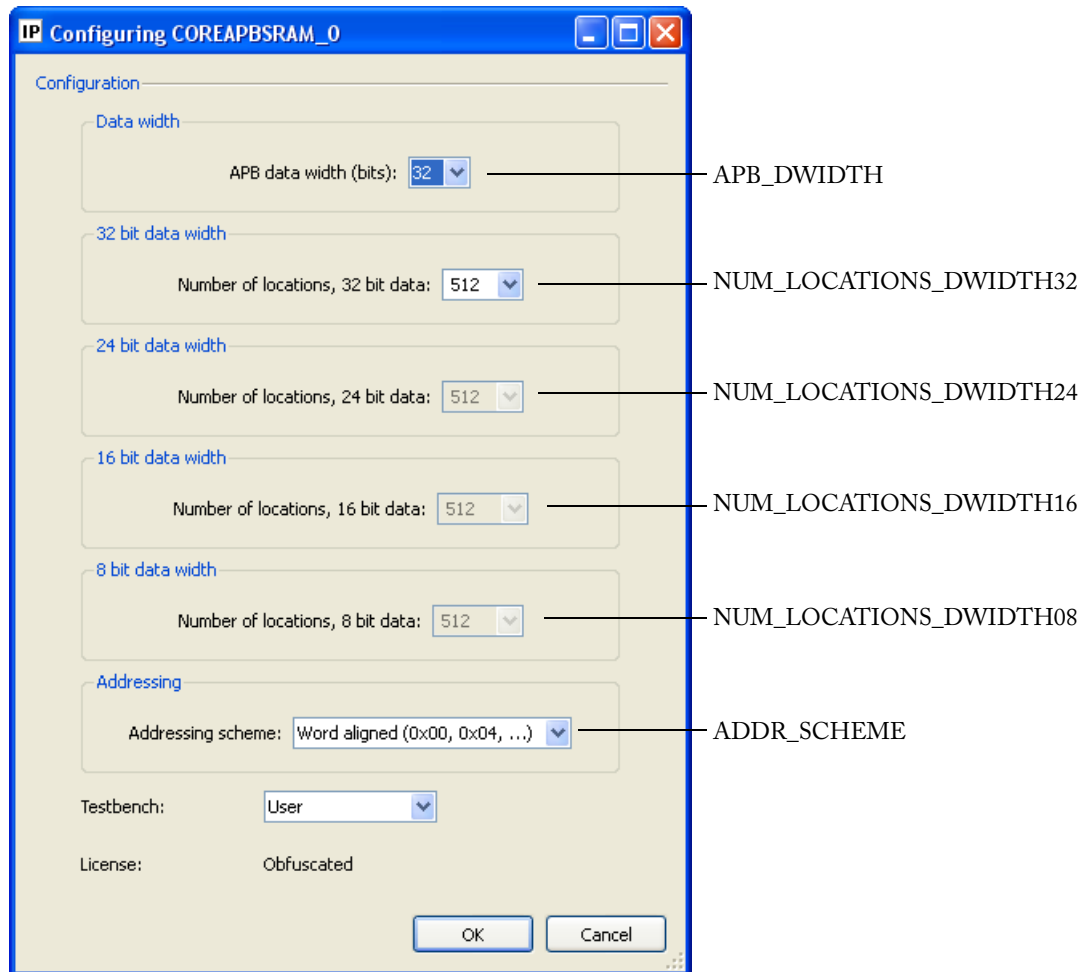


Figure 2-1 · CoreAPBSRAM Configuration Window

You can select an APB data width of 8, 16, 24 or 32 bits. Depending on the data width chosen, only one of the subsequent four configuration options is enabled. These options allow the number of memory locations to be set.

The addressing scheme can also be adjusted to control the address offsets at which successive physical memory locations appear. Successive locations can appear at 32-bit word offsets such that the first location is at offset 0x00, the second location is at offset 0x04, the third at 0x08, and so on. Alternatively, sequential addressing can be selected so that, starting from the first location, successive locations are at address offsets 0x00, 0x01, 0x02. Either addressing scheme can

be selected regardless of the APB data width setting. Table 2-1 through Table 2-4 show the memory organization for the various data width and addressing scheme settings.

Table 2-1 · Memory Organization for APB_DWIDTH = 32

	Word Aligned Addressing	Sequential Addressing
Contents	Address	Address
word 0	0x0000	0x0000
word 1	0x0004	0x0001
...
word 8191	0x7FFC	0x1FFF

Table 2-2 · Memory Organization for APB_DWIDTH = 24

	Word Aligned Addressing	Sequential Addressing
Contents	Address	Address
24 bit word 0	0x0000	0x0000
24 bit word 1	0x0004	0x0001
...
24 bit word 8191	0x7FFC	0x1FFF

Table 2-3 · Memory Organization for APB_DWIDTH = 16

	Word Aligned Addressing	Sequential Addressing
Contents	Address	Address
halfword 0	0x0000	0x0000
halfword 1	0x0004	0x0001
halfword 2	0x0008	0x0002
...
...
halfword 16383	0xFFFC	0x3FFF

Table 2-4 · Memory Organization for APB_DWIDTH = 8

	Word Aligned Addressing	Sequential Addressing
Contents	Address	Address
byte 0	0x00000	0x0000
byte 1	0x00004	0x0001
byte 2	0x00008	0x0002
...
...
...
byte 32767	0x1FFFC	0x7FFF

Example System

Figure 2-2 illustrates a typical system using Core8051s, CoreGPIO, and CoreAPBSRAM. APB bus interfaces can be auto-connected in SmartDesign using the “Auto Connect” menu option.

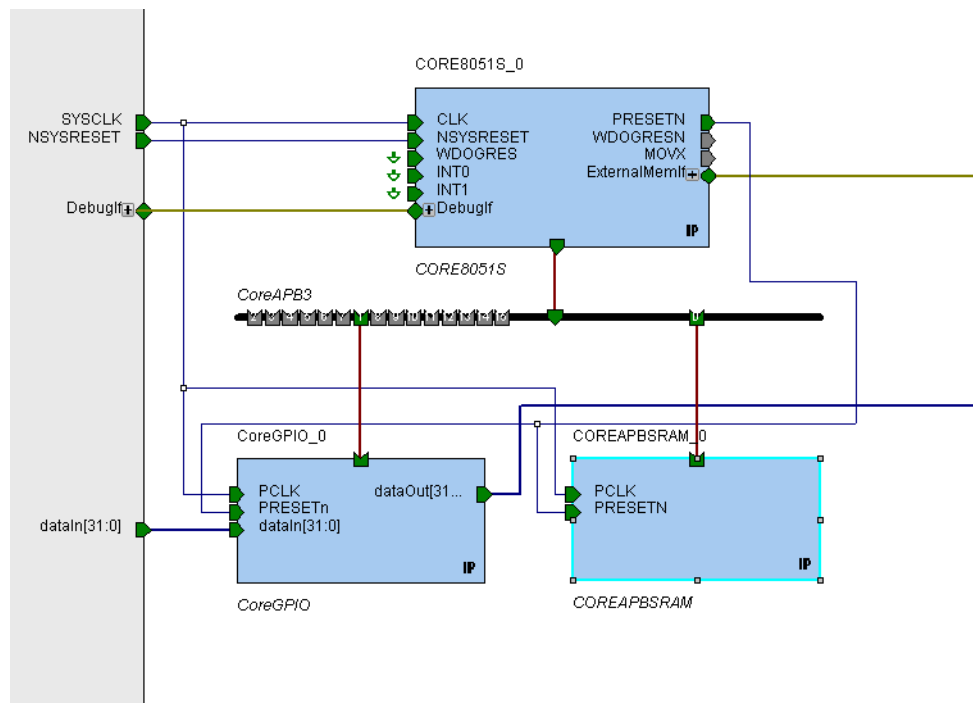


Figure 2-2 · Sample System with Core8051s, CoreGPIO, and CoreAPBSRAM

Registers

CoreAPBSRAM does not contain any memory mapped registers such as control or status registers.

Memory Map

The SRAM contained within CoreAPBSRAM appears at offset 0x0000 and continues up to an upper address which depends on the amount of SRAM configured.

Testing and Verification

CoreAPBSRAM comes with a simple user testbench, which can be invoked using Libero IDE. Refer to the Libero IDE online help for more information on running user testbenches for cores.

To run the user testbench, set the testbench configurable option to **user** when generating a CoreAPBSRAM design. Click the Simulation button in the Libero IDE GUI to run the testbench automatically.

Note: If CoreAPBSRAM is included as a component within a larger design, then the CoreAPBSRAM component should be set as the design root (from the right-click menu, select **Set As Root**), before running the user testbench.

User Testbench

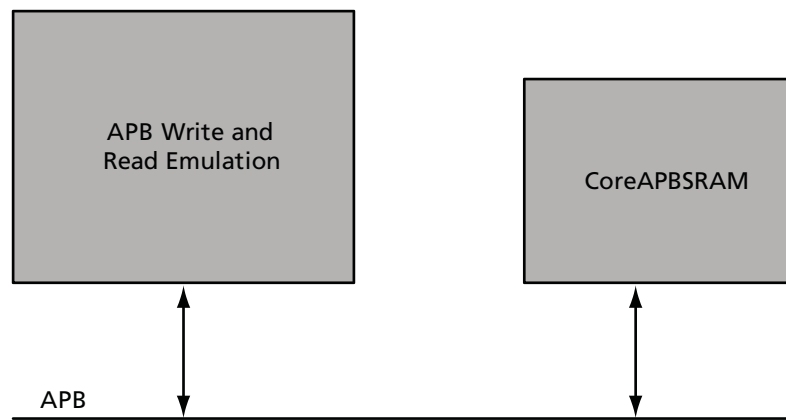


Figure 5-1 · CoreAPBSRAM User Testbench

The testbench operates by executing a series of accesses to CoreAPBSRAM using functions which emulate APB writes and reads. Values are written to the SRAM memory block contained within CoreAPBSRAM, and the same locations are then read back to check that the memory can successfully be written and read.

Various user modifiable generics/parameters are present in the user testbench to enable the variation of APB data width, number of memory locations, and type of addressing scheme. In addition to varying the parameter settings, other changes may be made to the user testbench to suit any specific needs.

Interface Description

Parameters

Table 6-1 describes the CoreAPBSRAM parameters and generics.

Table 6-1 · CoreAPBSRAM Generics/Parameters

Parameter	Values	Description
FAMILY	15, 16, 17, 20, 21, 22, 23	Must be set to match the supported FPGA family. 15 - ProASIC3 16 - ProASIC3E 17 - Fusion 20 - IGLOO 21 - IGLOOe 22 - ProASIC3L 23 - IGLOO PLUS
APB_DWIDTH	8, 16, 24, or 32	APB data width
NUM_LOCATIONS_DWIDTH32	512 to 8,192	Number of memory locations for 32-bit data width. Range is 512 to 8,192, in steps of 512.
NUM_LOCATIONS_DWIDTH24	512 to 8,192	Number of memory locations for 24-bit data width. Range is 512 to 8,192, in steps of 512.
NUM_LOCATIONS_DWIDTH16	512 to 16,384	Number of memory locations for 16-bit data width. Range is 512 to 16,384, in steps of 512.
NUM_LOCATIONS_DWIDTH08	512 to 32,768	Number of memory locations for 8-bit data width. Range is 512 to 32,768, in steps of 512.
ADDR_SCHEME	0 or 1	0 = consecutive memory locations are at 32-bit word aligned byte addresses; that is, at addresses 0x00, 0x04, 0x08, 0x0c, etc. 1 = consecutive memory locations are at sequential addresses; that is, at addresses 0x00, 0x01, 0x02, 0x03, etc.

Ports

Table 6-2 outlines the top-level signals for CoreAPBSRAM.

Table 6-2 · CoreAPBSRAM Ports

Name	Type	Description
PCLK	Input	APB System Clock. Reference clock for all internal logic
PRESETN	Input	APB active low asynchronous reset
PWDATA [APB_DWIDTH-1:0]	Input	APB write data
PRDATA[APB_DWIDTH-1:0]	Output	APB read data
PADDR[16:0]	Input	APB address bus.
PENABLE	Input	APB strobe. Indicates the second cycle of an APB transfer.
PSEL	Input	APB slave select
PWRITE	Input	APB write/read select signal
PREADY	Output	AMBA 3 APB ready signal for future AMBA 3 APB compliance, tied high
PSLVERR	Output	AMBA 3 APB transfer error signal for future AMBA 3 APB compliance, tied low

Note: Unless otherwise noted, all the signals above are active high.

Ordering Information

Ordering Codes

CoreAPBSRAM can be ordered through your local Actel sales representative. It should be ordered using the following number scheme: CoreAPBSRAM-XX, where XX is listed in [Table 7-1](#).

Table 7-1 · Ordering Codes

XX	Description
OM	RTL for Obfuscated RTL – multiple-use license
RM	RTL for RTL source – multiple-use license

Note: CoreAPBSRAM-OM is included free in the Libero IDE Catalog if you have a valid Libero IDE license.

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call 650.318.4480

From Southeast and Southwest U.S.A., call 650.318.4480

From South Central U.S.A., call 650.318.4434

From Northwest U.S.A., call 650.318.4434

From Canada, call 650.318.4480

From Europe, call 650.318.4252 or +44 (0) 1276 401 500

From Japan, call 650.318.4743

From the rest of the world, call 650.318.4743

Fax, from anywhere in the world 650.318.8044

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the [Actel Customer Support website \(www.actel.com/custsup/search.html\)](http://www.actel.com/custsup/search.html) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's [home page](http://www.actel.com), at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460

800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. [Sales office listings](#) can be found at www.actel.com/contact/offices/index.html.

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