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CoreApbNvm

Handbook

Actel
POWER MATTERS

Actel Corporation, Mountain View, CA 94043

Printed in the United States of America

Part Number: 50200139-1

Release: March 2009

Trademarks

Table of Contents

Introduction

Core Overview

CoreApbNvm allows advanced microcontroller bus architecture (AMBA) Peripheral Bus (APB) access to the Actel Fusion® nonvolatile memory (NVM), using a simple register-based access scheme. The core is designed to be configurable for use in various applications, using variable APB bus widths and a number of NVM instances (where supported). In addition, CoreApbNvm contains an Init/Config block which is used on reset to initialize RAM with the contents of NVM0. After reset, the Init/Config block can also be used to copy a user-specified number of words from NVM, starting at a user-specified base address.

Figure 1 shows the CoreApbNvm block diagram.

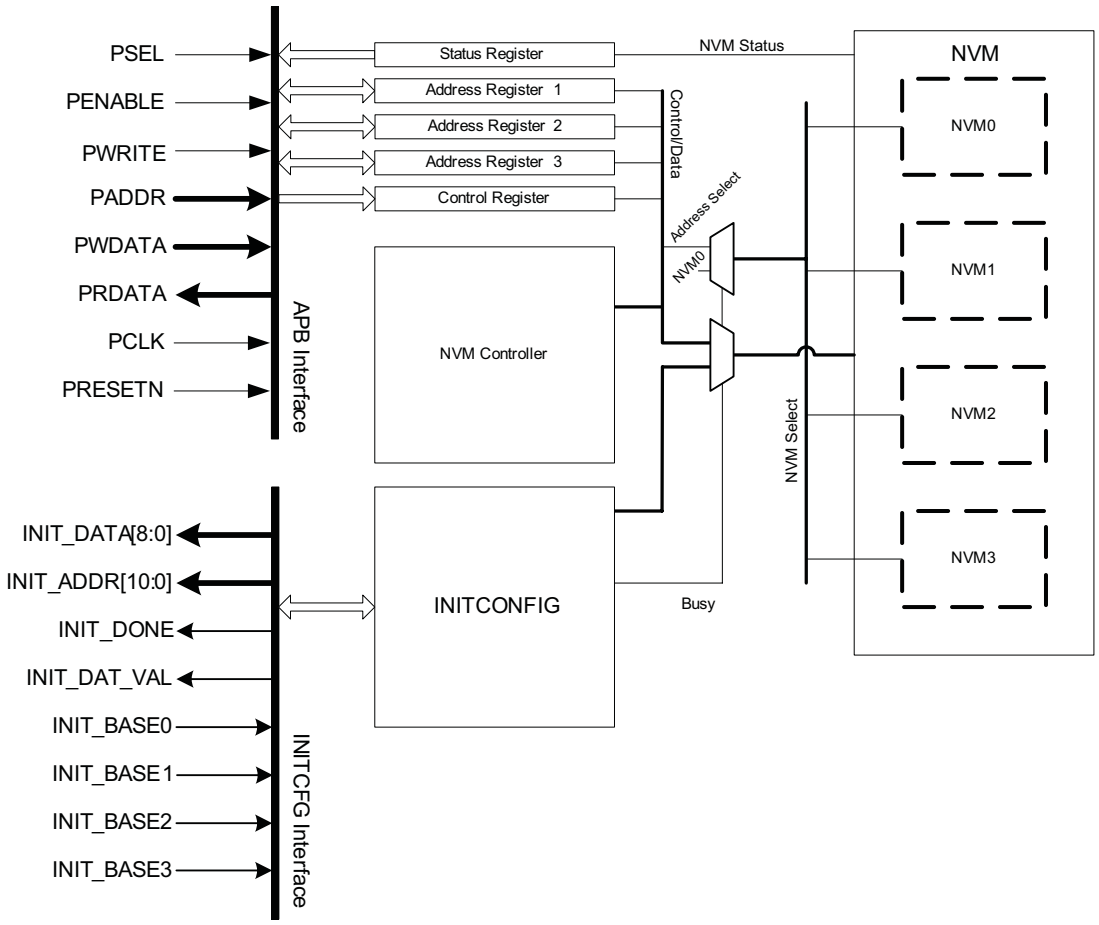

Figure 1 · CoreApbNvm Block Diagram

Key Features

CoreApbNvm has the following features:

- Fully AMBA 2 APB-compliant
- Compatible with AMBA 3 APB
- Multiple memory sizes and variable number of NVM blocks
- Configurable 8-, 16-, or 32-bit data bus size
- Configurable APB address width in range of 8 to 32 bits
- Init/Config block for fetching data from NVM to RAM, primarily for CoreABC soft-mode initialization
- Remapping function via Init/Config block to load RAM from different addresses of NVM
- Register controlled auto increment mode

Core Version

This handbook applies to CoreApbNVM v2.1.

Supported Families

All Fusion devices are supported by CoreApbNvm.

Utilization and Performance

Table 1 to Table 3 on page 7 describe the tile count and performance of CoreApbNvm for various configurations.

Table 1 · High-Tile Parameter Values

Family	Cells or Tiles			Utilization		Performance
	Sequential	Combinatorial	Total	Device	Percentage	
Fusion	159	458	617	AFS1500	1%	56.5 MHz

Note: Data in this table were achieved using typical synthesis and layout settings. Top-level parameters/generics that differ from the default values were set as follows: APB_DWIDTH = 32, NUM_INSTANCES = 4, INIT_ENABLED = 1.

Table 2 · Typical Parameter Values

Family	Cells or Tiles			Utilization		Performance
	Sequential	Combinatorial	Total	Device	Percentage	
Fusion	111	284	395	AFS090	17%	68.4 MHz

Note: Data in this table were achieved using typical synthesis and layout settings. Top-level parameters/generics that differ from the default values were set as follows: APB_DWIDTH = 8, NUM_INSTANCES = 1, INIT_ENABLED = 1.

Table 3 · Low-Tile Parameter Values

Family	Cells or Tiles			Utilization		Performance
	Sequential	Combinatorial	Total	Device		
Fusion	73	143	216	AFS090	9%	71.7 MHz

Note: Data in this table was achieved using typical synthesis and layout settings. Top-level parameters/generics that differ from the default values were set as follows: APB_DWIDTH = 8, NUM_INSTANCES = 1, INIT_ENABLED = 0.

Supported Interfaces

CoreApbNvm has an AMBA 2 APB Slave interface, with signals for an Init/Config Master interface and AMBA 3 APB operation.

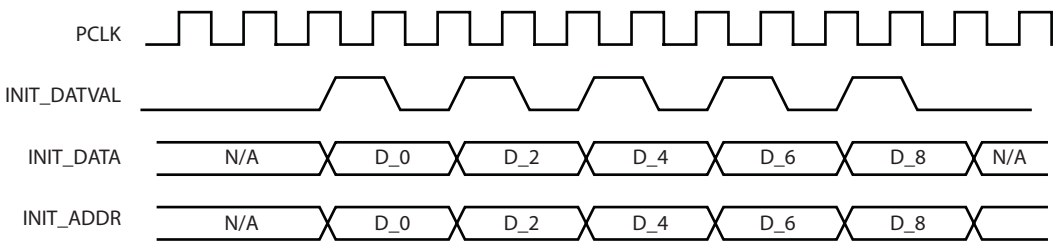

Figure 1-1 · Init/Config Interface Timing Diagram

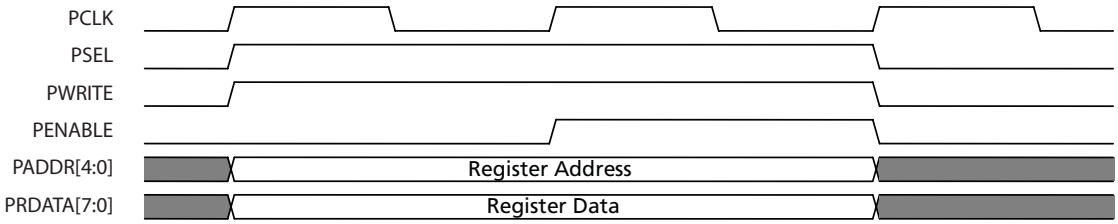

Figure 1-2 · APB Data Write Cycle

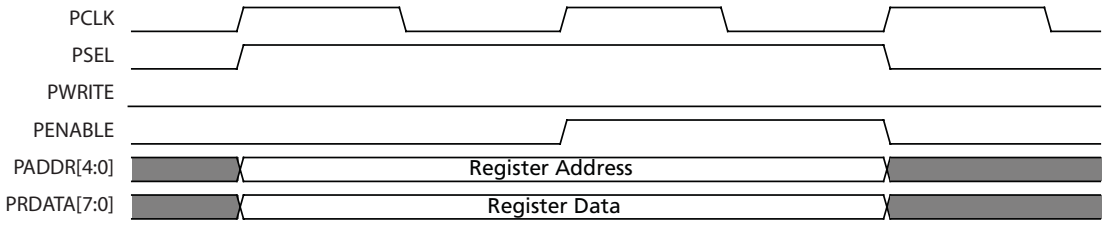

Figure 1-3 · APB Data Read Cycle

Tool Flows

SmartDesign

CoreApbNvm is available for download to the SmartDesign IP Catalog, via the Libero® Integrated Design Environment (IDE) web repository. For information on using SmartDesign to instantiate, configure, connect, and generate cores, please refer to the Libero IDE online help.

Figure 2-1 shows the CoreApbNvm configuration window with the corresponding top-level parameters.

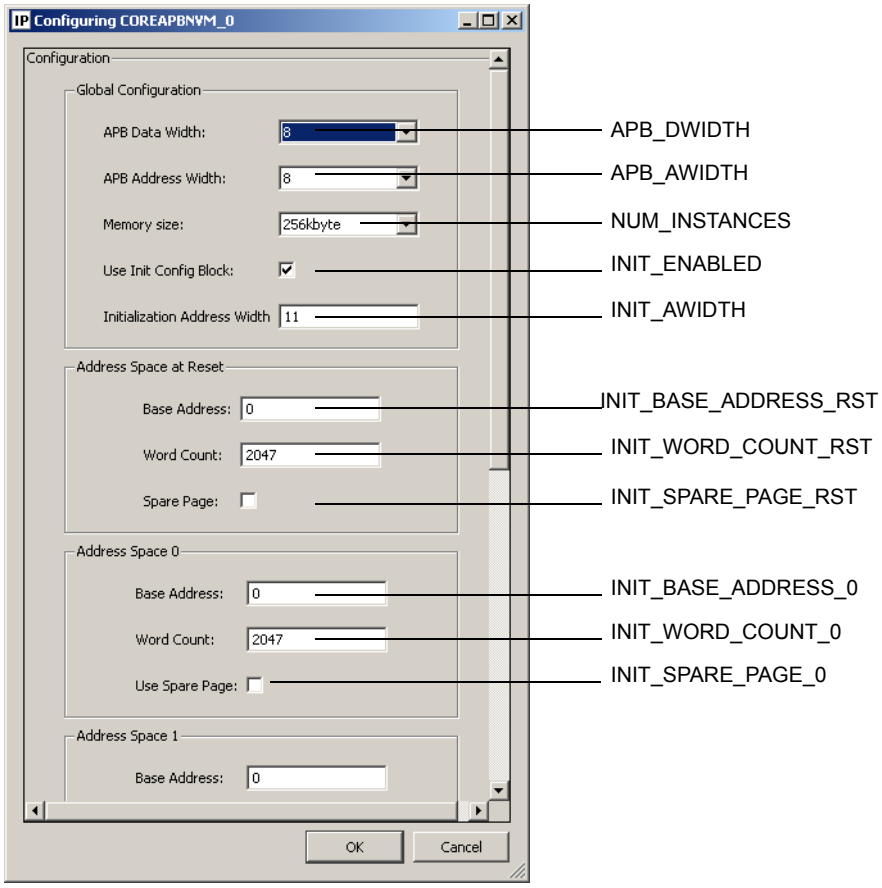

Figure 2-1 · CoreApbNvm Configuration Window

Example System

Figure 2-2 shows a typical system using CoreABC (*proc*), CoreAPB, and CoreApbNvm.

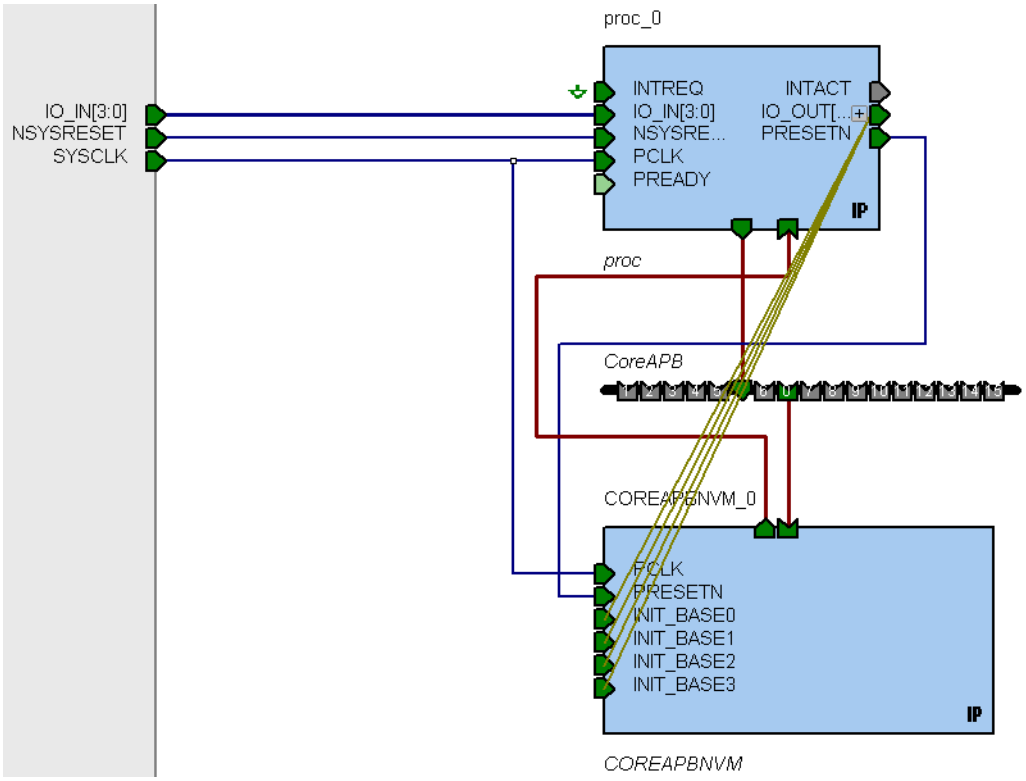

Figure 2-2 · Sample System with CoreABC and CoreAI

Note the connection between the Init/Config interface from CoreApbNvm (Init/Config Master) and CoreABC (Init/Config Slave). The CoreABC outputs connect directly to the custom initialization interface of CoreApbNvm. This connection allows for CoreABC to initiate a RAM-reload from different address spaces, so different programs can be loaded from the NVM during CoreABC execution, real-time. APB bus interfaces are autoconnected in SmartDesign.

3 NVM Addressing

Overview

Table 3-1 below illustrates the bits required to read/write an address in the NVM.

Table 3-1 · NVM Addressing Scheme

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM #		SP	18-bit NVM address																	

As shown in Table 3-1, 21 bits are required to access any address, including spare page, in the NVM. There are the 18 bits as specified in the *Actel Fusion Mixed-Signal FPGAs* datasheet for sector, page, block, and byte addressing; as well as 2 bits (NVM #) to specify which of four NVM instantiations are being accessed, and 1 bit (SP) to access the spare page of the sector currently being accessed.

In most cases, 21 address bits will not be available on the APB address bus and they will need to be stored in three 8-bit registers, as described in "Register Map" on page 15.

Note: The spare page of sector 0 is unavailable for any user data. Writes to this page will return an error, while reads will return all zeroes.

Auto-Increment Feature

CoreApbNvm has a register-controlled auto-increment feature, which is enabled by default. The auto-increment feature increments the address by the appropriate amount each time a NVM read or write operation is performed. The appropriate amount is calculated based on the APB data width (APB_DWIDTH parameter). In 8-bit mode, all bits of the NVM address are used; in 16-bit mode, bit 0 is ignored; and in 32-bit mode, bits 1 and 0 are ignored. The following increments are used:

- **8 bit mode:** increment by 1
- **16 bit mode:** increment by 2
- **32 bit mode:** increment by 4

4 Registers

Register Map

Table 4-1 describes the CoreApbNvm registers and their uses. The "Register Descriptions" section describes each register in detail.

Table 4-1 · Register Map

PADDR[4:0] (hex)	Type	Reset Value (hex)	Size (bits)	Brief Description
0x00	R/W	0x00	APB_DWIDTH	Address Register 1
0x04	R/W	0x00	8	Address Register 2 Unused if APB_DWIDTH = 32
0x08	R/W	0x00	8	Address Register 3 Unused if APB_DWIDTH = 16
0x0C	R/W	0x00	APB_DWIDTH	NVM Write Data
0x10	W	0x00	8	Control Register
0x14	R	0x80	8	Status Register
0x18	R	0x00	APB_DWIDTH	NVM Read Data

Note: The lower 2 bits of PADDR are unused.

Register Descriptions

Address Registers

Address registers are used to load addresses into the internal NVM address register when the load bit of the control register is written to. Reading values from the address register reads back the current NVM address stored in the internal (21 bit) NVM address register.

8-bit Registers

Address registers 1, 2, and 3 at address 0x00, 0x04, and 0x08 respectively, are used to store the 21-bit NVM address described in Table 3-1 on page 13. The actual address bit mapping scheme varies depending on the APB_DWIDTH parameter, as described in the following sections.

APB_DWIDTH = 8

The registers are all 8 bits wide and are mapped in the following manner:

Address Register 1: Bits 7 to 0 of the 21 bit NVM address.

Address Register 2: Bits 15 to 8 of the 21 bit NVM address.

Address Register 3: Bits 20:16 of the 21 bit NVM address.

Note: The top 3 bits of this register are unused.

APB_DWIDTH = 16

Address Register 1 is 16 bits wide and Address Register 3 is not used. Registers are mapped as follows:

Address Register 1: Bits 15 to 0 of the 21 bit NVM address.

Address Register 2: Bits 20 to 16 of the 21 bit NVM address.

Note: The top 3 bits of this register are unused.

Address Register 3: Unused.

APB_DWIDTH = 32

Address Register 1 is 32 bits wide and Address Registers 2 and 3 are not used.

Address Register 1: Bits 20 to 0 of the 21 bit NVM address.

Note: The top 12 bits of this register are unused.

Address Register 2: Unused.

Address Register 3: Unused.

NVM Write Data Register

APB_DWIDTH-Sized Register

This register stores the data that is to be written to the NVM. When a write operation is initiated, the data in this register is written to the NVM page buffer. For more information on the NVM write operation, please refer to the *Actel Fusion Mixed-Signal FPGAs* datasheet.

Control Register

8-bit Register

This write register controls the operation of CoreApbNvm. Table 4-2 describes the operation of the control register.

Table 4-2 · Control Register

Bit	7	6	5	4	3	2	1	0
	NVM dis. Auto-incr.	–	–	NVM program	NVM read enable	NVM write enable	-	Load addr

NVM disable auto-incr: This is a toggle bit. By default, auto-increment is enabled. Writing a 1 to this address disables auto-increment. Writing a 1 again re-enables it, etc.

NVM program: Programs the current page with data loaded in the Page Buffer.

NVM read enable: Initiates a read to the current Page Buffer.

NVM write enable: Initiates a write to the current Page Buffer.

Load addr: Loads the address stored in APB-addressable Address Registers 1, 2, and 3 into an internal 21-bit address register. NVM address, spare page, and NVM number are then read from this internal register.

Status Register

8-bit Register

This read register gives access to the current status of CoreApbNvm. Table 4-3 describes the operation of the status register.

Table 4-3 · Status Register

Bit	7	6	5	4	3	2	1	0
	NVM auto-incr.	INIT busy	Error	End of Page	-	NVM busy	NVM status [1]	NVM status [0]

NVM auto-incr: This is a status bit. 1 indicates auto-increment is enabled. 0 indicates it is disabled.

INIT busy: RAM init in progress

Error: If the NVM status of any NVM operation is not "00" as described below, this bit is set to 1, and is "sticky." The error bit can only be cleared by writing any value to the status register.

End of Page: Status bit indicates that the current NVM address is at the end of a page. Auto-increment will cease to increment the NVM address at this point.

NVM busy: Tied directly to the NVM busy output signal. Please refer to the *Actel Fusion Mixed-Signal FPGAs* datasheet for more information.

NVM status [1:0]: Status of the last operation completed:

00: Successful completion

01: Read-/Unprotect-Page: single error detected and corrected

Write: operation addressed a write-protected page

Erase-Page: protection violation

Program: Page Buffer is unmodified

Protection violation

10: Read-/Unprotect-Page: two or more errors detected

11: Write: attempt to write to another page before programming current page

Erase-Page/Program: page write count has exceeded the 10-year retention threshold

NVM Read Data

APB_DWIDTH-Sized Register

This read only register returns the read data from the last read operation.

Software Flow

CoreApbNvm supports both read and write operation through a series of APB register writes and reads. "Read Operation" and "Read Operation" on page 18 describe typical write and read operations. Note that both operations assume address auto-incrementing is enabled. Software flows with auto-increment disabled would involve more address register writes.

Read Operation

The algorithm for a typical read operation is shown in Figure 4-1 on page 19. The read operation is used to read data from NVM. As with the write operation, write an initial address to the three address registers, followed by a load address (0x01) write to the command register. This loads the value of the address registers into a contiguous 21-bit internal register. Subsequent NVM writes and reads are done using this address. This is the register that is auto-incremented when address auto-incrementing is enabled. The actual read is performed by writing 0x08 to the control register. This sets the read enable bit and performs an NVM read operation. If a page boundary is being crossed, this can take several cycles. Poll the status register for the NVM busy bit, as well as the status. Once the NVM finishes its read operation, NVM read data is copied into the read data register, where it can be accessed via APB.

Write Operation

The algorithm for a typical write operation is shown in Figure 4-2 on page 20. The write operation is used to write data to the NVM. Write an initial address to the three address registers, followed by a load address (0x01) write to the command register. This loads the value of the address registers into a contiguous 21-bit internal register. Subsequent NVM writes and reads are done using this address. This contiguous 21-bit internal register is auto-incremented when address auto-incrementing is enabled. Write data to the NVM write data register, followed by writing 0x04 to the control register (write enable is set). This writes the data in the data register to the NVM page buffer. After the NVM finishes its write (busy bit is polled), check to make sure the write status is okay.

CoreApbNvm does not keep track of page addresses. Program the current page once the end of the page has been reached.

Note: Once the end of a page is reached, the internal address register ceases to be auto-incremented (i.e., when the lower 7 bits of the address register are 0h7F).

Notes

While the Init/Config is active (Busy bit is high), the APB does not have write or read access to the NVM. However, all APB registers are accessible.

Init/Config pulls data only from NVM0.

On reset, Init/Config initializes RAM with data starting at INIT_BASE_ADDRESS_RST, described on Table 5-1 on page 21.

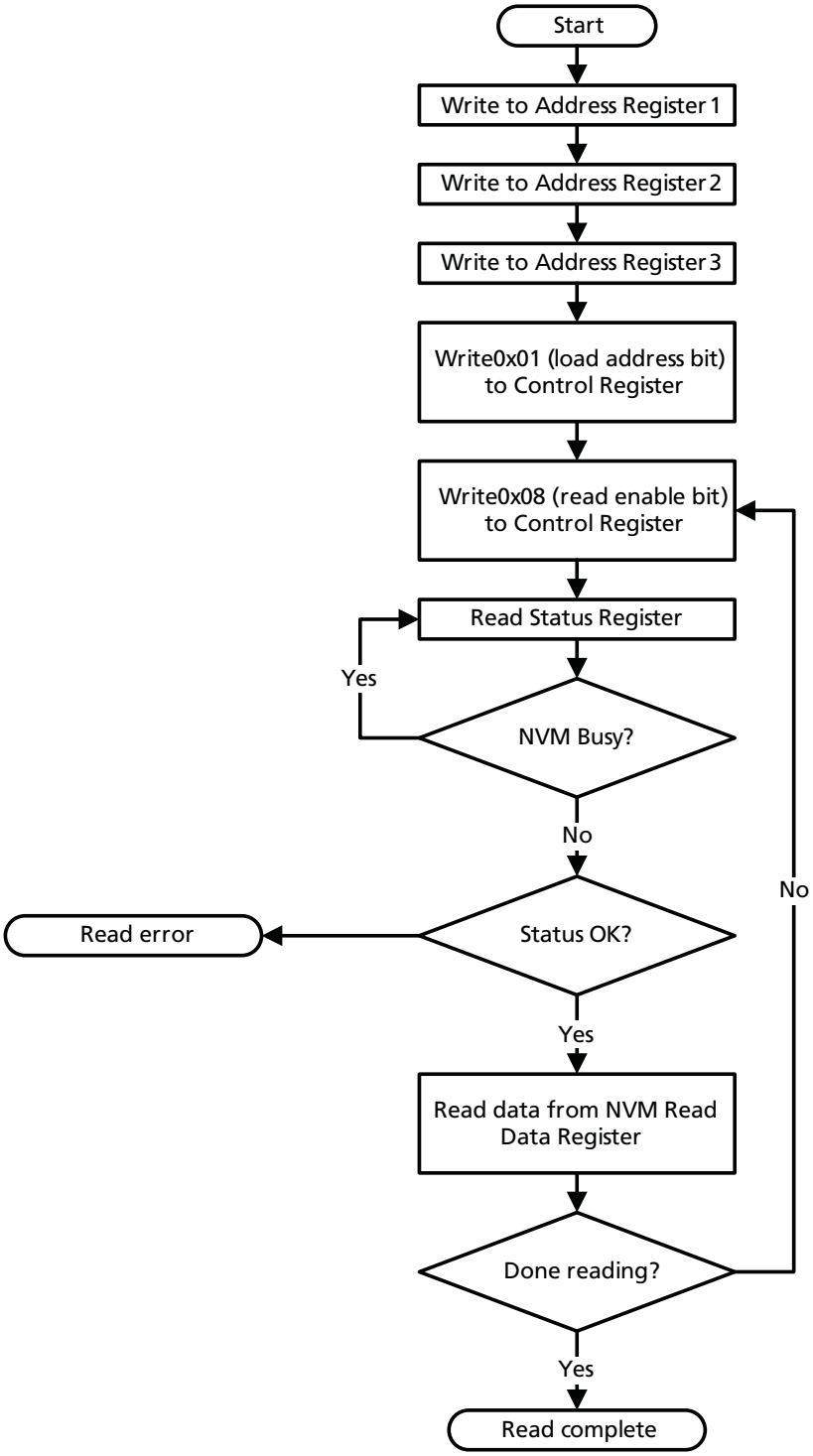

Figure 4-1 · Read Operation Flow Diagram

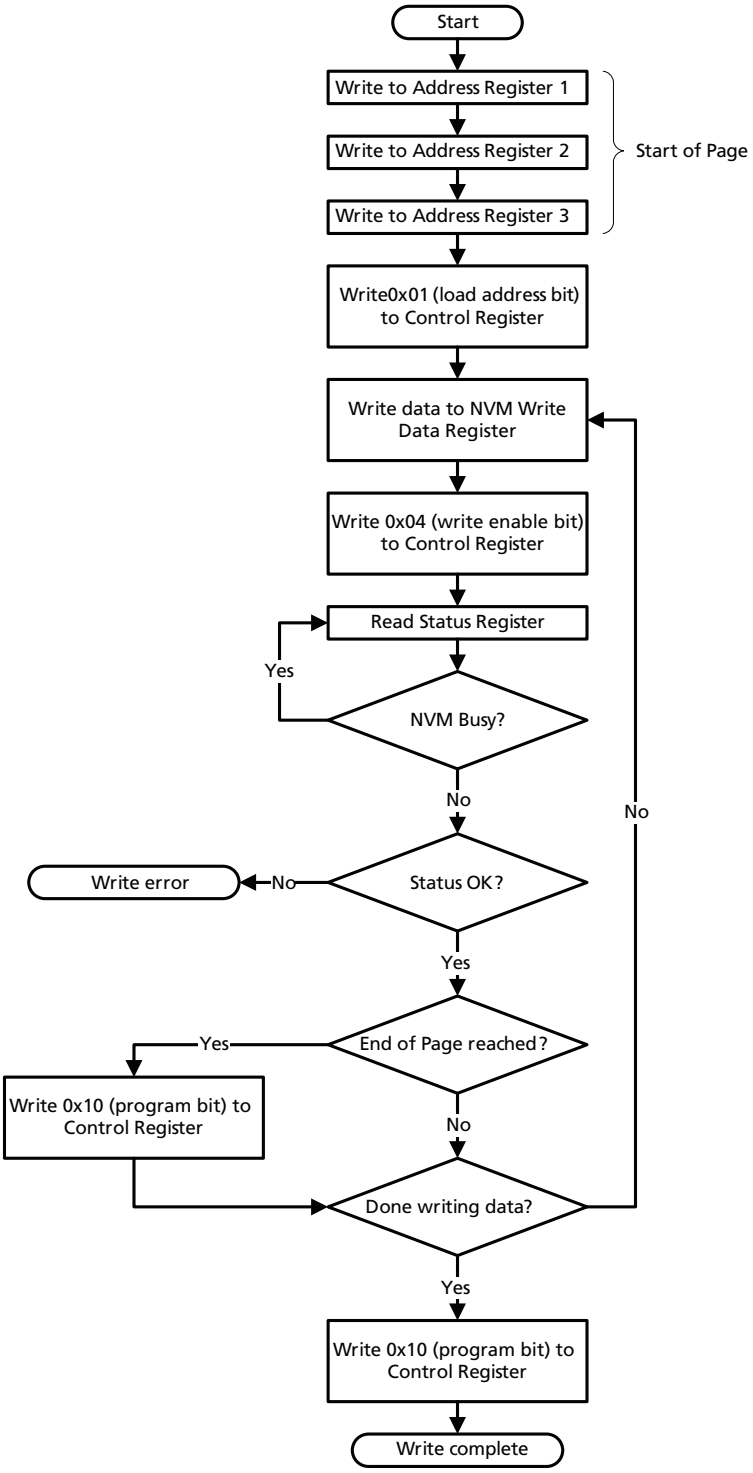

Figure 4-2 · Write Operation Flow Diagram

5 Interface Descriptions

Parameters

Table 5-1 outlines the generics for CoreApbNvm.

Table 5-1 · CoreApbNvm Generics

Parameter	Values	Description
FAMILY	17	Must be set to match the supported FPGA family 17 = Fusion
APB_DWIDTH	8,16,32	APB data width
APB_AWIDTH	8 - 21	APB address width
INIT_AWIDTH	11-16	Initialization address width
INIT_ENABLED	0 or 1	If 1, Init Config block is generated. If 0, Init Config block is not generated, outputs are tied low (except INIT_DONE, which is tied high).
INIT_BASE_ADDRESS_RST	0 to (2**18) - 1	Initialization base address at reset. Must be aligned to page boundary (0x00, 0x80, etc.)
INIT_WORD_COUNT_RST	0 to (2** INIT_AWIDTH) - 1	Number of (9-bit) words to be initialized to RAM, starting at the base address above, at reset.
INIT_SPARE_PAGE_RST	0 or 1	1 = data stored for this client is in spare page addresses (init at reset).
INIT_BASE_ADDRESS_0	0 to (2**18) - 1	Initialization base address 0 for post-reset initialization. Must be aligned to page boundary (0x00, 0x80, etc.)
INIT_WORD_COUNT_0	0 to (2** INIT_AWIDTH) - 1	Number of words to be initialized to RAM, starting at the base address above.
INIT_SPARE_PAGE_0	0 or 1	1 = data stored for this client is in spare page addresses.
INIT_BASE_ADDRESS_1	0 to (2**18) - 1	Initialization base address 1 for post-reset initialization. Must be aligned to page boundary (0x00, 0x80, etc.)
INIT_WORD_COUNT_1	0 to (2** INIT_AWIDTH) - 1	Number of words to be initialized to RAM, starting at the base address above.
INIT_SPARE_PAGE_1	0 or 1	1 = data stored for this client is in spare page addresses.

Table 5-1 · CoreApbNvm Generics (continued)

Parameter	Values	Description
INIT_BASE_ADDRESS_2	0 to (2**18) - 1	Initialization base address 2 for post-reset initialization. Must be aligned to page boundary (0x00, 0x80, etc.)
INIT_WORD_COUNT_2	0 to (2** INIT_AWIDTH) - 1	Number of words to be initialized to RAM, starting at the base address above.
INIT_SPARE_PAGE_2	0 or 1	1 = data stored for this client is in spare page addresses.
INIT_BASE_ADDRESS_3	0 to (2**18) - 1	Initialization base address 3 for post-reset initialization. Must be aligned to page boundary (0x00, 0x80, etc.)
INIT_WORD_COUNT_3	0 to (2** INIT_AWIDTH) - 1	Number of words to be initialized to RAM, starting at the base address above.
INIT_SPARE_PAGE_3	0 or 1	1 = data stored for this client is in spare page addresses.

Ports

Table 5-2 outlines the top-level signals for CoreApbNvm.

Table 5-2 · CoreApbNvm Ports

Name	Type	Description
APB Bus Signals		
PCLK	Input	APB System Clock – Reference clock for all internal logic
PRESETN	Input	APB active low asynchronous reset
PWDATA [APB_DWIDTH-1:0]	Input	APB write data
PRDATA [APB_DWIDTH-1:0]	Output	APB read data
PADDR [APB_AWIDTH-1:0]	Input	APB address bus.
PENABLE	Input	APB strobe – Indicates the second cycle of an APB transfer
PSEL	Input	APB Slave select
PWRITE	Input	APB write/read select signal

Table 5-2 · CoreApbNvm Ports (continued)

Name	Type	Description
PREADY	Output	AMBA 3 APB-ready signal for future AMBA 3 APB compliance, tied high
PSLVERR	Output	AMBA 3 APB transfer error signal for future AMBA 3 APB compliance, tied low
Init/Config signals		
INIT_DONE	Output	Initialization done signal. Asserted when initialization is completed.
INIT_DATA[8:0]	Output	Initialization data - to RAM blocks
INIT_ADDR[11:0]	Output	Initialization address - to RAM blocks
INIT_DATVAL	Output	Init data valid signal
INIT_BASE0	Input	Synchronous, active high signal to initialize RAM with NVM data starting at INIT_BASE_ADDRESS_0
INIT_BASE1	Input	Synchronous, active high signal to initialize RAM with NVM data starting at INIT_BASE_ADDRESS_1
INIT_BASE2	Input	Synchronous, active high signal to initialize RAM with NVM data starting at INIT_BASE_ADDRESS_2
INIT_BASE3	Input	Synchronous, active high signal to initialize RAM with NVM data starting at INIT_BASE_ADDRESS_3

Note: Unless otherwise noted, all of the signals above are active high.

6 Testing and Verification

CoreApbNvm comes with a simple user testbench, which can be invoked using Libero IDE. Refer to the Libero online help.

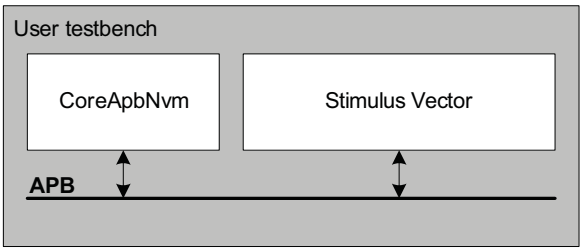

Figure 6-1 · CoreApbNvm User Testbench

The user testbench includes examples of how to do simple APB writes and reads using predefined read/write functions. Modify this testbench to suit any needs.

7 Ordering Information

Ordering Codes

CoreApbNVM can be ordered through your local Actel sales representative. It should be ordered using the following number scheme: CoreApbNVM-XX, where XX is listed in Table 7-1.

Table 7-1 · Ordering Codes

XX	Description
OM	RTL for Obfuscated RTL – multiple-use license
RM	RTL for RTL source – multiple-use license

Note: CoreApbNvm-OM is included free with a Libero IDE license.

A

List of Document Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v2.1)	Page
March 09	Corrected reference to CoreAI to CoreAPB.	12
	Added information about usage of Address Registers.	15
	Added End of Page support for Status Register bit 4.	17

B

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

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Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
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From Northwest U.S.A., call **650.318.4434**
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From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
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Actel Customer Technical Support Center

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Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/custsup/search.html) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/contact/offices/index.html.

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