CoreAHBLSRAM v2.2

Handbook

Microsemi

Revision History

Date	Revision	Change
March 2016	3	V2.2
December 2014	2	V2.1
January 2013	1	V2.0

Confidentiality Status

This is a non-confidential document.

Table of Contents

Preface

About this Document

This handbook provides details about the CoreAHBLSRAM DirectCore module, and how to use it.

Intended Audience

FPGA designers using Libero® System-on-Chip (SoC).

Introduction

Overview

CoreAHBLSRAM v2.2 provides access to the embedded large SRAM (LSRAM) and small SRAM (USRAM) blocks present on SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) family devices through AHB-Lite slave interface. It facilitates convenient access to SRAM by AHB masters.

Various configuration parameters or generics apply to CoreAHBLSRAM to control the amount of memory it provides access to, and to the data width of the core.

Key Features

CoreAHBLSRAM is a highly configurable core that provides the following features:

- Configurable memory size. Memory size can be configured from 2048 bytes to 139264 bytes, in steps of 2K bytes for LSRAMs (RAM1Kx18)
- Configurable memory size. Memory size can be configured from 128 bytes to 9216 bytes in steps of 128 bytes for USRAMs (RAM64x18)
- Configurable parameter to utilize either LSRAM or USRAM memory
- Merges multiple SRAM blocks to form large SRAMs or USRAMs
- AHB interface with data width of 32-bits

Core Version

This handbook is for CoreAHBLSRAM version 2.2.

Supported Families

- RTG4™
- SmartFusion®2
- IGLOO®2

Utilization and Performance

Table 1 shows the utilization and performance data for the SmartFusion2 (M2S050T), IGLOO2 (M2GL050T) and RTG4 (RT4G150) device families.

Speed Grade – STD, Core Voltage – 1.2V and Operating Condition- IND

Table 1 CoreAHBLSRAM Device Utilization and Performance

Family	AHB Data Width	SRAM Type	LSRAM Depth	USRAM Depth	Logic Elements				Frequency (MHz)
					Sequential	Combinational	Total	Percentage	
SmartFusion2	32	LSRAM	2048	128	99	76	175	0.15	170.3
SmartFusion2	32	USRAM	2048	9216	2663	3172	5835	5.18	167.4
IGLOO2	32	LSRAM	139264	128	2518	4273	6791	6.02	127.6
IGLOO2	32	USRAM	2048	3840	1219	1386	2605	2.31	199.9
RTG4	32	LSRAM	114688	128	2085	3526	5611	1.84	76.8
RTG4	32	USRAM	2048	128	205	198	403	0.13	115.0

Note: The data in this table is achieved using typical synthesis and layout settings. Frequency (in MHz) was set to 100 and speed grade was STD.

Functional Block

CoreAHBLSRAM consists of three major functional blocks: AHBL slave interface logic, SRAM control logic, and SRAM block instances as shown in Figure 1.

The IP core selects either the LSRAM (RAM1Kx18) or the USRAM (RAM64x18) based on the configurable parameter **SEL_RAM_TYPE.**

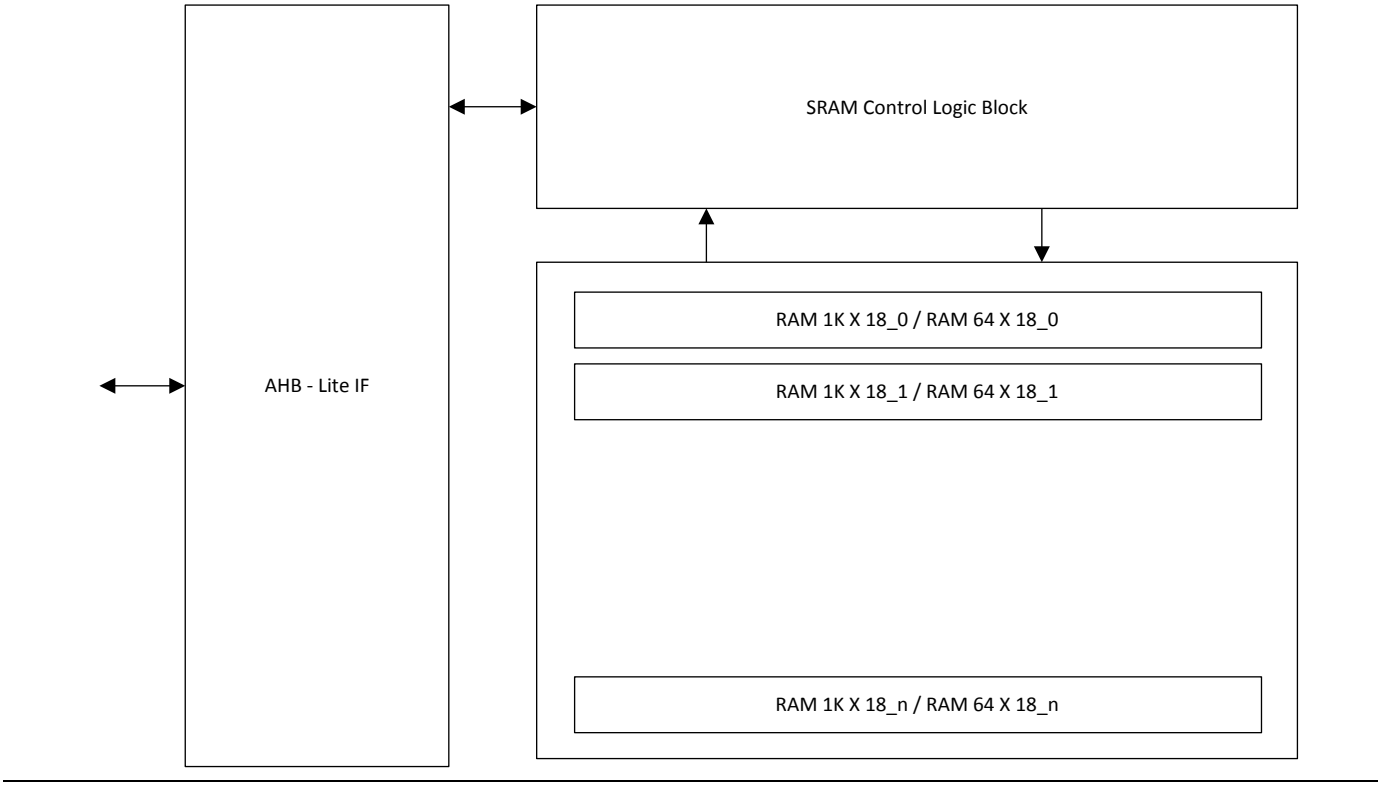

Figure 1 CoreAHBLSRAM Block Diagram

AHB-Lite Interface

The core implements standard AHB-Lite slave interface, which provides word, half-word, and byte accesses. Read and write accesses on the AHB slave interface gets converted into corresponding transfers on the LSRAM or USRAM.

SRAM Control Logic

The SRAM control logic block converts the AHB-Lite read/write transactions into the corresponding transactions on the LSRAM/USRAM memory block. The core provides configurable parameters to select LSRAM or USRAM. It also has the ability to merge blocks of memory based on the requirement.

The SRAM memory size can be configured from 2048 bytes to 139264 bytes (considering only 68 RAM1Kx18 LSRAMs) in steps of 2048 bytes for LSRAMs, and 128 bytes to 9216 bytes in steps of 128 bytes for USRAMs.

SRAM Block

Note: The availability of LSRAM and USRAM blocks in a specific die of supported families must be checked prior to design. Some dies will not have enough LSRAM and USRAM blocks to support the maximum density. However, they will support other densities.

The SRAM memory begins at address offset 0x0000 and continues to an upper limit, which depends on the configuration of the core.

The AHB-Lite interface supports transfer sizes of word (32-bit), half-word (16-bit), and byte (8-bit). The internal configuration of the SRAMs is always fixed to support the maximum data width (that is, 32-bit data width). Each LSRAM lowest configuration (2Kx8) is 16 Kbits that is 2 Kbytes.

The maximum density that CoreAHBLSRAM supports is 139,264 bytes, which can be achieved by using 68 blocks of LSRAM (that is, 68 x {2048x8} = 139,264 bytes).

In order to support the AHB-Lite Transfer Sizes (using HSIZE) of byte (8-bit) writes, half-word (16-bit) writes, and word (32-bit) writes, the core logic configures the memory to support byte writes, where each byte has its own separate write enable signal.

For each USRAM, the lowest configuration is 128x8. The maximum density CoreAHBLSRAM supports is 9,216 bytes, which can be achieved by using 72 blocks of USRAM (that is 72 x {128x8} = 9,216 bytes).

Interface Description

Ports

Table 2 I/O Signal Description

Port Name	Width	Direction	Description
AHBL Slave Interface Ports			
HCLK	1	In	AHB clock. All the AHB signals inside the block are clocked on the rising edge.
HRESETn	1	In	AHB Reset. This signal is active low. Asynchronous assertion and synchronous de-assertion. This is used to reset AHB registers in the block.
HSEL	1	In	AHBL slave select. This signal indicates that the current transfer is intended for the selected slave.
HADDR	18	In	AHBL address. 32-bit address on the AHBL interface. For LSRAM, only [17:0] bits are valid.
HWRITE	1	In	AHBL write. Where HIGH indicates that the current transaction is a write. Where LOW indicates that the current transaction is a read.
HREADYIN	1	In	When high, the HREADY signal indicates to the master and all slaves, that the previous transfer is complete.
HREADYOUT	1	Out	When high, the HREADYOUT signal indicates that a transfer has been completed on the bus. This signal can be driven low to extend a transfer.
HTRANS	2	In	AHBL transfer type. Indicates the transfer type of the current transaction. “00” = IDLE “01” = BUSY “10” = NONSEQUENTIAL “11” = SEQUENTIAL

Port Name	Width	Direction	Description
HSIZE	3	In	AHBL transfer size. Indicates the size of the current transfer (8/16/32/64 bit transactions only) “00” = 8 bit (byte) transaction “01” = 16 bit (half-word) transaction “10” = 32 bit (word) transaction “11” = 64 bit (double-word) transaction
HBURST	3	In	AHBL Burst type “000” = single “001” = incr “010” = wrap4 “011” = incr4 “100” = wrap8 “101” = incr8 “110” = wrap16 “111” = incr16
HWDATA	AHB_DWIDTH	In	AHBL write data. Write data from the AHBL master to the AHBL slave.
HRESP	1	Out	AHBL response status. When driven high at the end of a transaction, it indicates that the transaction was completed with errors. When driven low at the end of a transaction, it indicates that the transaction was completed successfully.
HRDATA	AHB_DWIDTH	Out	AHBL read data. Read data from the AHBL slave to the AHBL master.

Configuration Parameters

CoreAHBLSRAM Configurable Options

There are a number of configurable options that apply to CoreAHBLSRAM as shown in Table 3. If a configuration other than the default is required, select the configuration dialog box in SmartDesign to select appropriate values for the configurable options.

Table 3 CoreAHBLSRAM Configuration Options

Name	Valid Range	Default
FAMILY	19, 24, and 25	Supported FPGA family: 19: SmartFusion2 24: IGLOO2 25: RTG4 Default value is: 19
AHB_AWIDTH	32	A 32-bit System AHB address bus.
AHB_DWIDTH	32	Write/Read data bus on AHB side.
LSRAM_NUM_LOCATIONS_DWIDTH32	2 k to 139 k in steps of 2 k	Number of memory locations 2 k, 4 k, 6 k,.....,139 k (1 k = 1024 location) This is valid only for LSRAM memory configuration
USRAM_NUM_LOCATIONS_DWIDTH32	128 to 9 k	Number of memory locations 128, 256,.....,9 k (in steps of 128) This is valid only for USRAM memory configuration.
SEL_SRAM_TYPE	0 or 1	Used to select the fabric memory type 0: Select RAM1Kx18 LSRAM memory 1: Select RAM64x18 USRAM memory

Tool Flows

License

CoreAHBLSRAM is licensed free.

RTL

Complete RTL source code is provided for the core and testbenches.

SmartDesign

CoreAHBLSRAM is available for download in the Libero IP catalog through the web repository. Once it is listed in the catalog, the core can be instantiated using the SmartDesign flow. For information on using SmartDesign to configure, connect, and generate cores, refer to the Libero online help. An example instantiated view is shown in Figure 2.

After configuring and generating the core instance, basic functionality can be simulated using the test-bench supplied with the CoreAHBLSRAM. The testbench parameters automatically adjust to the CoreAHBLSRAM configuration. The CoreAHBLSRAM can be instantiated as a component of a larger design.

CoreAHBLSRAM is compatible with Libero SoC. For more information on using SmartDesign to instantiate and generate cores, refer to the *Using DirectCore in Libero® System-on-Chip (SoC) User Guide* or consult the Libero SoC online help.

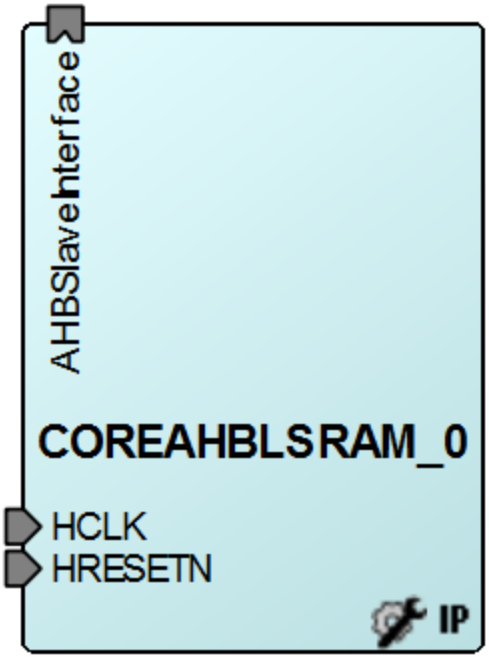

Figure 2 SmartDesign CoreAHBLSRAM Instance View

Configuring CoreAHBLSRAM in SmartDesign

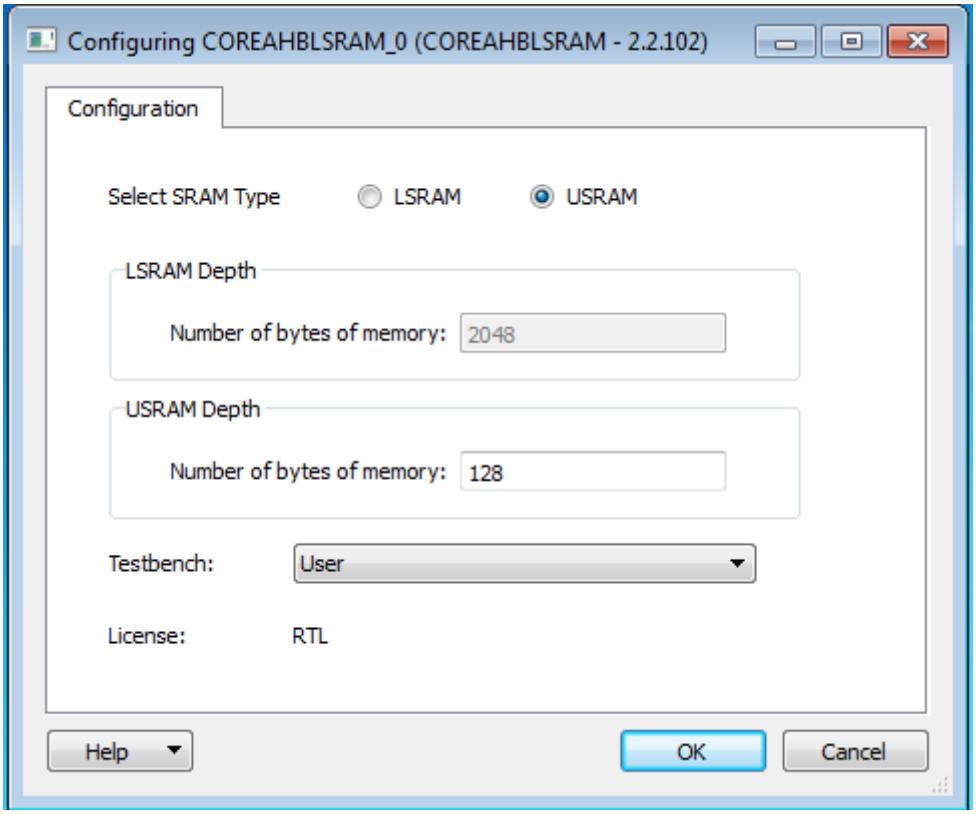

Figure 3 SmartDesign CoreAHBLSRAM Configuration window

Testbench Operation and Modification

A unified test-bench is used to verify and test CoreAHBLSRAM called a user test-bench.

User Test-bench

The user test-bench is included with the releases of CoreAHBLSRAM that verifies the operations of the CoreAHBLSRAM.

A simplified block diagram of the user test-bench is shown in Figure 4. The user test-bench instantiates a Microsemi DirectCore CoreAHBLSRAM DUT. The AHBLSRAM master model tasks drive write or read transactions to the DUT. The DUT in turn performs write and read to the SRAM memories which are instantiated inside the DUT. The checker model tasks checks and determines whether or not the transaction is successful and displays the result.

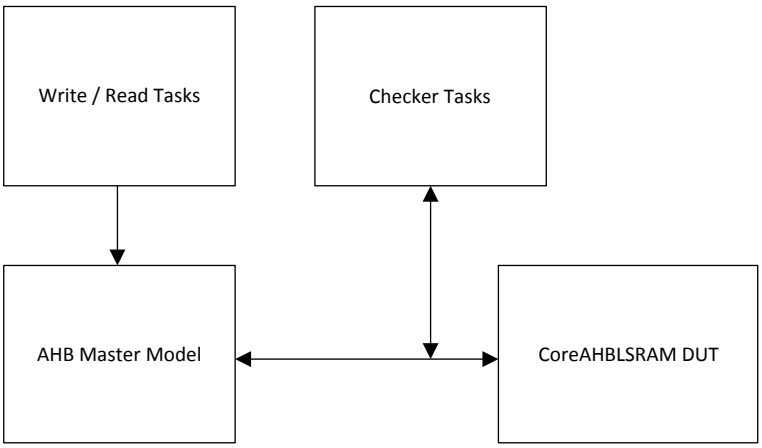

Figure 4 CoreAHBLSRAM User Test-bench

Register Map and Descriptions

CoreAHBLSRAM do not contain any registers.

List of Changes

The following table shows important changes made in this document for each revision.

Date and Revision	Change	Page
Revision 3 (March 2016)	Fixed bugs and issues. Refer to Table 2 in CoreAHBLSRAM v2.2 Release Notes	NA
Revision 2 (December 2014)	Added RTG4 and IGLOO2 support	NA
Revision 1 (January 2013)	Initial release	NA

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The technical support email address is soc_tech@microsemi.com.

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