RN0041
Release Notes
CoreABC v3.8

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Contents

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 12.0

Updated changes related to CoreABC v3.8.

1.2 Revision 11.0

Updated changes related to CoreABC v3.7.

1.3 Revision 10.0

Updated changes related to CoreABC v3.6.

1.4 Revision 9.0

Updated changes related to CoreABC v3.5.

1.5 Revision 8.0

Updated changes related to CoreABC v3.4.

1.6 Revision 7.0

Updated changes related to CoreABC v3.3.

1.7 Revision 6.0

Updated changes related to CoreABC v3.1.

1.8 Revision 5.0

Updated changes related to CoreABC v3.0.

1.9 Revision 4.0

Updated changes related to CoreABC v2.3.

1.10 Revision 3.0

Updated changes related to CoreABC v2.2.

1.11 Revision 2.0

Updated changes related to CoreABC v2.1.

1.12 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreABC v2.02.

2 CoreABC v3.8 Release Notes

This document accompanies the release of CoreABC v3.8. It describes the features and enhancements of CoreABC v3.8. This document contains information about the system requirements, supported families, implementations, and known issues and workarounds.

CoreABC (ABC = APB Bus Controller) is a simple, configurable, low gate count, programmable controller for use in advanced microcontroller bus architecture (AMBA®) version 3 advanced peripheral bus (APB) based designs. CoreABC is an AMBA3 APB master which can connect to and manage APB slave peripherals through an AMBA3 APB bus fabric component such as CoreAPB3.

CoreABC supports a comprehensive assembler based configurable instruction set architecture and extensive and flexible configuration of size and feature options, allowing it to be tuned to meet the resource constraints and processing power requirements of a wide variety of applications.

2.1 Features

- Extensive configurability, allowing very low cost and resource efficient implementations.
- Programmable APB bus controller.
- Hard, soft (RAM), or NVM instruction storage on Fusion devices; hard instruction storage on SmartFusion2, IGLOO2, RTG4, PolarFire, and PolarFire SoC devices; hard or soft instruction storage on other device families.
- Automatic detection of CoreAI in CoreABC's APB address space and auto-creation of analog configuration MUX (ACM) data, based on CoreAI configuration.
- APB interface can be configured for 8, 16, or 32-bit data.
- In NVM instruction storage mode, APB data type read and write access to the instruction store memory (through an APB slave interface) is supported.
- Built in general purpose input/output (GPIO) signals.
- Interrupt driven operation using interrupt request and interrupt active signals.

2.2 Interfaces

CoreABC has an AMBA3 APB master interface that typically connects to CoreAPB3.

In NVM instruction storage mode, an AMBA3 APB slave interface can be used to provide data type access to the instruction store.

In Soft instruction storage mode, an initialization and configuration interface is available for initializing the instruction store that contains RAM blocks.

2.3 Delivery Types

CoreABC is licensed in two ways, Obfuscated or register transfer level (RTL).

2.3.1 Obfuscated

Complete RTL code is provided for the core, allowing the core to be instantiated with SmartDesign. Simulation, synthesis, and layout can be performed within Libero. The RTL code for the core is obfuscated.

2.3.2 RTL

Complete RTL source code is provided for the core.

2.4 Supported Families

- PolarFire SoC
- PolarFire®
- RTG4™
- SmartFusion®2
- SmartFusion®
- Fusion
- IGLOO®2
- IGLOO
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3E
- ProASIC3L
- Axcelerator
- RTAX-S

2.5 Supported Tool Flows

Use Libero v8.6 SP1 or later with the CoreABC v3.7 release. Verilog users must use Synopsys Synplify AE v8.2.1 or later.

When using core in RTG4 device family, use SynplifyPro N-2018.03M-SP1-1 or later versions.

2.5.1 Installation Instructions

CoreABC is available through the Libero SoC IP Catalog. It can be downloaded from a remote web-based repository and installed into your local vault, ready for use. Once installed in Libero SoC, the core can be instantiated, configured, connected, and generated using the SmartDesign tool.

2.6 New Features and Devices

Added support for PolarFire devices. Currently, only hard mode instruction storage is supported for PolarFire devices.

2.7 Discontinued Features and Devices

No features have been discontinued in the CoreABC v3.8 release.

2.8 Known Issues and Workarounds

There are no known issues for CoreABC v3.8.

2.9 Resolved Issues in the v3.8 Release

Table 1 • **Resolved SARs in CoreABC v3.8 Release**

SAR	Description
103698	Added ECC support for RAM blocks in RTG4, PolarFire, and PolarFireSoC device families.
102909	Fixed: Simulation fails when Z register is disabled.
110036	Fixed: Error when RETISR instruction is used and number of I/O flags is less than 32.
78097	Fixed: Check HDL error - cannot call side-effect procedure sprintf from within pure function.
110718	Added synthesis pragma on/off on unsupported VHDL/Verilog constructs.
107848	Added support to automatically generate derived constraints.
105373	Resolved : CoreABC HB descriptions truncated.
103717 108018 110711	Added information in the core Release Note on the Simplify Pro version to be used when CoreABC is used in RTG4 device family.

2.10 Resolved Issues in the v3.7 Release

No issues resolved in v3.7, support for PolarFire devices added.

2.11 Resolved Issues in the v3.6 Release

Table 2 • **Resolved SARs in CoreABC v3.6 Release**

SAR	Description
11658	INITDATVAL port wrongly listed as INITDATAVAL in handbook.

2.12 Resolved Issues in the v3.5 Release

Table 3 • **Resolved SARs in CoreABC v3.5 Release**

SAR	Description
11513	(Enhancement) Support AND, >>, <=, 0b0000 on immediate values.
17862	(Enhancement) Generate .h mem file suitable for #including in C init code.
22240	(Enhancement) Double-clicking a token in Program Editor should select it.
30970	(Enhancement) Hazard flag for PUSH used without CALL/RETURN.

2.13 Resolved Issues in the v3.4 Release

Table 4 • **Resolved SARs in CoreABC v3.4 Release**

SAR	Description
36938 36941 38219	"min" and "max" should not be used for function names in VHDL.
39931	Unmatched "synthesis translate_off" in textio.vhd file.

2.14 Resolved Issues in the v3.3 Release

Table 5 • **Resolved SARs in CoreABC v3.3 Release**

SAR	Description
22474	Configurator analysis view does not always report the correct program counter value.
29113	Errors with multiple instances of CoreABC in a VHDL design flow.
29600	Added explicit support for SmartFusion device family.

2.15 Resolved Issues in the v3.1 Release

Table 6 • **Resolved SARs in CoreABC v3.1 Release**

SAR	Description
25193	Compilation of NVM mode CoreABC design fails for AFS090 device

2.16 Resolved Issues in the v3.0 Release

Table 7 • **Resolved SARs in CoreABC v3.0 Release**

SAR	Description
21840 11788	Some instruction sequences result in erroneous behavior due to a multiplexer select bit not being properly controlled.
11789	Memory files not generated correctly in Soft mode.
11574	ACM lookup table data incorrect/incomplete for certain CoreAI configurations.
11597	Incorrect library mappings in the debugblk.vhd file causes problems in the obfuscated VHDL flow.
12014	Initialization and configuration (InitCfg) interface not grouped as bus interface.
23069	Instruction skipped when returning from active low interrupt.
23356	Failing conditional checks based on general purpose inputs 10, 18, and 27.

2.17 Resolved Issues in the v2.3 Release

Table 8 • **Resolved SARs in CoreABC v2.3 Release**

SAR	Description
63779	Instruction enhancements have been made to support the following: • ALU operations on RAM contents • Indirect APB addressing • IOWRT and IOREAD enhancements • Multiply support
61286	The Analysis window calculates the INITWIDTH value from the number of instructions in use rather than the configured ICWIDTH parameter.
63977 63697	Pressing the ESC key in the assembler exits the assembler without saving edits. The GUI now opens a confirmation window before exiting when changes have been made.
64835	CoreABC firmware is lost if analyze is used instead of saving it.
64031	Configuration GUI incorrectly gives an error when the loop counter (Z register) is disabled.
64585	When using the numeric keypad, double digits are entered.
64586	Cannot use "DEF ADDRESS 0" in the configurator.
64588	Analysis does not check if instructions are enabled. This information is shown in the parameters window. The parameters window must be checked prior to exiting the Configurator to verify that only enabled instructions have been used.
65657	The Assembler/Configurator allows saving inconsistent configurations and programs. Users must verify that no warnings are shown in both the Parameters and Program windows of the Configurator before exiting the Configurator.

2.18 Resolved Issues in the v2.2 Release

Table 9 • **Resolved SARs in CoreABC v2.2 Release**

SAR	Description
63778	APB access to slots >= 2. When accessing slots 2, 6, 8, etc., CoreABC would actually access APB slot 0. When addressing slots 3, 5, 7, 9, etc., the core would actually address slot 1. This has been corrected. The core now correctly accesses the appropriate APB slot.
64208	RETURN clears INTACT. The RETURN instruction clears the internal interrupt active bit and the INTACT output. Only the RETISR instruction should have cleared this bit.

2.19 Resolved Issues in the v2.1 Release

The v2.1 release contains an updated handbook. No changes have been made to the RTL code apart from updating version numbers in the source files.

2.20 Resolved Issues in the v2.02 Release

This was the first core production release; hence there are no resolved issues from a previous release.