Core16550 v3.3 Release Notes

This is the production release for the Core16550 IP core. This release note describes the features and enhancements and also contains information about system requirements, supported families, implementations, and known issues and workarounds.

Key Features

Following are the key features of Core16550:

- Transmitter and receiver are each buffered with up to 16-byte FIFOs to reduce the number of interrupts presented to the CPU
- Adds or strips standard asynchronous communication bits (start, stop, and parity)
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud generator
- Modem control functions (CTSn, RTSn, DSRn, DTRn, RIn, and DCDn)
- Advanced Peripheral Bus (APB) register interface

Delivery Types

Core16550 is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with Libero System-on-Chip (SoC). Simulation, Synthesis, and Layout can be performed with Libero SoC. The RTL code for the core is obfuscated and some of the testbench source files are not provided. They are precompiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- Fusion
- IGLOO™/e
- ProASIC®3/E
- ProASIC PLUS®
- Axcelerator®
- RTAX-S
- SmartFusion®
- SmartFusion®2
- IGLOO®2
- RTG4™

Supported Tool Flows

Use Libero SoC v11.5 or IDE v9.2, or later with this Core16550 release.

Install Instructions

The Core16550 CPZ file must be installed using Libero SoC. In the catalog window of Libero SoC, click settings button and select "Add Core to Vault". Once installed in Libero SoC, the core can be instantiated, configured, and exported to the Libero SoC environment.

For RTL and Obfuscated versions of the core, the FlexLM license must be installed and CoreConsole must be restarted before the core can be exported.

Consult Libero SoC help for further instructions regarding core installation and licensing.

Documentation

The release contains a copy of the *Core16550 Handbook*. The handbook describes the core functionality, gives implementation suggestions, and provides step-by-step instructions on how to simulate, synthesize, and place-and-route this core. The documentation may be viewed by right-clicking in the **Core Selection Pane** in Libero SoC after the core has been installed.

For more information about Intellectual Property, visit: *http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores*. For updates and additional information about software, FPGAs, and hardware, visit: *www.microsemi.com.*

Supported Test Environments

The following test environments are supported for Core16550:

- VHDL user testbench
- Verilog user testbench

Discontinued Features and Devices

No features have been discontinued in the v3.3 release.

New Features and Devices

The v3.3 release adds support of RTG4.

Resolved Issues in the v3.3 Release

***Table 1-1* • SARs and Descriptions**

SAR Number	Description
57400	Added RTG4 Support

Known Issues and Workarounds

None.

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